Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

ORCA® ORT82G5 0.622/1.0—1.25/2.0—2.5/3.125 Gbits/s Backplane Interface FPSC

Introduction

Lucent Technologies Microelectronics Group has developed a next generation FPSC intended for high-speed serial backplane data transmission. Built on the Series 4 reconfigurable embedded system-on-chips (SoC) architecture, the ORT82G5 is made up of backplane transceivers containing eight channels, each operating at up to 3.125 Gbits/s (2.5 Gbits/s data rate), with a full-duplex synchronous interface with built-in clock and data recovery (CDR), along with up to 400k usable FPGA system gates. The CDR circuitry is a macrocell available from Lucent's smart silicon macro library, and has already been implemented in numerous applications including ASICs, standard products, and FPSCs to create interfaces for SONET/SDH, STS-48/STM-16, STS-192/STM-64, and 10 Gbit Ethernet applications. With the addition of protocol and access logic such as protocol-independent framers, asynchronous transfer mode (ATM) framers, packet-over-SONET (POS) interfaces, and framers for HDLC for Internet protocol (IP), designers can build a configurable interface retaining proven backplane driver/receiver technology. Designers can also use the device to drive high-speed data transfer across buses within a system that are not SONET/SDH based. For example, designers can build a 20 Gbits/s bridge for 10 Gbits/s Ethernet; the high-speed SERDES interfaces can comprise two XAUI interfaces with configurable back-end interfaces such as XGMII or POS-PHY4. The ORT82G5 can also be used to provide a full 10 Gbits/s backplane data connection with protection between a line card and switch fabric.

The ORT82G5 offers a clockless high-speed interface for interdevice communication on a board or across a backplane. The built-in clock recovery of the ORT82G5 allows for higher system performance, easier-to-design clock domains in a multiboard system, and fewer signals on the backplane. Network designers will benefit from the backplane transceiver as a network termination device.The first version of the device supports 8b/10b encoding/decoding and link state machines for Ethernet, fibre-channel, and *InfiniBand* *. Version II adds SONET data scrambling/descrambling, streamlined SONET framing, transport overhead handling, plus the programmable logic to terminate the network into proprietary systems. For non-SONET applications, all SONET functionality is hidden from the user and no prior networking knowledge is required.

* *InfiniBand* is a trademark of Infiniband Trade Association.

Table 1. ORCA ORT82G5 Family—Available FPGA Logic

Device	PFU Rows	PFU Columns	Total PFUs	User I/O	LUTs	EBR Blocks	EBR Bits (k)	Usable† Gates (k)
ORT82G5	36	36	1296	432	10,368	12	111	380—800

† The embedded core and interface are not included in the above gate counts. The usable gate counts range from a logic-only gate count to a gate count assuming that 20% of the PFUs/SLICs are being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit plus each block has an additional 25k gates. 7k gates are used for each PLL and 50k gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate count calculations.

Embedded Function Features

- High-speed SERDES programmable serial data rates of 622 Mbits/s (SONET only), 1.25 Gbits/s, 2.5 Gbits/s, and 3.125 Gbits/s.
- Asynchronous operation per receive channel (separate PLL per channel).
- Transmit pre-emphasis (programmable) for improved receive data eye opening.
- Receiver energy detector to determine if a link is active.
- 8-bit (SONET or 8b/10b) or 10-bit (raw data) parallel internal bus for data processing in FPGA logic.
- Provides a 10 Gbits/s backplane interface to switch fabric with protection. Also supports port cards at 622 Mbits/s or 2.5 Gbits/s.
- 3.125 Gbits/s SERDES compliant with XAUI serial data specification for 10 Gbit Ethernet applications with protection.
- Compliant to *InfiniBand* 1.0 physical layer specification.
- Compliant to fibre-channel physical layer specification.
- Allows wide range of applications for SONET network termination, as well as generic data moving for high-speed backplane data transfer.
- No knowledge of SONET/SDH needed in generic applications. Simply supply data (100 MHz—156.25 MHz clock) and optionally a frame pulse.
- High-speed interface (HSI) function for clock/data recovery serial backplane data transfer without external clocks.
- Eight-channel HSI function provides 2.5 Gbits/s serial user data interface per channel for a total chip bandwidth of 20 Gbits/s (full duplex).
- SERDES has low-power CML buffers. Support for 1.5 V/1.8 V I/Os.
- Programmable STS-12 or STS-48 framing in SONET mode.
- Powerdown option of SERDES HSI receiver on a per-channel basis.
- Selectable 8b/10b coder/decoder or SONET scrambler/descrambler (added for version 2).
- SERDES HSI automatically recovers from loss-of-clock once its reference clock returns to normal operating state.
- Frame alignment across multiple ORT82G5 devices for work/protect switching at STS-768/STM256 and above rates in SONET mode.
- Most XAUI features for 10 Gbit Ethernet are embedded including the required link state machine.
- In-band management and configuration through transport overhead extraction/insertion in SONET mode.
- Supports transparent mode where the only insertion is A1/A2 framing bytes in SONET mode.
- Built-in boundry scan (*IEEE* * 1149.1 and 1149.2 JTAG), including the SERDES interface.
- FIFOs align incoming data across all eight channels (all eight channels, two groups of four channels, or four groups of two channels). Optional ability to bypass alignment FIFOs for asynchronous operation between channels. (Each channel includes its own clock and frame pulse or comma detect.)
- Addition of two 4K X 36 dual-port RAMs with access to the programmable logic.

Intellectual Property Features

Programmable logic provides a variety of yet-to-be standardized interface functions, including the following Lucent ME IP core functions:

- 10 Gbits/s Ethernet as defined by *IEEE* 802.3ae:
  - — XGMII for interfacing to 10 Gbits/s Ethernet MACs. XGMII is a 156 MHz double data rate parallel short reach (typically less than 2") interconnect interface.
  - — $X^{59} + X^{19} + X^{1}$ scrambler/descrambler for 10 Gbits/s Ethernet.
  - — 64b/66b encoders/decoders for 10 Gbits/s Ethernet.
  - — XAUI to XGMII translator, including dual XAUI protection.
- POS-PHY interface for 10 Gbits/s SONET/SDH and OTN systems and some 10 Gbits/s Ethernet systems to allow easy integration of *InfiniBand*, fibre-channel, and 10 Gbits/s Ethernet in data over fibre applications.
- Ethernet MAC functions at 10/100 Mbits/s, 1 Gbits/s, and 10 Gbits/s.
- Other functions such as Fibre-Channel and *InfiniBand* link layer IP cores also plan to be developed.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Programmable Features

- High-performance programmable logic:
  - — 0.13 µm 7-level metal technology.
  - — Internal performance of >250 MHz.
  - — Over 400k usable system gates.
  - — Meets multiple I/O interface standards.
  - — 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - — LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - — Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - — Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - — Two slew rates supported (fast and slew-limited).
  - — Fast-capture input latch and input flip-flop (FF)/latch for reduced input setup time and zero hold time.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
  - — Off-chip clock drive capability.
  - — Two-input function generator in output path.
- New programmable high-speed I/O:
  - — Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I and II), HSTL (Class I, III, IV), ZBT, and DDR.
  - — Double-ended: LVDS, bused-LVDS, and LVPECL.
  - — Customer defined: ability to substitute arbitrary standard cell I/O to meet fast moving standards.
- New capability to (de)multiplex I/O signals:
  - — New DDR on both input and output at rates up to 311 MHz (622 MHz effective rate).
  - — New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).
- Enhanced twin-quad programmable function unit (PFU):
  - — Eight 16-bit look-up tables (LUTs) per PFU.
  - — Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - — New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - — New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - — 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - — Flexible fast access to PFU inputs from routing.
  - — Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and *PAL**-like and-or-invert (AOI) in each programmable logic cell.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provides optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 200 MHz.
- New 200 MHz embedded quad-port RAM blocks, 2 read ports, 2 write ports, and 2 sets of byte lane enables. Each embedded RAM block can be configured as:
  - — 1—512 x 18 (quad-port, two read/two write) with optional built in arbitration.
  - — 1—256 x 36 (dual-port, one read/one write).
  - — 1—1k x 9 (dual-port, one read/one write).
  - — 2—512 x 9 (dual-port, one read/one write for each).
  - — 2 RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - — Supports joining of RAM blocks.
  - — Two 16 x 8-bit content addressable memory (CAM) support.
  - — FIFO 512 x 18, 256 x 36, 1k x 9, or dual 512 x 9.
  - — Constant multiply (8 x 16 or 16 x 8).
  - — Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 66 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.

* *PAL* is a trademark of Advanced Micro Devices, Inc.

Programmable Features (continued)

- Built-in testability:
  - — Full boundary scan (*IEEE* 1149.1 and Draft 1149.2 JTAG).
  - — Programming and readback through boundary scan port compliant to *IEEE* Draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provide optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock to out I/O specifications and may provide reduced ground bounce for output buses by allowing flexible delays of switching output buffers.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC**860 and *PowerPC* II high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA*† specification 2.0 AHB system bus (*ARM*† processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard cell blocks.
- New network PLLs meet ITU-T G.811 specifications and provide clock conditioning for DS-1/E-1 and STS-3/STM-1 applications.
- Flexible general purpose PPLLs offer clock multiply (up to 8x), divide (down to 1/8x), phase shift, delay compensation, and duty cycle adjustment combined.
- Variable size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.
- *ORCA* Foundry 2000 development system software. Supported by industry-standard CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets universal test and operations PHY interface for ATM (UTOPIA) Levels 1, 2, and 3; as well as POS-PHY3. Also meets proposed specifications for UTOPIA Level 4 for and POS-PHY3 (2.5 Gbits/s) and POS-PHY4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.
- Two new edge clock routing structures allow up to seven high-speed clocks on each edge of the device for improved setup/hold and clock to out performance.

* *PowerPC* is a registered trademark of International Business Machines, Inc.
† *AMBA* is a trademark, and *ARM* is a registered trademark of Advanced RISC Machines Limited.

Block Diagrams

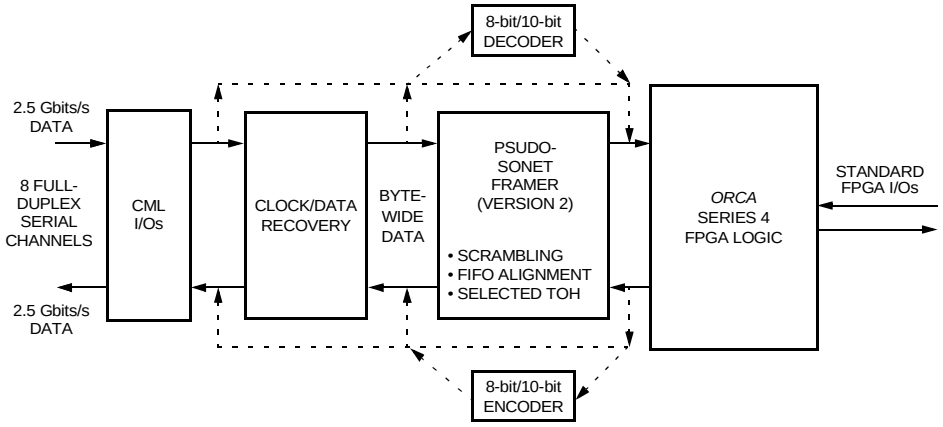


Figure 1. ORT82G5 Block Diagram

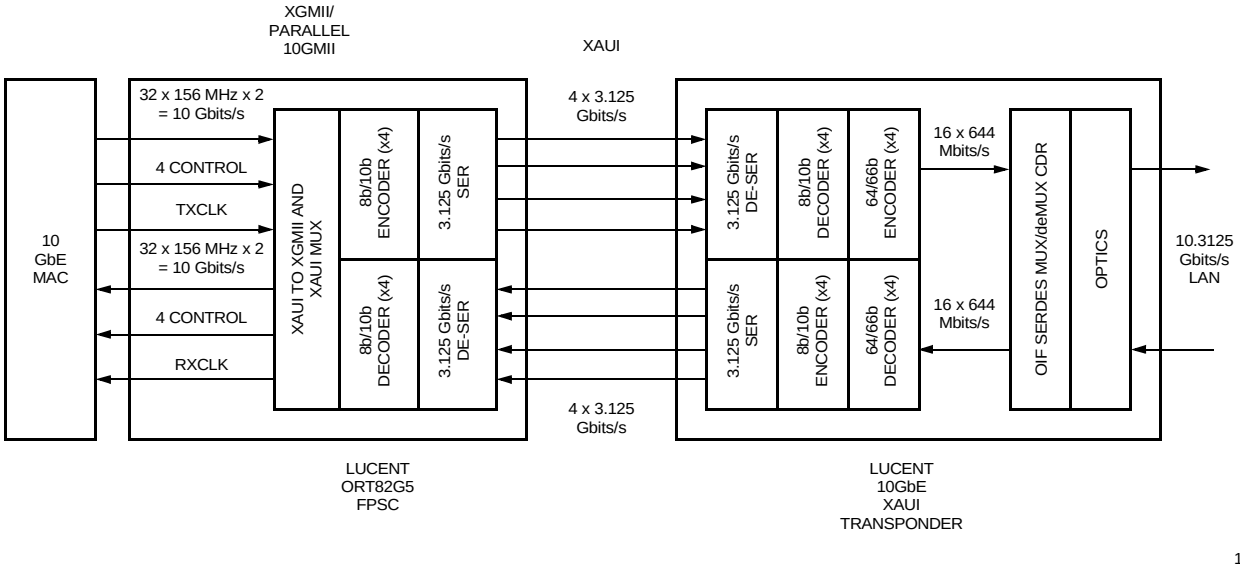


Figure 2. 10 Gbits/s Ethernet: Serial LAN

Block Diagrams (continued)

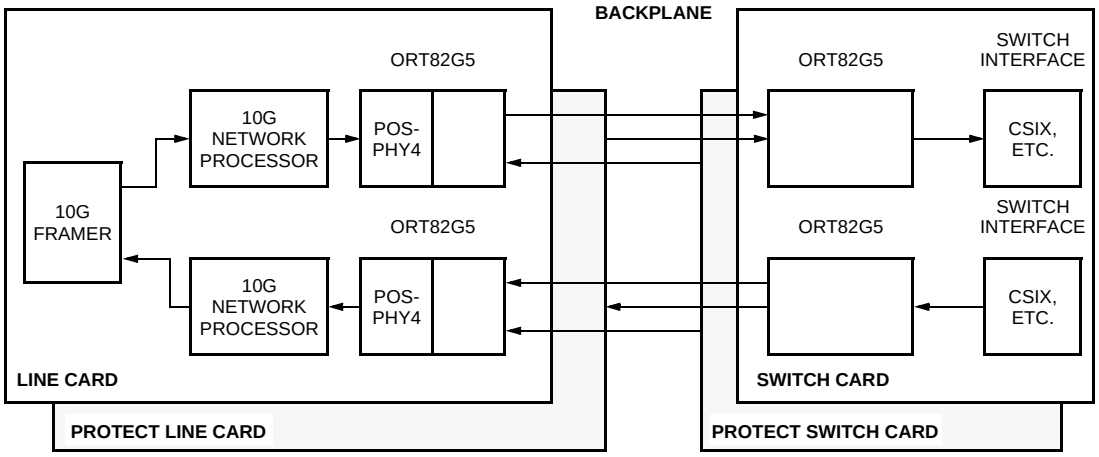
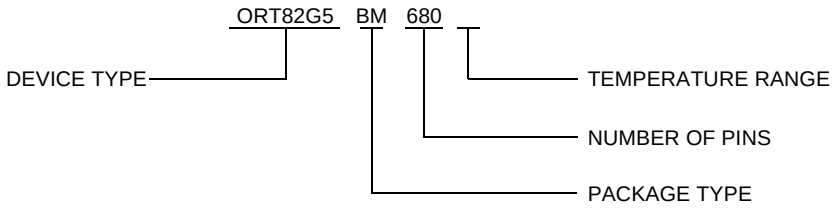


Figure 3. 10 Gbits/s Application with Protection

Ordering Information



5-6435.n(F)

Table 2. Device Options

Device	Parameter	Value
ORT82G5	Voltage	1.5 V core 3.3 V/2.5 V/1.8 V/1.5 V I/O
	Package	680-pin PBGAM

Table 3. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to 85 °C

Table 4. Package Type Options

Symbol	Description
BM	Plastic Ball Grid Array, Multilayer

Software Ordering Information

Implementing a design in an ORT82G5 requires the *ORCA* Foundry Development System and an ORT82G5 FPSC Design Kit. For ordering information, please visit:

http://www.lucent.com/micro/netcom/ipkits

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