Product Brief
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microelectronics group

Lucent Technologies
Bell Labs Innovations

ORCA® ORLI10G
10 Gbits/s Line Interface FPSC

Introduction

Lucent Technologies Microelectronics Group has developed a new *ORCA* Series 4 based FPSC, which combines a high-speed line interface with a flexible FPGA logic core. Built on the Series 4 reconfigurable embedded system-on-chips (SoC) architecture, the ORLI10G consists of an OIF standard (OIF 99.102.5) compliant XSBI 10 Gbits/s transmit and 10 Gbits/s receive line interface. Both transmit and receive interfaces consist of 16-bit LVDS data up to 667 Mbits/s, integrated transmit and receive programmable PLLs for data rate conversions between the line-side and system-side data rates, and a progammable logic interface at the system end for use with SONET/SDH, Ethernet, or OTN/digital wrapper with strong FEC system device data standards. In addition to the embedded functionality, the device will include up to 400k of usable FPGA gates. The line interface includes logic to divide the data rate down to 167 MHz or less (1/4 line rate) or 84 MHz or less (1/8 line rate) for transfer to the FPGA logic. The ORLI10G is designed to connect directly to Lucent's 10 Gbits/s TTRN0110G MUX and TRCV0110G deMUX on the line side as well as other industry standard devices. The programmable logic interface on the system side allows for direct connection to a 10 Gbits/s Ethernet MAC, a 10 Gbits/s SONET/SDH framer/data engine or a 10 Gbits/s digital wrapper/FEC framer/data engine.

For 10 Gbits/s Ethernet, the ORLI10G supports the physical coding sublayer (PCS), interfaces to the physical media attachment (PMA), and connects to the system interface (host or switch) for the proposed *IEEE* * 802.3ae 10 Gbits/s serial LAN PHY.

The ORLI10G FPSC is a high-speed programmable device for 10G/s data solutions. It can be used as the interface between the line interface and the system interface in a variety of emerging networks, including 10 Gbits/s SONET/SDH (OC-192/STM-48), 10 Gbits/s optical transport networks (OTN) using digital wrapper and strong FEC, or 10 Gbits/s Ethernet. Other functions include use in quad OC-48/STM-16 SONET/SDH systems, interfaces between quad OC-48/STM-16 and OC-192/STM-64 components, and use as a generic data transfer mechanism between two devices at 10 Gbits/s rates. Data is received at the line interface and then sent to either a 4-bit or 8-bit serial-to-parallel converter. On the transmit interface, either a 4-bit or 8-bit parallel-to-serial converter is used. Thus the data rate at the internal FPGA interface is either 1/4 or 1/8 the line rate.

The programmable PLLs on the ORLI10G provide for great flexibility in handling clock rate conversion due to differing amounts of overhead bits in various system data standards. For example, when used as a 10 Gbits/s Ethernet interface, the ORLI10G will automatically divide the line frequency of 645 MHz by 4 x 64/66 (receive side) to synchronize with the system frequency of 156 MHz. When the ORLI10G is used as an interface to a 10 Gbits/s digital wrapper/FEC framer/data engine, these same PLLs can divide the strong FEC standard line frequency of 667 MHz by 4 x 14/15 (receive side) to provide the 156 MHz system clock frequency. The ORLI10G can also divide down the STS-192/STM-64 SONET/SDH data line rate of 622 MHz by 4 to synchronize with a 155 MHz system clock. The ORLI10G can also be configured to provide a 78 MHz system data rate.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Table 1. *ORCA* ORLI10G—Available FPGA Logic

Device	PFU Rows	PFU Columns	Total PFUs	User I/Os	LUTs	EBR Blocks	EBR Bits (k)	Usable Gates (k)
ORLI10G	36	36	1296	432	10368	12	111	380—800

† The embedded core and interface are not included in the above gate counts. The usable gate counts range from a logic-only gate count to a gate count assuming 20% of the PFUs/SLICs being used as RAMs. The logic-only gate count includes each PFU/SLIC (counted as 108 gates/PFU), including 12 gates per LUT/FF pair (eight per PFU), and 12 gates per SLIC/FF pair (one per PFU). Each of the four PIO groups are counted as 16 gates (three FFs, fast-capture latch, output logic, CLK, and I/O buffers). PFUs used as RAM are counted at four gates per bit, with each PFU capable of implementing a 32 x 4 RAM (or 512 gates) per PFU. Embedded block RAM (EBR) is counted as four gates per bit plus each block has an additional 25k gates. 7k gates are used for each PLL and 50k gates for the embedded system bus and microprocessor interface logic. Both the EBR and PLLs are conservatively utilized in the gate count calculations.

Embedded Function Features

- Provides a 10 Gbits/s line interface-to-interface with various system standards such as OC-192/STM-64 SONET/SDH, Quad OC-48/STM-16 10 Gbits/s Ethernet and, 10 Gbits/s OTN (digital wrapper/strong FEC).
- Embedded PLLs with programmable M/N multiplication/division values provide for flexible data rate conversion between line side and system side.
- Line-side provides for 16-bit LVDS data with multiple line frequencies supported up to 667 MHz depending on system standard.
- Line-side interface, including timing and jitter specifications, compliant to OIF 99.102.5 standard.
- Receive side interface can be split into four separate asynchronous 2.5 Gbits/s interfaces (4-bit LVDS data interface for each) with a separate clock for each for transfer to the FPGA logic.
- Data and clock rates divided by 4 or 8 for use in FPGA logic.
- Direct interface to Lucent's 10 Gbits/s MUX (TTRN0110G) and deMUX (TRCV0110G).
- LVDS I/Os compliant with *EIA**-644, support hot insertion. All embedded LVDS I/Os include both input and output on-board termination to allow high speed operation.
- Low-power LVDS buffers.
- Built-in boundry scan (*IEEE* 1149.1 JTAG).

Intellectual Property Features

Programmable logic provides a variety of yet-to-be standardized interface functions, including the following IP core functions:

- 10 Gbits/s Ethernet as defined by *IEEE* 802.3ae:
  - — XGMII for interfacing to 10 Gbits/s Ethernet MACs. XGMII is a 156 MHz double data rate parallel short-reach (typically less than 2 inches) interconnect interface.
  - — Elastic store buffers for clock domain transfer to/from the XGMII interface.
  - — $X^{59} + X^{19} + X^{1}$ scrambler/descrambler for 10 Gbits/s Ethernet.
  - — 66-bit word aligner and 64-bit/66-bit receive path decoder, 64-bit/66-bit transmit path encoder, and 66-bit/64-bit transmit path conversion for Ethernet overhead bits.
  - — 10 Gbits/s media access controller (MAC) available in a separate FPGA or ASIC.
- POS-PHY4 interface for 10 Gbits/s SONET/SDH and OTN systems and some 10 Gbits/s Ethernet systems.
- Quad 2.5 Gbits/s SONET/SDH to 10 Gbits/s SONET/SDH MUX/deMUX functions.

Programmable Features

- High-performance programmable logic:
  - — 0.13 µm 7-level metal technology.
  - — Internal performance of >250 MHz.
  - — 400k usable system gates.
  - — Meets multiple I/O interface standards.
  - — 1.5 V operation (30% less power than 1.8 V operation) translates to greater performance.
- Traditional I/O selections:
  - — LVTTL and LVCMOS (3.3 V, 2.5 V, and 1.8 V) I/Os.
  - — Per pin-selectable I/O clamping diodes provide 3.3 V PCI compliance.
  - — Individually programmable drive capability: 24 mA sink/12 mA source, 12 mA sink/6 mA source, or 6 mA sink/3 mA source.
  - — Two slew rates supported (fast & slew-limited).
  - — Fast-capture input latch and input flip-flop (FF) latch for reduced input setup time and zero hold time.
  - — Fast open-drain drive capability.
  - — Capability to register 3-state enable signal.
  - — Off-chip clock drive capability.
  - — Two input function generator in output path.
- New programmable high-speed I/O:
  - — Single-ended: GTL, GTL+, PECL, SSTL3/2 (class I & II), HSTL (Class I, III, IV), ZBT, and DDR.
  - — Double-ended—LVDS, bused-LVDS, LVPECL.
  - — Customer defined—ability to substitute arbitrary standard cell I/O to meet fast moving standards.
- New capability to (de)multiplex I/O signals:
  - — New DDR on both input and output at rates of up to 311 MHz (622 MHz effective rate).
  - — New 2x and 4x downlink and uplink capability per I/O (i.e., 50 MHz internal to 200 MHz I/O).

* *EIA* is a registered trademark of Electronic Industries Association.

Programmable Features (continued)

- Enhanced twin-quad programmable function unit (PFU):
  - — Eight 16-bit look-up tables (LUTs) per PFU.
  - — Nine user registers per PFU, one following each LUT, and organized to allow two nibbles to act independently, plus one extra for arithmetic operations.
  - — New register control in each PFU has two independent programmable clocks, clock enables, local set/reset, and data selects.
  - — New LUT structure allows flexible combinations of LUT4, LUT5, new LUT6, 4 → 1 MUX, new 8 → 1 MUX, and ripple mode arithmetic functions in the same PFU.
  - — 32 x 4 RAM per PFU, configurable as single- or dual-port. Create large, fast RAM/ROM blocks (128 x 8 in only eight PFUs) using the SLIC decoders as bank drivers.
  - — Soft-wired LUTs (SWL) allow fast cascading of up to three levels of LUT logic in a single PFU through fast internal routing which reduces routing congestion and improves speed.
  - — Flexible fast access to PFU inputs from routing.
  - — Fast-carry logic and routing to all four adjacent PFUs for nibble-wide, byte-wide, or longer arithmetic functions, with the option to register the PFU carry-out.
- Abundant high-speed buffered and nonbuffered routing resources provide 2x average speed improvements over previous architectures.
- Hierarchical routing optimized for both local and global routing with dedicated routing resources. This results in faster routing times with predictable and efficient performance.
- SLIC provides eight 3-statable buffers, up to a 10-bit decoder, and *PAL**-like and-or-invert (AOI) in each programmable logic cell.
- New cycle stealing capability allows a typical 15% to 40% internal speed imporvement after final place and route. This feature also allows many I/O specifications to be met for setup/hold and clock-to-out times. It may also reduce ground bounce effects for output buses by allowing flexible delays in switching output buffers.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provides optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 200 MHz.
- New 200 MHz embedded quad-port RAM blocks, 2 read ports, 2 write ports, and 2 sets of byte lane enables. Each embedded RAM block can be configured as:
  - — 1—512 x 18 (quad-port, two read/two write) with optional built in arbitration.
  - — 1—256 x 36 (dual-port, one read/one write).
  - — 1—1k x 9 (dual-port, one read/one write).
  - — 2—512 x 9 (dual-port, one read/one write for each).
  - — 2 RAMS with arbitrary number of words whose sum is 512 or less by 18 (dual-port, one read/one write).
  - — Supports joining of RAM blocks.
  - — Two 16 x 8-bit content addressable memory (CAM) support.
  - — FIFO 512 x 18, 256 x 36, 1k x 9, or dual 512 x 9.
  - — Constant multiply (8 x 16 or 16 x 8).
  - — Dual variable multiply (8 x 8).
- Embedded 32-bit internal system bus plus 4-bit parity interconnects FPGA logic, microprocessor interface (MPI), embedded RAM blocks, and embedded standard cell blocks with 100 MHz bus performance. Included are built-in system registers that act as the control and status center for the device.
- Built-in testability:
  - — Full boundary scan (*IEEE* 1149.1 and draft 1149.2 JTAG).
  - — Programming and readback through boundary scan port compliant to *IEEE* draft 1532:D1.7.
  - — TS_ALL testability function to 3-state all I/O pins.
  - — New temperature-sensing diode.
- Improved built-in clock management with programmable phase-locked loops (PPLLs) provides optimum clock modification and conditioning for phase, frequency, and duty cycle from 20 MHz up to 420 MHz.
- New cycle stealing capability allows a typical 15% to 40% internal speed improvement after final place and route. This feature also enables compliance with many setup/hold and clock-to-out I/O specifications and may provide reduced ground bounce from output buses by allowing flexible delays of switching output buffers.

* *PAL* is a trademark of Advanced Micro Devices, Inc.

Programmable Logic System Features

- PCI local bus compliant for FPGA I/Os.
- Improved *PowerPC**860 and *PowerPC* II high-speed synchronous microprocessor interface can be used for configuration, readback, device control, and device status, as well as for a general-purpose interface to the FPGA logic, RAMs, and embedded standard cell blocks. Glueless interface to synchronous *PowerPC* processors with user-configurable address space provided.
- New embedded *AMBA*† specification 2.0 AHB system bus (*ARM* † processor) facilitates communication among the microprocessor interface, configuration logic, embedded block RAM, FPGA logic, and embedded standard-cell blocks.
- New network PLLs meet ITU-T G.811 specifications and provide clock conditioning for DS-1/E-1 and STS-3/STM-1 applications.
- Flexible general-purpose PPLLs offer clock multiply (up to 8x), divide (down to 1/8x), phase shift, delay compensation, and duty cycle adjustment combined.
- Variable-size bused readback of configuration data capability with the built-in microprocessor interface and system bus.
- Internal, 3-state, and bidirectional buses with simple control provided by the SLIC.
- New clock routing structures for global and local clocking significantly increases speed and reduces skew (<200 ps for OR4E4).
- New local clock routing structures allow creation of localized clock trees.
- New double-data rate (DDR) and zero-bus turnaround (ZBT) memory interfaces support the latest high-speed memory interfaces.
- New 2x/4x uplink and downlink I/O capabilities interface high-speed external I/Os to reduced speed internal logic.
- *ORCA* Foundry 2000 development system software. Supported by industry-standard.
- CAE tools for design entry, synthesis, simulation, and timing analysis.
- Meets universal test and operations PHY interface for ATM (UTOPIA) levels 1, 2, and 3 as well as POS-PHY3. Also meets proposed specifications for UTOPIA Level 4 and POS-PHY4 for 10 Gbits/s interfaces.
- Meets POS-PHY3 (2.5 Gbits/s) and POS-PHY4 (10 Gbits/s) interface standards for packet-over-SONET as defined by the Saturn Group.
- Two new edge clock routing structures allow up to seven high-speed clocks on each edge of the device for improved setup/hold and clock to out performance.

* *PowerPC* is a registered trademark of International Business Machines, Inc.
† *AMBA* is a trademark, and *ARM* is a registered trademark of Advanced RISC Machines Limited.

Block Diagram

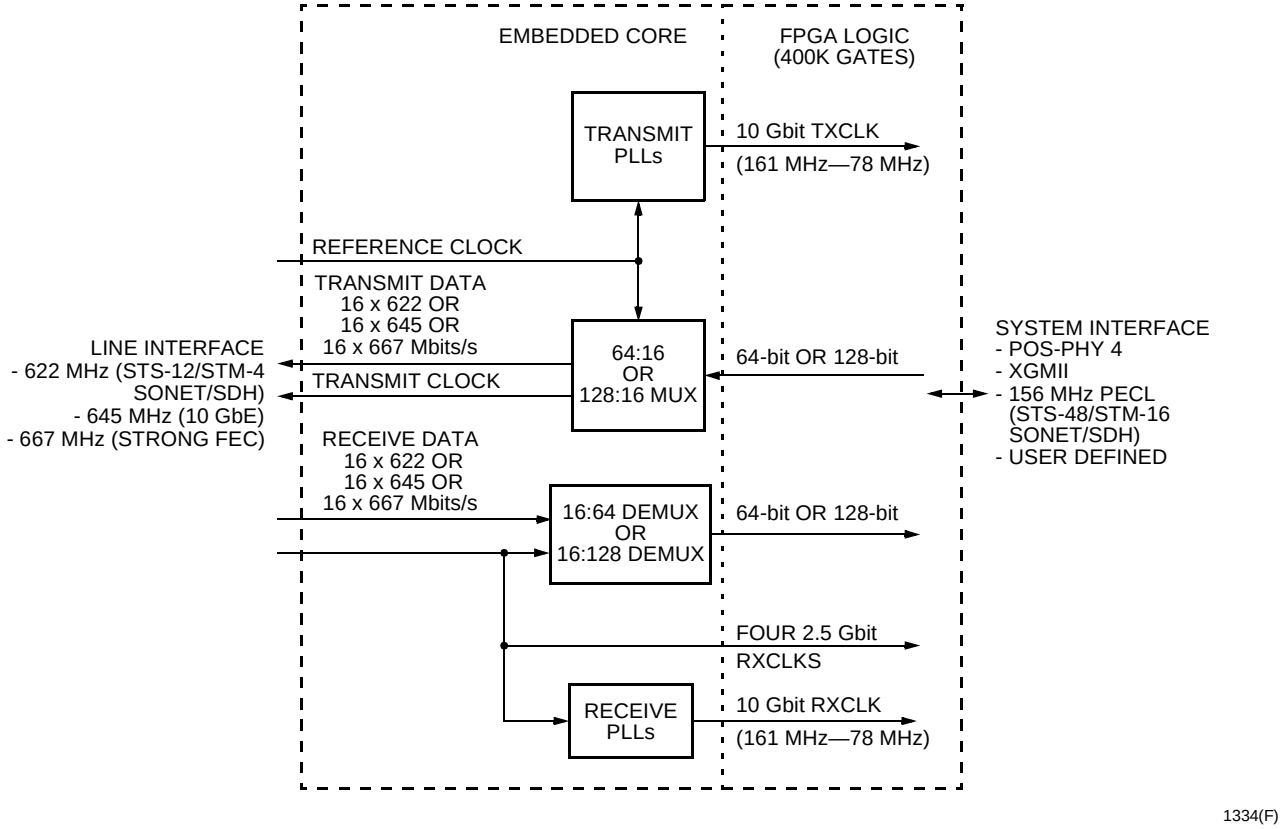

Figure 1. ORLI10G Block Diagram

System Diagram

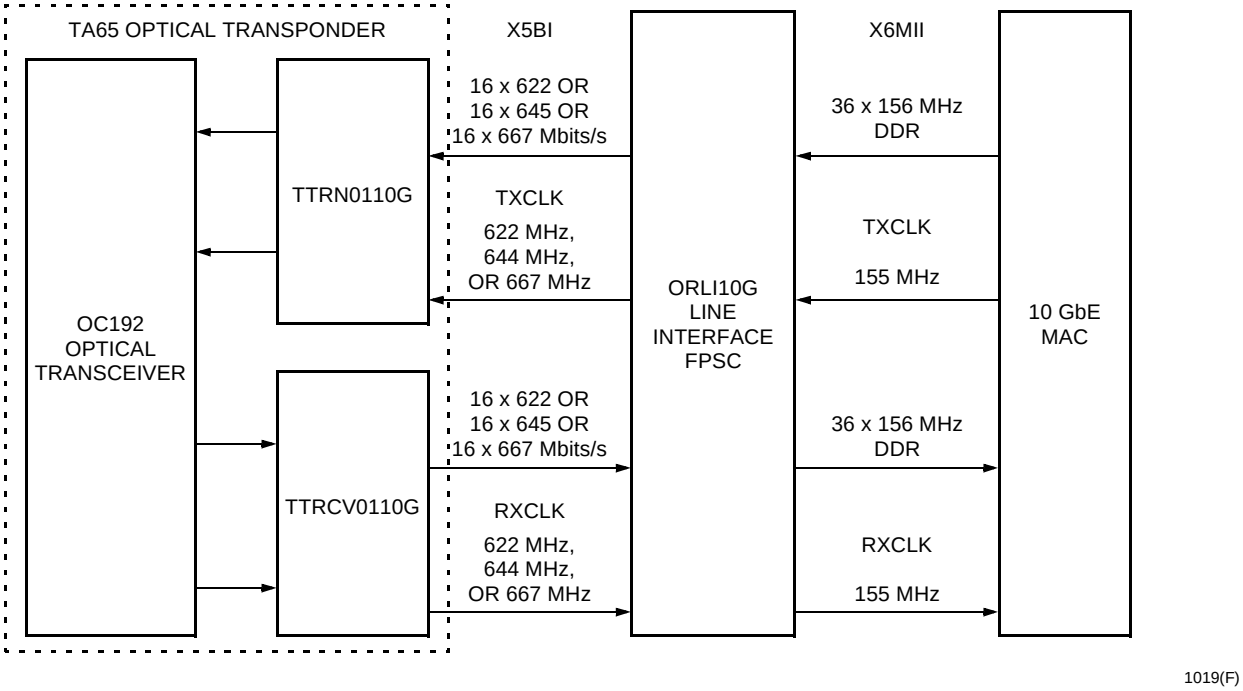

Figure 2. ORLI10G Application Example (10 Gbits/s Ethernet)

Hardware Ordering Information

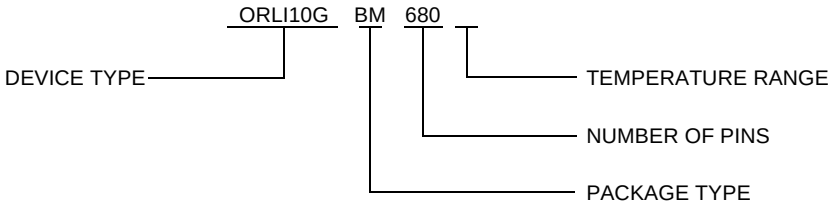

Table 2. Device Type Options

Device	Parameter	Value
ORLI10G	Voltage	1.5 V core 3.3 V/2.5 V I/O
	Package	416-pin PBGAM (BM416) 680-pin PBGAM (BM680)

Table 3. Temperature Options

Symbol	Description	Temperature
(Blank)	Commercial	0 °C to 70 °C
I	Industrial	–40 °C to +85 °C

Table 4. Package Type Options

Symbol	Description
BM	Plastic Ball Grid Array, Multilayer

Table 5*. ORCA* FPSC Package Matrix (Speed Grades)

Device	Package	
	416-Pin PBGAM	**680-Pin PBGAM**
	BM416	**BM680**
ORLI10G	–1	–1

Software Ordering Information

Implementing a design in an ORLI10G requires the *ORCA* Foundry Development System and an ORLI10G FPSC Desgin Kit. For ordering information, please visit:

http://www.lucent.com/micro/netcom/ipkits/orli10g/

For additional information, contact your Microelectronics Group Account Manager or the following:
INTERNET: **http://www.lucent.com/micro**, or for FPGA information, **http://www.lucent.com/orca**
E-MAIL: **docmaster@micro.lucent.com**
N. AMERICA: Microelectronics Group, Lucent Technologies Inc., 555 Union Boulevard, Room 30L-15P-BA, Allentown, PA 18109-3286
1-800-372-2447, FAX 610-712-4106 (In CANADA: **1-800-553-2448**, FAX 610-712-4106)
ASIA PACIFIC: Microelectronics Group, Lucent Technologies Singapore Pte. Ltd., 77 Science Park Drive, #03-18 Cintech III, Singapore 118256
Tel. (65) 778 8833, FAX (65) 777 7495
CHINA: Microelectronics Group, Lucent Technologies (China) Co., Ltd., A-F2, 23/F, Zao Fong Universe Building, 1800 Zhong Shan Xi Road, Shanghai 200233 P. R. China **Tel. (86) 21 6440 0468**, **ext. 325**, FAX (86) 21 6440 0652
JAPAN: Microelectronics Group, Lucent Technologies Japan Ltd., 7-18, Higashi-Gotanda 2-chome, Shinagawa-ku, Tokyo 141, Japan
Tel. (81) 3 5421 1600, FAX (81) 3 5421 1700
EUROPE: Data Requests: MICROELECTRONICS GROUP DATALINE: **Tel. (44) 7000 582 368**, FAX (44) 1189 328 148
Technical Inquiries: GERMANY: **(49) 89 95086 0** (Munich), UNITED KINGDOM: **(44) 1344 865 900** (Ascot),
FRANCE: **(33) 1 40 83 68 00** (Paris), SWEDEN: **(46) 8 594 607 00** (Stockholm), FINLAND: **(358) 9 3507670** (Helsinki),
ITALY: **(39) 02 6608131** (Milan), SPAIN: **(34) 1 807 1441** (Madrid)

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