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NTE859/NTE859SM
Integrated Circuit
Quad, Low Noise, JFET Input
Operational Amplifier

Description:

The NTE859 (14–Lead DIP) and NTE859SM (SOIC–14 Surface Mount) JFET–input operational amplifiers are low noise amplifiers with low noise input bias, offset currents, and fast slew rate. The low harmonic distortion and low noise make these devices ideally suited as amplifiers for high–fidelity and audio preamplifier applications. Each amplifier features JFET–inputs (for high input impedance) coupled with bipolar output stages all integrated on a single monolithic chip.

Features:

- Low Power Consumption
- Wide Common–Mode and Differential Voltage Ranges
- Low Input Bias and Offset Currents
- Output Short–Circuit Protection
- Low Total Harmonic Distortion: 0.003% Typ
- Low Noise: Vn = 18nV$\sqrt{H_Z}$ Typ
- High Input Impedance: JFET–Input Stage
- Internal Frequency Compensation
- Latch–Up Free Operation
- High Slew Rate: 13V/μs Typ

Absolute Maximum Ratings: (T_A = 0 to +70°C unless otherwise specified)

Supply Voltage (Note 1), V_{CC}(+) 18V
Supply Voltage (Note1), V_{CC}(–) . . . . . –18V
Differential Input Voltage (Note 2), V_{ID} . . . . . ±30V
Input Voltage Range (Note 1, Note 3),V_{IDR} . . . . . ±15V
Duration of Output Short Circuit (Note 4),t_S . . . . . Unlimited
Power Dissipation (T_A = +25°C), P_D 680mW
Derate Above 25°C . . . . . 10mW/°C
Operating Ambient Temperature Range, T_A . . . . . 0° to +70°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 1/16” from Case for 10sec), T_L . . . . . +260°C

Note 1. All voltage values, except differential voltages, are with reapect to the midpoint between V_{CC}(+) and V_{CC}(–).
Note 2. Differential voltages are at the non–inverting input pin with respect to the inverting pin.
Note 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15V, whichever is less.
Note 4. The output may be shorted to GND or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

Electrical Characteristics: (V_{CC} = ±15V, T_A = 0 to+70°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	V_O = 0, R_S = 50Ω	T_A = +25°C	–	3	10	mV
				–	–	13	mV
Temperature Coefficient of Input Offset Voltage	αV_{IO}	V_O = 0, R_S = 50Ω		–	10	–	µV/°C
Input Offset Current	I_{IO}	V_O = 0, Note 6	T_A = +25°C	–	5	100	pA
				–	–	2	nA
Input Bias Current	I_{IB}	V_O = 0, Note 6	T_A = +25°C	–	30	200	pA
				–	–	7	nA
Common–Mode Input Voltage Range	V_{ICR}	T_A = +25°C		±11	±12	–	V
Maximum Peak Output Voltage Range	V_{OM}	R_L = 10kΩ, T_A = +25°C		±12	±13.5	–	V
		R_L = ≥10kΩ		±12	–	–	V
		R_L = ≥2kΩ		±10	±12	–	V
Large–Signal Differential Voltage Amplification	A_{VD}	V_O = ±10V, R_L ≥ 2kΩ	T_A = +25°C	25	200	–	V/mV
				15	–	–	V/mV
Unity–Gain Bandwidth	B_1	T_A = +25°C		–	3	–	MHz
Input Resistance	r_i	T_A = +25°C		–	10^{12}	–	Ω
Common–Mode Rejection Ratio	CMRR	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50Ω, T_A = +25°C		70	86	–	dB
SupplyVoltage Rejection Ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	k_{SVR}	V_{CC} = ±15V to ±9V, V_O = 0, R_S = 50Ω, T_A = +25°C		70	86	–	dB
Supply Current (Per Amplifier)	I_{CC}	No Load, V_O = 0, T_A = +25°C		–	1.4	2.5	mA
Crosstalk Attenuation	V_{o1}/V_{o2}	A_{VD} = 100, T_A = +25°C		–	120	–	dB

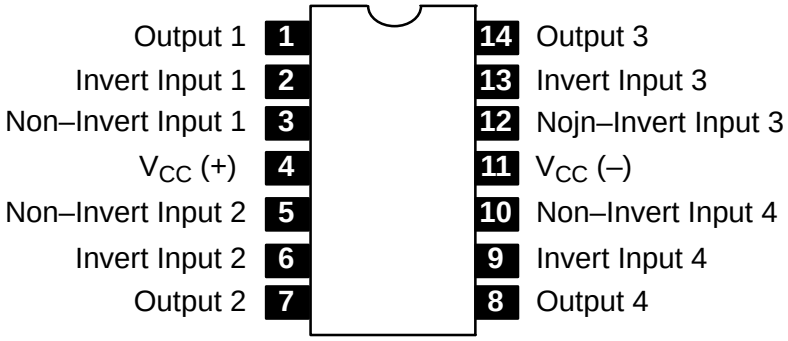
Note 5. All characteristics are measured under open–loop conditions with zero common–mode voltage unless otherwise specified.

Note 6. Input bias currents of a FET–input operational amplifier are normal junction reverse currents, which are temperature sensitive. Pulse techniques must be used that will maintain the junction temperatures as close to the ambient temperature as is possible.

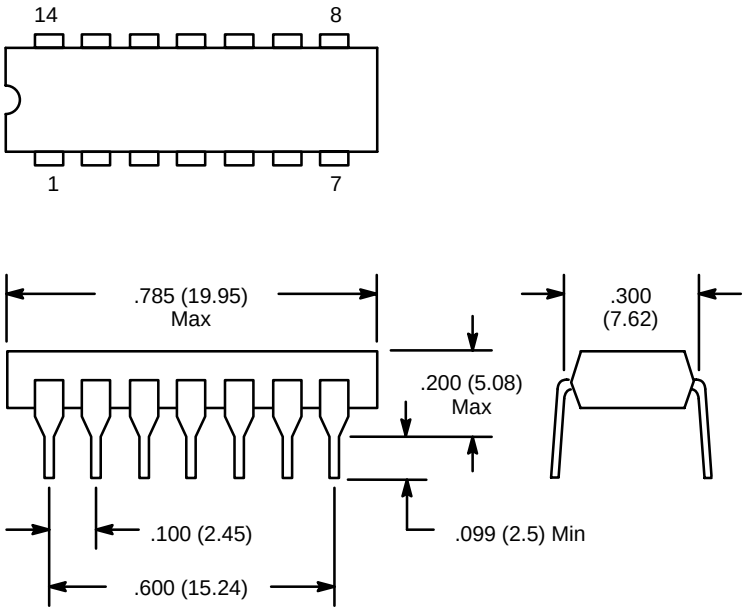
Operating Characteristics: (V_{CC} = ±15V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Slew Rate at Unity Gain	SR	V_I = 10V, R_L = 2kΩ, C_L = 100pF		8	13	–	V/µs
Rise Time Overshoot Factor	t_r	V_I = 10V, R_L = 2kΩ, C_L = 100pF		–	0.1	–	µs
				–	10	–	%
Equivalent Input Noise Voltage	V_n	R_S = 100Ω	f = 1kHz	–	18	–	nV/√Hz
			f = 10Hz to 10kHz	–	4	–	µV
Equivalent Input Noise Current	I_n	R_S = 100Ω, f = 1kHz		–	0.01	–	pA/√Hz
Total Harmonic Distortion	THD	$V_{O(rms)}$= 10V, R_S ≤ 1kΩ, R_L ≥ 2kΩ, f = 1kHz		–	0.003	–	%

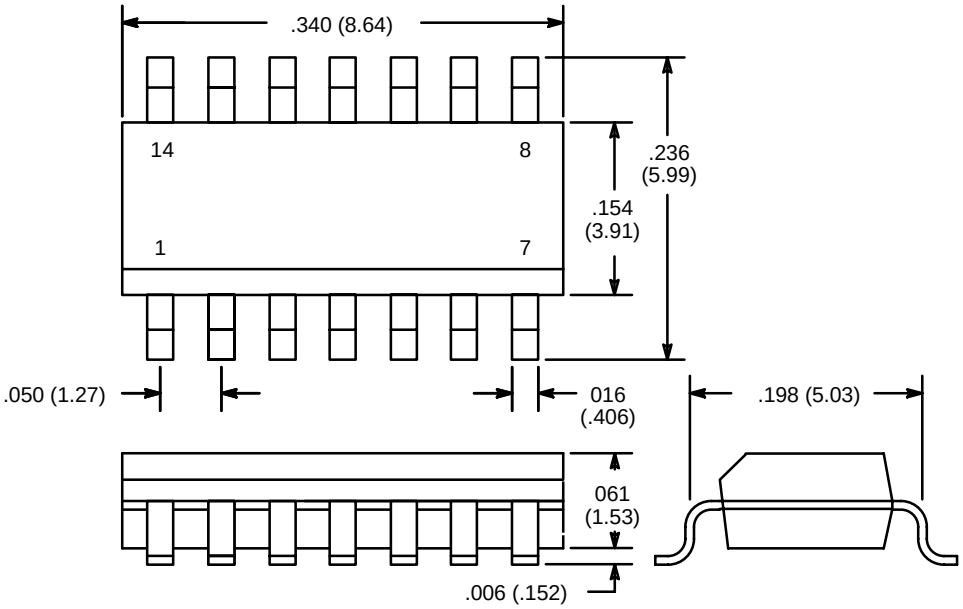
Pin Connection Diagram



NTE859 (14–Lead DIP)



NTE859SM (SOIC–14)



NOTE: Pin1 on Beveled Edge