**NT56V6650C0T (16Mx4)**

*64Mb Synchronous DRAM*
*Data Sheet*

## Revision Log

| Rev Date | Version | Content of Modification |
|----------|---------|-------------------------|
| Sep / 1999 | 1.0 | 1 st  Revision |
| June / 2000 | 1.1 | Added speed grade –75B (PC133@CL3 & PC100@CL2) to following items as : <br> 1. Product Family <br> 2. DC currents <br> 3. AC Timing Parameters |

# Contents

# NT56V6650C0T

**64Mb : x4**
**PC133 / PC100 Synchronous DRAM**

## Description

The NT56V6650C0T is four-bank Synchronous DRAMs organized as 4Mbit x 4 I/O x 4 Bank . The devices achieve high-speed data transfer rates of up to 133MHz by employing a pipeline chip architecture that synchronizes the output data to a system clock. The chip is fabricated with NANYA advanced 64Mbit single transistor CMOS DRAM process technology.

The device is designed to comply with all JEDEC standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, and data input/output (I/O or DQ) circuits are synchronized with the positive edge of an externally supplied clock. /RAS, /CAS, /WE, and /CS are pulsed signals which are examined at the positive edge of each externally applied clock (CLK). Internal chip operating modes are defined by combinations of these signals and a command decoder initiates the necessary timings for each operation. A fourteen bit address bus accepts address data in the conventional /RAS /CAS multiplexing style. Twelve row addresses (A0-A11) and two bank select addresses (A12, A13) are strobed with /RAS. Ten column addresses (A0-A9) plus bank select addresses and A10 are strobed with /CAS.

Prior to any access operation, the /CAS latency, burst length, and burst sequence must be programmed into the device by address inputs A0-A9 during a mode register set cycle. In addition, it is possible to program a multiple burst sequence with single write cycle for write through cache operation.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 133MHz is possible depending on burst length, /CAS latency, and speed grade of the device. Simultaneous operation of both decks of a stacked device is allowed, depending on the operation being done. Auto Refresh (CBR), Self Refresh, and Low Power operation are supported.

## Feature

- JEDEC standard 3.3V± 0.3V Power Supply
- LVTTL compatible inputs and outputs
- Four Banks controlled by Bank Selects(A12/A13)
- Single Pulsed /RAS Interface
- Fully Synchronous to Positive Clock Edge
- MRS cycle with address key programmability for :
  - CAS Latency ( 2, 3 )
  - Burst Length ( 1, 2, 4, 8 & Full-page )
  - Burst Type ( Sequential or Interleave )
- Multiple Burst Read with Single Write Option
- Automatic and Controlled Precharge Command
- Data Mask for Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Suspend Mode and Power Down Mode
- Standard Power operation
- 4096 refresh cycles/64ms
- Random Column Address every CLK (1-N Rule)
- Package:54-pin 400 mil TSOP-Type II

## Product Family

| Part NO. | Organization | Speed（MHz@CL-tRP-tRCD) | | Interface | Package |
|---|---|---|---|---|---|
| NT56V6650C0T-7 | | 143 MHz @ 3-3-3 | - | | |
| NT56V6650C0T-75B | | 133 MHz @ 3-3-3 | 100 MHz @ 2-2-2 | | |
| NT56V6650C0T-75 | 16M x 4 | 133 MHz @ 3-3-3 | - | LVTTL | 54pin TSOP II |
| NT56V6650C0T-8A | | 125 MHz @ 3-3-3 | 100MHZ @ 2-2-2 | | |
| NT56V6650C0T-8B | | 125 MHz @ 3-3-3 | 100MHz @ 3-2-2 | | |

## Pin Assignment ( Top View )

**16M x 4**

| Left | Pin | Pin | Right |
|---|---|---|---|
| $V_{DD}$ | 1 | 54 | $V_{SS}$ |
| NC | 2 | 53 | NC |
| $V_{DDQ}$ | 3 | 52 | $V_{SS\,Q}$ |
| NC | 4 | 51 | NC |
| DQ0 | 5 | 50 | DQ3 |
| $V_{SSQ}$ | 6 | 49 | $V_{DDQ}$ |
| NC | 7 | 48 | NC |
| NC | 8 | 47 | NC |
| $V_{DDQ}$ | 9 | 46 | $V_{SSQ}$ |
| NC | 10 | 45 | NC |
| DQ1 | 11 | 44 | DQ2 |
| $V_{SSQ}$ | 12 | 43 | $V_{DDQ}$ |
| NC | 13 | 42 | NC |
| $V_{DD}$ | 14 | 41 | $V_{SS}$ |
| NC | 15 | 40 | NC |
| $\overline{WE}$ | 16 | 39 | DQM |
| $\overline{CAS}$ | 17 | 38 | CLK |
| $\overline{RAS}$ | 18 | 37 | CKE |
| $\overline{CS}$ | 19 | 36 | NC |
| A13/BS0 | 20 | 35 | A11 |
| A12/BS1 | 21 | 34 | A9 |
| A10/AP | 22 | 33 | A8 |
| A0 | 23 | 32 | A7 |
| A1 | 24 | 31 | A6 |
| A2 | 25 | 30 | A5 |
| A3 | 26 | 29 | A4 |
| $V_{DD}$ | 27 | 28 | $V_{SS}$ |
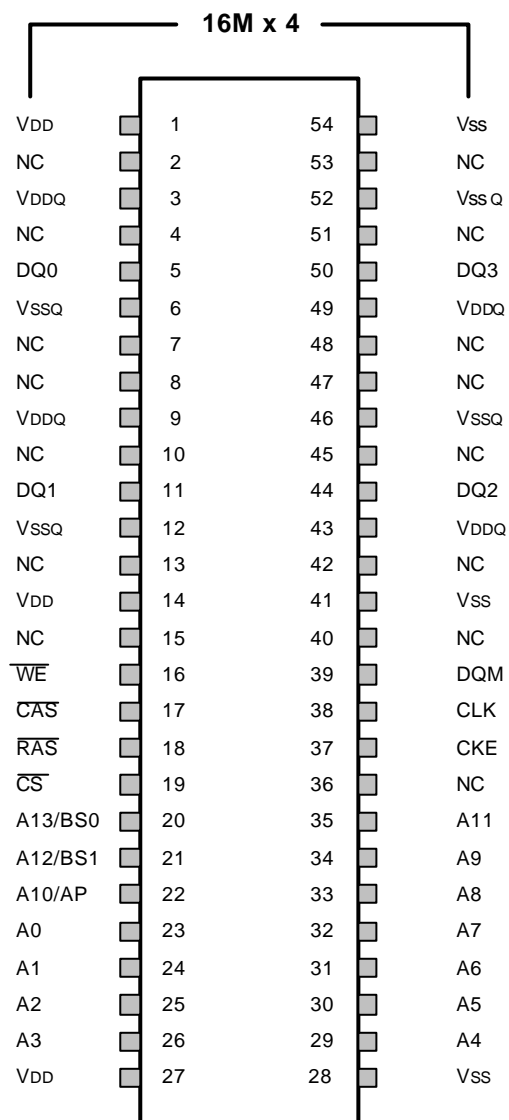
**54-pin Plastic TSOP-II 400 mil**

## Pin Description

| CLK | Clock Input | DQ0-DQ15 | Data Input/Output |
|---|---|---|---|
| CKE | Clock Enable | DQM, LDQM, UDQM | Data Mask |
| /CS (/CS0, /CS1 ) | Chip Select | VDD | Power (+3.3V) |
| /RAS | Row Address Strobe | VSS | Ground |
| /CAS | Column Address Strobe | VDDQ | Power for DQs (+3.3V) |
| /WE | Write Enable | VSSQ | Ground for DQs |
| BS1, BS0 (A12, A13) | Bank Select | NC | No Connection |
| A0-A11 | Address Inputs | -- | -- |

## Input / Output Functional Description
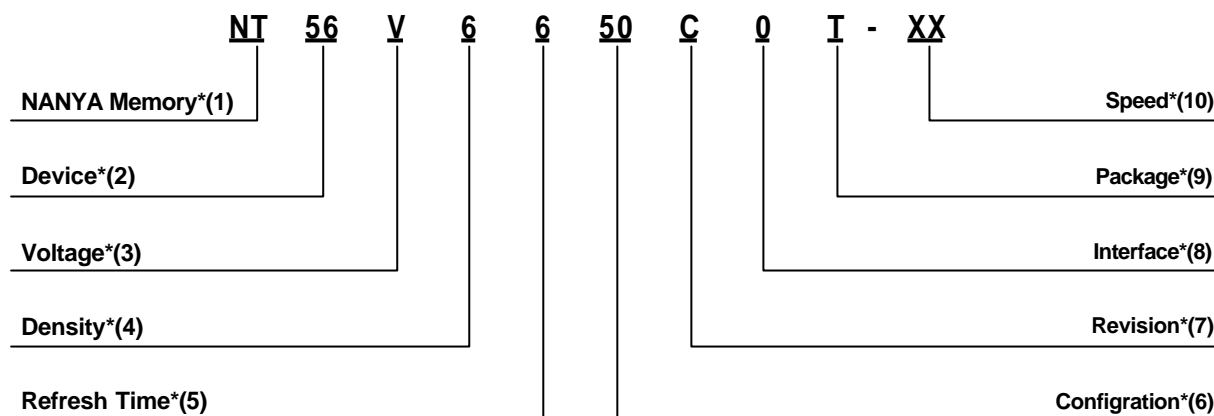
| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CLK | Input | Positive Edge | The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock. |
| CKE | Input | Active High | Activates the CLK signal when high and deactivates the CLK signal when low. By deactivating the clock, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode. |
| /CS, /CS0, /CS1 | Input | Active Low | /CS ( /CS0 , /CS1 for stacked devices) enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| /RAS, /CAS /WE | Input | Active Low | When sampled at the positive rising edge of the clock, /CAS, /RAS, and /WE define the operation to be executed by the SDRAM. |
| BS1, BS0 (A12, A13) | Input | -- | Selects which bank is to be active. |
| A0 - A11 | Input | -- | During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. A10 is used to invoke auto-precharge operation at the end of the burst read or write cycle. If A10 is high, auto-precharge is selected and BS0, BS1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10 is used in conjunction with BS0, BS1 to control which bank(s) to precharge. If A10 is high, all banks will be precharged regardless of the state of BS. If A10 is low, then BS0 and BS1 are used to define which bank to precharge. |
| DQ0-DQ3 | Input-Output | -- | Data Input/Output pins operate in the same manner as on conventional DRAMs |
| DQM | Input | Active High | The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. DQM low turns the output buffers on and DQM high turns them off. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. |
| VDD, VSS | Supply | -- | Power and ground for the input buffers and the core logic. |
| VDDQ, VSSQ | Supply | -- | Isolated power supply and ground for the output buffers to provide improved noise immunity. |

## Functional Block Diagram
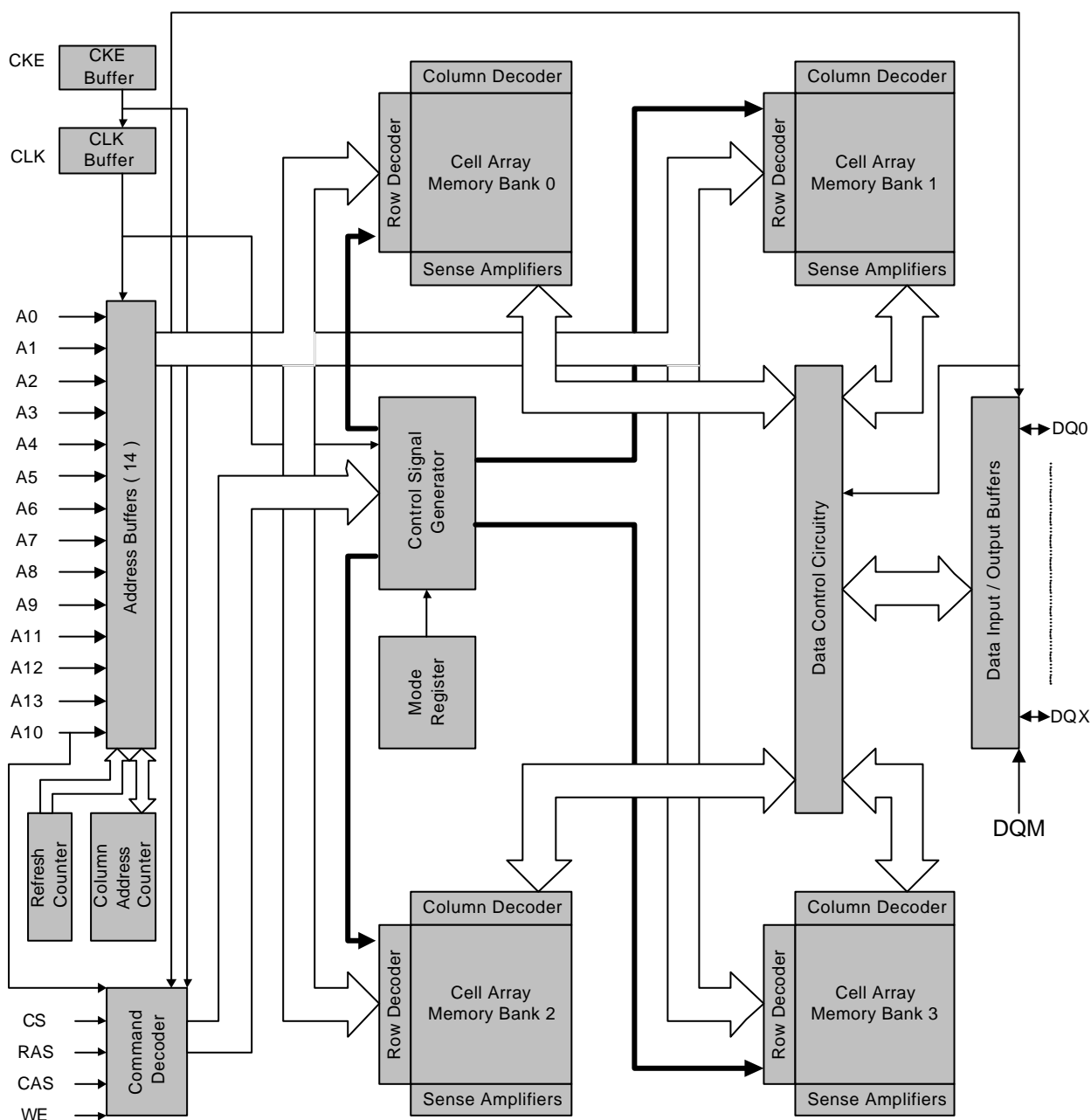


Cell Array , per bank , for 4Mb x 4 DQ   : 4096 Row x 1024Col x 4DQ (DQ0-DQ3  ).

## Part Number Guide

```
        NT   56   V   6   6   50   C   0   T  -  XX
```

NANYA Memory*(1)                          Speed*(10)

Device*(2)                               Package*(9)

Voltage*(3)                              Interface*(8)

Density*(4)                              Revision*(7)

Refresh Time*(5)                         Configuration*(6)

**(1) NANYA Memory**

**(2) Device**
   56 - - - - - - - - SDRAM

**(3) Voltage**
   V - - - - - - - - 3.3V

**(4) Density**
   1 - - - - - - - - 16M
   6 - - - - - - - - 64M
   2 - - - - - - - - 128M

**(5) Refresh Time**
   7 - - - - - - - - 2K/32ms
   6 - - - - - - - - 4K/64ms

**(6) Configuration**
   10 - - - - - - - - 4 bank, x 8
   20 - - - - - - - - 4 bank, x 16
   50 - - - - - - - - 4 bank, x 4

**(7) Revision**
   A - - - - - - - - 1st version
   B - - - - - - - - 2nd version
   C - - - - - - - - 3rd version
   D - - - - - - - - 4th version

**(8) Interface**
   0 - - - - - - - - LVTTL
   1 - - - - - - - - SSTL

**(9) Package**
   T - - - - - - - -TSOP II
   F - - - - - - - -TQFP
   Q - - - - - - - -QFP

**(10) Speed**
   7 - - - - - - - -143MHz
   75 - - - - - - -133MHz
   8 - - - - - - - -125MHz
   10 - - - - - - -100MHz

## DC Characteristics

### Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage | -0.3 to +4.6 | V | 1 |
| $V_{DDQ}$ | Power Supply Voltage for Output | -0.3 to +4.6 | V | 1 |
| $V_{IN}$ | Input Voltage | -0.3 to $V_{DD}$+0.3 | V | 1 |
| $V_{OUT}$ | Output Voltage | -0.3 to $V_{DD}$+0.3 | V | 1 |
| $T_A$ | Operating Temperature (ambient) | 0 to +70 | ℃ | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +125 | ℃ | 1 |
| $P_D$ | Power Dissipation | 1.0 | W | 1 |
| $I_{OUT}$ | Short Circuit Output Current | 50 | mA | 1 |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended DC Operating Conditions ($T_A$ = 0 to 70 ℃ )

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Power Voltage | 3.0 | 3.3 | 3.6 | V | 1 |
| $V_{DDQ}$ | Power Voltage for Output | 3.0 | 3.3 | 3.6 | V | 1 |
| $V_{IH}$ | Input High Voltage | 2.0 | - | $V_{DD}$ + 0.3 | V | 1,2 |
| $V_{IL}$ | Input Low Voltage | -0.3 | - | 0.8 | V | 1,3 |

1. All voltages referenced to $V_{SS}$ and $V_{SSQ}$.
2. $V_{IH}$ (max) = $V_{DD}$ / $V_{DDQ}$ + 1.2V for pulse width ≤ 5ns
3. $V_{IL}$ (min) = $V_{SS}/V_{SSQ}$ - 1.2V for pulse width ≤ 5ns .

### Capacitance ($T_A$ = 25 ℃, f = 1MHz, VDD = 3.3V ± 0.3V)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Notes |
|---|---|---|---|---|---|---|
| $C_i$ | Input Capacitance (A0-A11, BS0, BS1, /CS, /RAS, /CAS, /WE, CKE, DQM) | 2.5 | 3.0 | 3.8 | pF | 1 |
| | Input Capacitance (CLK) | 2.5 | 2.8 | 3.5 | | |
| $C_O$ | Output Capacitance (DQ0 – DQ15) | 4.0 | 4.5 | 6.5 | | |

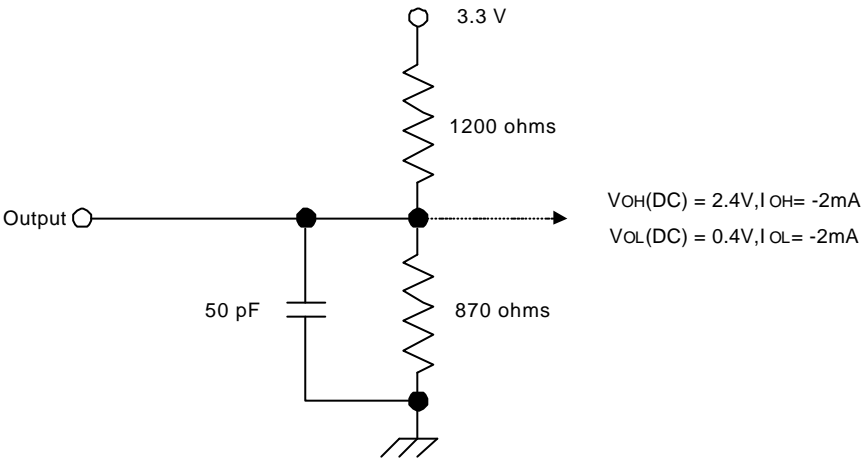1. Multiply given planar values by 2 for 2-High stacked device except /CS.

## DC Electrical Characteristics $(T_A = 0 \text{ to } +70\,°C\,, V_{DD} = 3.3V \pm 0.3V)$

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| $I_{I(L)}$ | Input Leakage Current, any input $(0.0V \le V_{IN} \le V_{DD})$, All Other Pins Not Under Test = 0V | -1 | +1 | uA | 1 |
| $I_{O(L)}$ | Output Leakage Current $(D_{OUT}$ is disabled, $0.0V \le V_{OUT} \le V_{DDQ})$ | -1 | +1 | uA | 1 |
| $V_{OH}$ | Output Level (LVTTL ) Output "H" Level Voltage $(I_{OUT} = -2.0mA)$ | 2.4 | - | V | - |
| $V_{OL}$ | Output Level (LVTTL ) Output "L" Level Voltage $(I_{OUT} = +2.0mA)$ | - | 0.4 | V | - |
| 1. Multiply given planar values by 2 for 2-High stacked device. | | | | | |

## DC Output Load Circuit



3.3 V

1200 ohms

Output

$V_{OH}(DC) = 2.4V, I_{OH} = -2mA$
$V_{OL}(DC) = 0.4V, I_{OL} = -2mA$

50 pF

870 ohms

## Operating, Standby, and Refresh Currents ($V_{DD}$ =3.3V $\pm$ 10% , $T_A$ =0°C to 70°C)

| Parameter | Symbol | Test condition | Version | | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| | | | - 7 | - 75(B) | - 8B | - 8A | | |
| Operating current | $I_{CC1}$ | 1 bank operation , $t_{RC}$ = $t_{RC}$(mim), $t_{CK}$ = min Active-Precharge Command cycling without burst operation | 75 | 75 | 70 | 70 | mA | 1,2,3 |
| Precharge standby current in power-down mode | $I_{CC2}P$ | CKE $\leq$ $V_{IL}$(max), $t_{CK}$ = min , /CS = $V_{IH}$(min), | 2 | | | | mA | 1 |
| | $I_{CC2}PS$ | CKE $\leq$ $V_{IL}$(max), $t_{CK}$ =$\infty$, /CS = $V_{IH}$(min) | 2 | | | | mA | 1 |
| Precharge standby current in non power-down mode | $I_{CC2}N$ | CKE $\geq$ $V_{IH}$(min), /CS = $V_{IH}$(min), $t_{CK}$ = min | 35 | 35 | 25 | 25 | mA | 1 |
| | $I_{CC2}NS$ | CKE $\geq$ $V_{IH}$(min), $t_{CK}$ =$\infty$ | 5 | | | | mA | 1,5 |
| No Operating current ( Active state : 4 bank) | $I_{CC3}P$ | CKE$\leq$$V_{IL}$(max), $t_{CK}$ =min | 3 | | | | mA | 1,7 |
| | $I_{CC3}N$ | CKE $\geq$$V_{IH}$(min), /CS = $V_{IH}$(min), $t_{CK}$ =min | 40 | 40 | 30 | 30 | mA | 1,5 |
| Operating current ( Burst mode ) | $I_{CC4}$ | $t_{CK}$ =min , Read/ Write command cycling, Multiple banks active, gapless data, BL=4 | 120 | 120 | 90 | 90 | mA | 1,6 |
| Auto(CBR) refresh current | $I_{CC5}$ | $t_{RC}$ = $t_{RC}$(min) ; $t_{CK}$ =min CBR command cycling | 145 | 145 | 140 | 140 | mA | 1,3,4 |
| Self refresh current | $I_{CC6}$ | CKE $\leq$ 0.2V | 1 | | | | mA | 1 |

1.  Currents given are valid for a single device. The total current for a stacked device depends on the operation being performed on the other deck.
2.  These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of $t_{CK}$ and $t_{RC}$. Input signals are changed up to three times during $t_{RC}$(min).
3.  The specified values are obtained with the output open.
4.  Input signals are changed once during $t_{CK}$(min).
5.  Input signals are changed once during three clock cycles.
6.  Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7.  Input signals are stable.

## AC Characteristics ($T_A$ = 0 to +70 °C , $V_{DD}$ = 3.3V ± 0.3V)

1.  An initial pause of 200ms,with DQM and CKE held high , is required after power-up. A precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation .
2.  The Transition time is measured between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$).
3.  In addition to meeting the transition rate specification, the clock and CKE must transit between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4.  Load Circuit  A : AC timing tests have $V_{IL}$ = 0.4 V and $V_{IH}$ = 2.4 V with the timing referenced to the 1.40V crossover point
5.  Load Circuit  A : AC measurement s assume $t_T$ = 1.0ns.
6.  Load Circuit B : AC timing tests have $V_{IL}$ = 0.8 V and $V_{IH}$ = 2.0 V with the timing referenced to the 1.40V crossover point
7.  Load Circuit B  : AC measurements assume $t_T$ = 1.2ns.

## AC Output Load Circuits



AC Output Load Circuit ( A )

AC Output Load Circuit ( B )
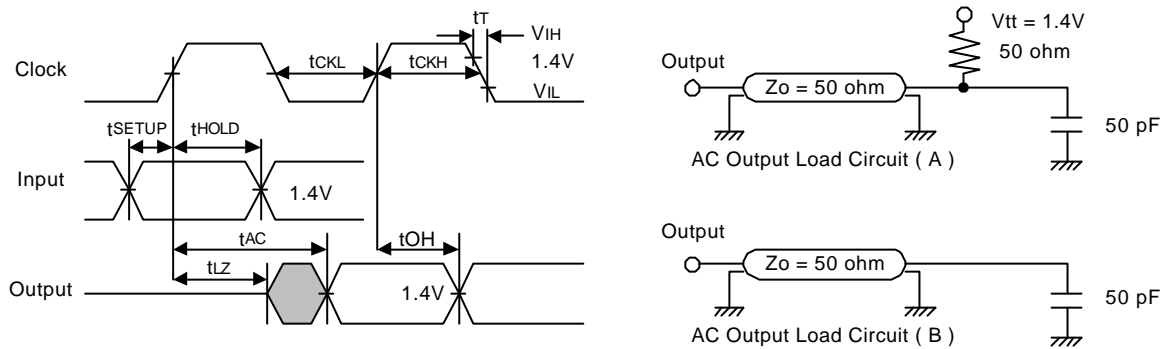
## AC Timing Parameters

## Clock and Clock Enable Parameters

| Symbol | Parameter | - 7 | | - 75B | | - 75 | | - 8B | | - 8A | | Unit | Note |
|--------|-----------|-----|------|-------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tCK3 | Clock Cycle Time, /CAS Latency = 3 | 7 | - | 7.5 | - | 7.5 | - | 8 | - | 8 | - | ns | |
| tCK2 | Clock Cycle Time, /CAS Latency = 2 | - | - | 10 | - | - | - | 10 | - | 12 | - | ns | |
| tAC3(A) | Clock Access Time, /CAS Latency = 3 | - | 6 | - | - | - | - | - | - | - | - | ns | 1 |
| tAC2(A) | Clock Access Time, /CAS Latency = 2 | - | - | - | - | - | - | - | - | - | - | ns | 1 |
| tAC3(B) | Clock Access Time, /CAS Laten cy = 3 | - | - | - | 5.4 | - | 5.4 | - | 6 | - | 6 | ns | 2 |
| tAC2(B) | Clock Access Time, /CAS Latency = 2 | - | - | 6 | - | - | - | - | 6 | - | 6 | ns | 2 |
| tCKH | Clock High Pulse Width | 3 | - | 2.5 | - | 2.5 | - | 3 | - | 3 | - | ns | |
| tCKL | Clock Low Pulse Width | 3 | - | 2.5 | - | 2.5 | - | 3 | - | 3 | - | ns | |
| tCES | Clock Enable Set-up Time | 2 | - | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | |
| tCEH | Clock Enable Hold Time | 1 | - | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | |
| tSB | Power down mode Entry Time | 0 | 7 | 0 | 7.5 | 0 | 7.5 | 0 | 10 | 0 | 12 | ns | |
| tT | Transition Time (Rise and Fall) | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | ns | |

1. Access time is measured at 1.4V. See AC Characteristics: notes 1, 2, 3, 4, 5 and load circuit A
2. Access time is measured at 1.4V. See AC Characteristics: notes 1, 2, 3, 6, 7 and load circuit B.

## Common Parameters

| Symbol | Parameter | - 7 | | - 75B | | - 75 | | - 8B | | - 8A | | Unit | Note |
|--------|-----------|-----|------|-------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tCS | Command Setup Time | 2 | - | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | |
| tCH | Command Hold Time | 1 | - | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | |
| tAS | Address and Bank Select Set-up Time | 2 | - | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | |
| tAH | Address and Bank Select Hold Time | 1 | - | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | |
| tRCD | /RAS to /CAS Delay | 21 | - | 20 | - | 20 | - | 20 | - | 20 | - | ns | 1 |
| tRC | Bank Cycle Time | 70 | - | 65 | - | 65 | - | 70 | - | 70 | - | ns | 1 |
| tRAS | Active Command Period | 49 | | 45 | | 45 | | 50 | | 50 | - | ns | 1 |
| tRP | Precharge Time | 21 | - | 20 | - | 20 | - | 20 | - | 20 | - | ns | 1 |
| tRRD | Bank to Bank Delay Time | 14 | - | 15 | - | 15 | - | 20 | - | 20 | - | ns | 1 |
| tCCD | /CAS to /CAS Delay Time | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | CLK | |

1. These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

## Mode Register Set Cycle

| Symbol | Parameter | - 7 | | - 75B | | - 75 | | - 8B | | - 8A | | Unit | Note |
|--------|-----------|-----|------|-------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tRSC | Mode Register Set Cycle Time | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | CLK | 1 |

1.These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

## Read Cycle

| Symbol | Parameter | - 7 | | - 75B | | - 75 | | - 8B | | - 8A | | Unit | Note |
|--------|-----------|-----|------|-------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tOH | Data Out Hold Time | 2.5 | - | - | - | - | - | 2.5 | - | 2.5 | - | ns | 1 |
| | | | | 2.7 | - | 2.7 | - | 3 | - | 3 | - | ns | 2 |
| tLZ | Data Out to Low Impedance Time | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns | |
| tHZ3 | Data Out to High | 3 | 6 | 3 | 5.4 | 3 | 5.4 | 3 | 6 | 3 | 6 | ns | 3 |
| tHZ2 | Impedance Time | - | - | - | - | - | - | 3 | 6 | 3 | 8 | ns | 3 |
| tDQZ | DQM Data Out Disable Latency | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | CLK | |

1.AC Output Load Circuit A.
2.AC Output Load Circuit B.
3.Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

## Refresh Cycle

| Symbol | Parameter | - 7 | | - 75B | | - 75 | | - 8B | | - 8A | | Unit | Note |
|--------|-----------|-----|------|-------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tREF | Refresh Period | - | 64 | - | 64 | - | 64 | - | 64 | - | 64 | ms | |
| tSREX | Self Refresh Exit Time | 10 | - | 10 | - | 10 | - | 10 | - | 10 | - | ns | |

## Write Cycle

| Symbol | Parameter | - 7 | | - 75B | | - 75 | | - 8B | | - 8A | | Unit | Note |
|--------|-----------|-----|------|-------|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tDS | Data In Set-up Time | 2 | - | 1.5 | - | 1.5 | - | 2 | - | 2 | - | ns | |
| tDH | Data In Hold Time | 1 | - | 0.8 | - | 0.8 | - | 1 | - | 1 | - | ns | |
| tDPL | Data input to Precharge | 14 | - | 15 | - | 15 | - | 15 | - | 15 | - | ns | |
| tDAL3 | Data In to Active Delay /CAS Latency = 3 | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | CLK | |
| tDAL2 | Data In to Active Delay /CAS Latency = 2 | - | - | - | - | - | - | 4 | - | 3 | - | CLK | |
| tDQW | DQM Write Mask Latency | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns | |

**64Mb : x4**
**PC133 / PC100 Synchronous DRAM**

## Clock Frequency and Latency

| Symbol | Parameter | - 7 | - 75B | | - 75 | - 8B | | - 8A | | Units |
|--------|-----------|-----|-----|-----|------|------|------|------|------|-------|
| tCK | Clock Frequency | 143 | 133 | 100 | 133 | 125 | 100 | 125 | 83 | MHz |
| tCK | Clock Cycle Time | 7 | 7.5 | 10 | 7.5 | 8 | 10 | 8 | 12 | ns |
| tAA | /CAS Latency | 3 | 3 | 2 | 3 | 3 | 2 | 3 | 2 | CLK |
| tRP | Precharge Time | 3 | 3 | 2 | 3 | 3 | 2 | 3 | 2 | CLK |
| tRCD | /RAS to /CAS Delay | 3 | 3 | 2 | 3 | 3 | 2 | 3 | 2 | CLK |
| tRC | Bank Cycle Time | 10 | 9 | 7 | 9 | 9 | 7 | 9 | 6 | CLK |
| tRAS | Minimum Bank Active Time | 7 | 6 | 5 | 6 | 6 | 5 | 6 | 4 | CLK |
| tDPL | Data In to Precharge | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | CLK |
| tDAL | Data In to Active/Refresh | 5 | 5 | 4 | 5 | 5 | 4 | 5 | 4 | CLK |
| tRRD | Bank  to Bank Delay Time | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | CLK |
| tCCD | /CAS to /CAS Delay Time | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | CLK |
| tWL | Write Latency | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLK |
| tDQW | DQM Write Mask Latency | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | CLK |
| tDQZ | DQM Data Disable Latency | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | CLK |
| tCSL | Clock Suspend Latency | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | CLK |

## Command Truth Table

| Function | Device State | CKE Previous Cycle | CKE Current Cycle | /CS | /RAS | /CAS | /WE | DQM | A12, A13 | A10 | A11, A0-A9 | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mode Register Set | Idle | H | X | L | L | L | L | X | OP Code | | | |
| Auto (CBR) Refresh | Idle | H | H | L | L | L | H | X | X | X | X | |
| Entry Self Refresh | Idle | H | L | L | L | L | H | X | X | X | X | |
| Exit Self Refresh | Idle(Self-Refresh) | L | H | H | X | X | X | X | X | X | X | |
| | | | | L | H | H | H | | | | | |
| Single Bank Precharge | See Current State Table | H | X | L | L | H | L | X | BS | L | X | 2 |
| Precharge all Banks | See Current State Table | H | X | L | L | H | L | X | X | H | X | |
| Bank Activate | Idle | H | X | L | L | H | H | X | BS | Row address | | 2 |
| Write | Active | H | X | L | H | L | L | X | BS | L | Column | 2 |
| Write with Auto-Precharge | Active | H | X | L | H | L | L | X | BS | H | Column | 2 |
| Read | Active | H | X | L | H | L | H | X | BS | L | Column | 2 |
| Read with Auto-Precharge | Active | H | X | L | H | L | H | X | BS | H | Column | 2 |
| Burst Termination | Active | H | X | L | H | H | L | X | X | X | X | 3,8 |
| No Operation | Any | H | X | L | H | H | H | X | X | X | X | |
| Device Deselect | Any | H | X | H | X | X | X | X | X | X | X | |
| Clock Suspend Mode Entry | Active | H | L | X | X | X | X | X | X | X | X | 4 |
| Clock Suspend Mode Exit | Active | L | H | X | X | X | X | X | X | X | X | |
| Data Write/Output Enable | Active | H | X | X | X | X | X | L | X | X | X | 5 |
| Data Mask/Output Disable | Active | H | X | X | X | X | X | H | X | X | X | |
| Power Down Mode Entry | Idle/Active | H | L | H | X | X | X | X | X | X | X | 6,7 |
| | | | | L | H | H | H | | | | | |
| Power Down Mode Exit | Any (Power Down) | L | H | H | X | X | X | X | X | X | X | 6,7 |
| | | | | L | H | H | H | | | | | |

1. All of the SDRAM operations are defined by states of /CS, /WE, /RAS, /CAS, and DQM at the positive rising edge of the clock. Operation of both decks of a stacked device at the same time is allowed, depending on the operation being performed on the other deck. Refer to the Current State Truth Table.
2. Bank Select(BS0,BS1):BS0,BS1=0,0 selects bank0; BS0,BS1=0,1 selects bank1; BS0,BS1=1,0 selects bank2; BS0,BS1= 1,1 selects bank 3.
3. During a Burst Write cycle there is a zero clock delay; for a Burst Read cycle the delay is equal to the /CAS latency.
4. During normal access mode, CKE is held high and CLK is enabled. When it is low, it freezes the internal clock and extends data Read and Write operations. One clock delay is required for mode entry and exit.
5. The DQM has two functions for the data DQ Read and Write operations. During a Read cycle, when DQM goes high data clock timing the data outputs are disabled and become high impedance after a two-clock delay. DQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).
6. All banks must be precharged before entering the Power Down Mode. (If this command is issued during a burst operation, the device state will be Clock Suspend Mode.) The Power Down Mode does not perform any refresh operations; therefore the device can't remain in this mode longer than the Refresh period ($t_{REF}$) of the device. One clock delay is required for mode entry and exit.
7. A No Operation or Device Deselect Command is required on the next clock edge following CKE going high.
8. Device state is full page burst operation. Use of this command to terminate other burst length operations is illegal.

## Clock Enable (CKE) Truth Table

| Current State | CKE Previous Cycle | CKE Current Cycle | /CS | /RAS | /CAS | /WE | A12, A13 | A11–A10 | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Self Fresh | H | X | X | X | X | X | X | X | INVALID | 1 |
| | L | H | H | X | X | X | X | X | Exit Self Refresh with Device Deselect | 2 |
| | L | H | L | H | H | H | X | X | Exit Self Refresh with No Operation | 2 |
| | L | H | L | H | H | L | X | X | ILLEGAL | 2 |
| | L | H | L | H | L | X | X | X | ILLEGAL | 2 |
| | L | H | L | L | X | X | X | X | ILLEGAL | 2 |
| | L | L | X | X | X | X | X | X | Maintain Self Refresh | |
| Power Down | H | X | X | X | X | X | X | X | INVALID | 1 |
| | L | H | H | X | X | X | X | X | Power Down mode exit, all banks idle | 2 |
| | L | H | L | X | X | X | X | X | ILLEGAL | 2 |
| | L | L | X | X | X | X | X | X | Maintain Power Down Mode | |
| All Banks Idle | H | H | H | X | X | X | | | Refer to the Idle State section of the Current State Truth Table | 3 |
| | H | H | L | H | X | X | | | | 3 |
| | H | H | L | L | H | X | | | | 3 |
| | H | H | L | L | L | H | X | X | CBR Refresh | |
| | H | H | L | L | L | L | OP Code | | Mode Register Set | 4 |
| | H | L | H | X | X | X | | | Refer to the Idle State section of the Current State Truth Table | 3 |
| | H | L | L | H | X | X | | | | 3 |
| | H | L | L | L | H | X | | | | 3 |
| | H | L | L | L | L | H | X | X | Entry Self Refresh | 4 |
| | H | L | L | L | L | L | OP Code | | Mode Register Set | 4 |
| | L | X | X | X | X | X | X | X | Power Down | 4 |
| Any State other than listed above | H | H | X | X | X | X | X | X | Refer to operations in the Current State Truth Table | |
| | H | L | X | X | X | X | X | X | Begin Clock Suspend next cycle | 5 |
| | L | H | X | X | X | X | X | X | Exit Clock Suspend next cycle | |
| | L | L | X | X | X | X | X | X | Maintain Clock Suspend | |

1. For the given Current State CKE must be low in the previous cycle.
2. When CKE has a low to high transition, the clock and other inputs are re-enabled asynchronously. The minimum setup time for CKE ($t_{CES}$) must be satisfied. When exiting power down mode, a NOP command (or Device Deselect Command) is required on the first rising clock after CKE goes high .
3. The address inputs (A13 - A0) depend on the command that is issued. See the Idle State section of the Current State Truth Table for more information.
4. The Precharge Power Down Mode,the Self Refresh Mode,and the Mode Register Set can only be entered from the all banks idle state.
5. Must be a legal command as defined in the Current State Truth Table.

**64Mb : x4**
**PC133 / PC100 Synchronous DRAM**

## Current State Truth Table (Part 1 of 3)(See note 1)

| Current State | /CS | /RAS | /CAS | /WE | A12, A13 | A11-A0 | Description | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Idle | L | L | L | L | OP Code | | Mode Register Set | Set the Mode Register | 2 |
| | L | L | L | H | X | X | Auto or Self Refresh | Start Auto or Self Refresh | 2,3 |
| | L | L | H | L | BS | X | Precharge | No Operation | |
| | L | L | H | H | BS | Row Address | Bank Active | Activate the specified bank and row | |
| | L | H | L | L | BS | Column | Write | ILLEGAL | 4 |
| | L | H | L | H | BS | Column | Read | ILLEGAL | 4 |
| | L | H | H | L | X | X | Burst Termination | No Operation | |
| | L | H | H | H | X | X | No Operation | No Operation | |
| | H | X | X | X | X | X | Device Deselect | No Operation or Power Down | 5 |
| Row Active | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | Precharge | 6 |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | Start Write; Determine if Auto Precharge | 7,8 |
| | L | H | L | H | BS | Column | Read | Start Read; Determine if Auto Precharge | 7,8 |
| | L | H | H | L | X | X | Burst Termination | No Operation | |
| | L | H | H | H | X | X | No Operation | No Operation | |
| | H | X | X | X | X | X | Device Deselect | No Operation | |
| Read | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | Terminate Burst; Start the Precharge | |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | Terminate Burst; Start the Write cycle | 8,9 |
| | L | H | L | H | BS | Column | Read | Terminate Burst; Start a new Read cycle | 8,9 |
| | L | H | H | L | X | X | Burst Termination | Terminate the Burst | |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |
| Write | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | Terminate Burst; Start the Precharge | |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | Terminate Burst; Start a new Write cycle | 8,9 |
| | L | H | L | H | BS | Column | Read | Terminate Burst; Start the Read cycle | 8,9 |
| | L | H | H | L | X | X | Burst Termination | Terminate the Burst | |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |

1.  CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2.  All Banks must be idle; otherwise, it is an illegal action.
3.  If CKE is active (high) the SDRAM will start the Auto(CBR) Refresh operation, if CKE is inactive(low) than the Self Refresh mode is entered.
4.  The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5.  If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6.  The minimum and maximum Active time ($t_{RAS}$) must be satisfied.
7.  The RAS to CAS Delay ($t_{RCD}$) must occur before the command is given.
8.  Column address A10 is used to determine if the Auto Precharge function is activated.
9.  The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time ($t_{RRD}$) is not satisfied.

## Current State Truth Table (Part 2 of 3)(See note 1)

| Current State | /CS | /RAS | /CAS | /WE | A12, A13 | A11-A0 | Description | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| Read with Auto Precharge | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | 4 |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | ILLEGAL | 4 |
| | L | H | L | H | BS | Column | Read | ILLEGAL | 4 |
| | L | H | H | L | X | X | Burst Termination | ILLEGAL | |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |
| Write with Auto Precharge | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | 4 |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | ILLEGAL | 4 |
| | L | H | L | H | BS | Column | Read | ILLEGAL | 4 |
| | L | H | H | L | X | X | Burst Termination | ILLEGAL | |
| | L | H | H | H | X | X | No Operation | Continue the Burst | |
| | H | X | X | X | X | X | Device Deselect | Continue the Burst | |
| Precharging | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | No Operation; Bank(s) idle after $t_{RP}$ | |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | ILLEGAL | 4 |
| | L | H | L | H | BS | Column | Read | ILLEGAL | 4 |
| | L | H | H | L | X | X | Burst Termination | No Operation; Bank(s) idle after $t_{RP}$ | |
| | L | H | H | H | X | X | No Operation | No Operation; Bank(s) idle after $t_{RP}$ | |
| | H | X | X | X | X | X | Device Deselect | No Operation; Bank(s) idle after $t_{RP}$ | |
| Row Activating | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | 4 |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4,10 |
| | L | H | L | L | BS | Column | Write | ILLEGAL | 4 |
| | L | H | L | H | BS | Column | Read | ILLEGAL | 4 |
| | L | H | H | L | X | X | Burst Termination | No Operation; Row Active after $t_{RCD}$ | |
| | L | H | H | H | X | X | No Operation | No Operation; Row Active after $t_{RCD}$ | |
| | H | X | X | X | X | X | Device Deselect | No Operation; Row Active after $t_{RCD}$ | |

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto(CBR) Refresh operation, if CKE is inactive(low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time ($t_{RAS}$) must be satisfied.
7. The RAS to CAS Delay ($t_{RCD}$) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time ($t_{RRD}$) is not satisfied.

## Current State Truth Table (Part 3of 3)(See note 1)

| Current State | /CS | /RAS | /CAS | /WE | A12, A13 | A11-A0 | Description | Action | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Command | | | | |
| Write Recovering | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | 4 |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | Start Write; Determine if Auto Precharge | 9 |
| | L | H | L | H | BS | Column | Read | Start Write; Determine if Auto Precharge | 9 |
| | L | H | H | L | X | X | Burst Termination | No Operation; Row Active after $t_{DPL}$ | |
| | L | H | H | H | X | X | No Operation | No Operation;Row Active after $t_{DPL}$ | |
| | H | X | X | X | X | X | Device Deselect | No Operation; Row Active after $t_{DPL}$ | |
| Write Recovering With Auto Precharge | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | 4 |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | 4 |
| | L | H | L | L | BS | Column | Write | ILLEGAL | 4,9 |
| | L | H | L | H | BS | Column | Read | ILLEGAL | 4,9 |
| | L | H | H | L | X | X | Burst Termination | No Operation; Precharge Active after $t_{DPL}$ | |
| | L | H | H | H | X | X | No Operation | No Operation; Precharge Active after $t_{DPL}$ | |
| | H | X | X | X | X | X | Device Deselect | No Operation; Precharge Active after $t_{DPL}$ | |
| Refreshing | L | L | L | L | OP Code | | Mode Regis ter Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | |
| | L | H | L | L | BS | Column | Write | ILLEGAL | |
| | L | H | L | H | BS | Column | Read | ILLEGAL | |
| | L | H | H | L | X | X | Burst Termination | No Operation; Idle after $t_{RC}$ | |
| | L | H | H | H | X | X | No Operation | No Operation; Idle after $t_{RC}$ | |
| | H | X | X | X | X | X | Device Deselect | No Operation; Idle after $t_{RC}$ | |
| Mode Register Accessing | L | L | L | L | OP Code | | Mode Register Set | ILLEGAL | |
| | L | L | L | H | X | X | Auto or Self Refresh | ILLEGAL | |
| | L | L | H | L | BS | X | Precharge | ILLEGAL | |
| | L | L | H | H | BS | Row Address | Bank Active | ILLEGAL | |
| | L | H | L | L | BS | Column | Write | ILLEGAL | |
| | L | H | L | H | BS | Column | Read | ILLEGAL | |
| | L | H | H | L | X | X | Burst Termination | ILLEGAL | |
| | L | H | H | H | X | X | No Operation | | |
| | H | X | X | X | X | X | Device Deselect | | |

1. CKE is assumed to be active (high) in the previous cycle for all entries. The Current State is the state of the bank that the Command is being applied to.
2. All Banks must be idle; otherwise, it is an illegal action.
3. If CKE is active (high) the SDRAM will start the Auto(CBR) Refresh operation, if CKE is inactive(low) than the Self Refresh mode is entered.
4. The Current State refers to only one of the banks. If BS selects this bank then the action is illegal. If BS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
5. If CKE is inactive (low) then the Power Down mode is entered; otherwise there is a No Operation.
6. The minimum and maximum Active time ($t_{RAS}$) must be satisfied.
7. The RAS to CAS Delay ($t_{RCD}$) must occur before the command is given.
8. Column address A10 is used to determine if the Auto Precharge function is activated.
9. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.
10. The command is illegal if the minimum bank to bank delay time ($t_{RRD}$) is not satisfied.

# DEVICE OPERATIONS

## Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs.

Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a predefined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power on voltage must not exceed VDD+0.3V on any of the input pins or VDD supplies. The CLK signal must be started at the same time. After power on, an initial pause of 200μs is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power on, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. A minimum of eight  Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

## Programming the Mode Register

For application flexibility, /CAS latency, burst length, burst sequence, and operation type are user defined variables and must be programmed into the SDRAM Mode Register with a single Mode Register Set Command. Any content of the Mode Register can be altered by re -executing the Mode Register Set Command. If the user chooses to modify only a subset of the Mode Register variables, all four variables must be redefined when the Mode Register Set Command is issued.

After initial power up, the Mode Register Set Command must be issued before read or write cycles may begin. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of /RAS, /CAS, /CS, and /WE at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to tRSC has elapsed.

### /CAS Latency

The /CAS latency is a parameter that is used to define the delay from when a Read Command is registered on a rising clock edge to when the data from that Read Command becomes available at the outputs. The /CAS latency is expressed in terms of clock cycles and can have a value of 2 or 3 cycles. The value of the /CAS latency is determined by the speed grade of the device and the  clock frequency that is used in the application. A table showing the relationship between the /CAS latency, speed grade, and clock frequency appears in the Electrical Characteristics section of this document. Once the appropriate /CAS latency has been sele cted it must be programmed into the mode register after power up, for an explanation of this procedure see Programming the Mode Register in the previous section.

## Mode Register Definition
**Mode Register set: (Programming mode)**

| A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address bus (Ax) |
|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|------------------|
| Operation Mode | | | | | | | CAS Latency | | | BT | Burst Length | | | Mode Register (Mx) |

| CAS Latency | | | | Burst Type | | Burst Length | | | | |
|----|----|----|---------|----|-----------|----|----|----|----------|----------|
| M6 | M5 | M4 | Latency | M3 | Type | M2 | M1 | M0 | BT=0 | BT=1 |
| 0 | 0 | 0 | Reserved | 0 | Sequential | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | Reserved | 1 | Interleave | 0 | 0 | 1 | 2 | 2 |
| 0 | 1 | 0 | 2 | | | 0 | 1 | 0 | 4 | 4 |
| 0 | 1 | 1 | 3 | | | 0 | 1 | 1 | 8 | 8 |
| 1 | 0 | 0 | Reserved | | | 1 | 0 | 0 | Reserved | Reserved |
| 1 | 0 | 1 | Reserved | | | 1 | 0 | 1 | Reserved | Reserved |
| 1 | 1 | 0 | Reserved | | | 1 | 1 | 0 | Reserved | Reserved |
| 1 | 1 | 1 | Reserved | | | 1 | 1 | 1 | Full Page | Reserved |

| Operation Mode | | | | | | | |
|-----|-----|-----|-----|----|----|----|------|
| M13 | M12 | M11 | M10 | M9 | M8 | M7 | Mode |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | Normal |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | Multiple Burst with Single Write |

## Burst Mode Operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). Three parameters define how the burst mode will operate: burst sequence, burst length, and operation mode. The burst sequence and burst length are programmable and are determined by address bits A0 - A3 during the Mode Register Set command. Operation mode is also programmable and is set by address bits A7 - A13.

Burst sequence defines the order in which the burst data will be delivered or stored to the SDRAM. The two types of burst sequence supported are sequential and interleaved. See the table below.

The burst length controls the number of bits that will be output after a Read Command, or the number of bits to be input after a Write Command. The burst length can be programmed to have values of 1, 2, 4, 8 or full page (actual page length is dependent on organization: x4, x8, or x16). Full page burst operation is only possible using the sequential burst type.

Burst operation mode can be normal operation or multiple burst with single write operation. Normal operation implies that the device will perform burst operations on both read and write cycles until the desired burst length is satisfied. Multiple burst with single write operation was added to support Write Through Cache operation. Here, the programmed burst length only applies to read cycles. All write cycles are single write operations when this mode is selected.

## Burst Length and Sequence

| Burst Length | Starting Bit | | | Interleave | Sequential |
|:---:|:---:|:---:|:---:|:---:|:---:|
| | A0 | | | | |
| 2 | 0 | | | 0-1 | 0-1 |
| | 1 | | | 1-0 | 1-0 |
| | A1 | A0 | | | |
| | 0 | 0 | | 0-1-2-3 | 0-1-2-3 |
| 4 | 0 | 1 | | 1-0-3-2 | 1-2-3-0 |
| | 1 | 0 | | 2-3-0-1 | 2-3-0-1 |
| | 1 | 1 | | 3-2-1-0 | 3-0-1-2 |
| | A2 | A1 | A0 | | |
| | 0 | 0 | 0 | 0-1-2-3-4-5-6-7 | 0-1-2-3-4-5-6-7 |
| | 0 | 0 | 1 | 1-0-3-2-5-4-7-6 | 1-2-3-4-5-6-7-0 |
| | 0 | 1 | 0 | 2-3-0-1-6-7-4-5 | 2-3-4-5-6-7-0-1 |
| 8 | 0 | 1 | 1 | 3-2-1-0-7-6-5-4 | 3-4-5-6-7-0-1-2 |
| | 1 | 0 | 0 | 4-5-6-7-0-1-2-3 | 4-5-6-7-0-1-2-3 |
| | 1 | 0 | 1 | 5-4-7-6-1-0-3-2 | 5-6-7-0-1-2-3-4 |
| | 1 | 1 | 0 | 6-7-4-5-2-3-0-1 | 6-7-0-1-2-3-4-5 |
| | 1 | 1 | 1 | 7-6-5-4-3-2-1-0 | 7-0-1-2-3-4-5-6 |
| Full Page (Note) | n | n | n | Not supported | Cn, Cn+1,Cn+2….. |

Note : Page length is a function of I/O organization and column addressing.
X 4  organization (CA0-CA9); Page Length = 1024 bits

## Bank Activate Command

In relation to the operation of a fast page mode DRAM, the Bank Activate command corresponds to a falling /RAS signal. The Bank Activate command is issued by holding /CAS and /WE high with /CS and /RAS low at the rising edge of the clock. The bank select address A12 - A13 is used to select the desired bank. The row address A0 - A11 is used to determine which row to activate in the selected bank.

The Bank Activate command must be applied before any Read or Write operation can be executed. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must meet or exceed the /RAS to /CAS delay time (tRCD). Once a bank has been activated, it must be precharged before another Bank Activate command can be applied to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (tRRD). The maximum time that each bank can be held active is specified as tRAS(max).

## Bank Activate Command Cycle

$\overline{CAS}$ Latency = 3, tRCD = 3
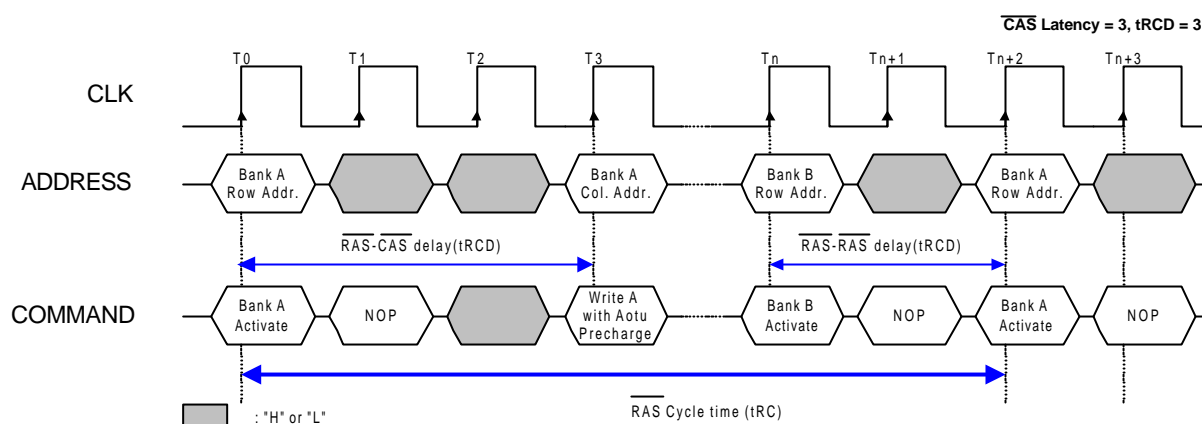


## Bank Select

The Bank Select inputs, BS0 and BS1, determine the bank to be used during a Bank Activate, Precharge, Read, or Write operation.

## Bank Selection Bits

| BS0 | BS1 | Bank |
|-----|-----|--------|
| 0 | 0 | Bank 0 |
| 0 | 1 | Bank 1 |
| 1 | 0 | Bank 2 |
| 1 | 1 | Bank 3 |

## Read and Write Access Modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting /RAS high and /CAS low at the clock's rising edge after the necessary /RAS to /CAS delay (tRCD). /WE must also be defined at this time to determine whether the access cycle is a read operation (/WE high), or a write operation (/WE low). The address inputs determine the starting column address.

The SDRAM provides a wide variety of fast access modes. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles at data rates of up to 150 MHz. The number of serial data bits for each access is equal to the burst length, which is programmed into the Mode Register. If the burst length is full page, data is repeatedly read out or written until a Burst Stop or Precharge Command is issued.

Similar to Page Mode of conventional DRAMs, a read or write cycle can not begin until the sense amplifiers latch the selected row address information. The refresh period (tREF) is what limits the number of random column accesses to an activated bank. A new burst access can be done even before the previous burst ends. The ability to interrupt a burst operation at every clock cycle is supported; this is referred to as the 1-N rule. When the previous burst is interrupted by another Read or Write Command, the remaining addresses are overridden by the new address.

Precharging an active bank after each read or write operation is not necessary, providing the same row is to be accessed again. To perform a read or write cycle to a different row within an activated bank, the bank must be precharged and a new Bank Activate command must be issued. When more than one bank is activated, interleaved (ping pong) bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, fast and seamless data access operation among many different pages can be realized. When multiple banks are activated, column to column interleave operation can be done between different pages. Finally, Read or Write Commands can be issued to the same bank or between active banks on every clock cycle.

## Burst Read Command

The Burst Read command is initiated by having /CS and /CAS low while holding /RAS and /WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets the type of burst (sequential or interleave) and the burst length (1, 2, 4, 8, full page). The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the /CAS latency that is set in the Mode Register.

## Burst Read Operation
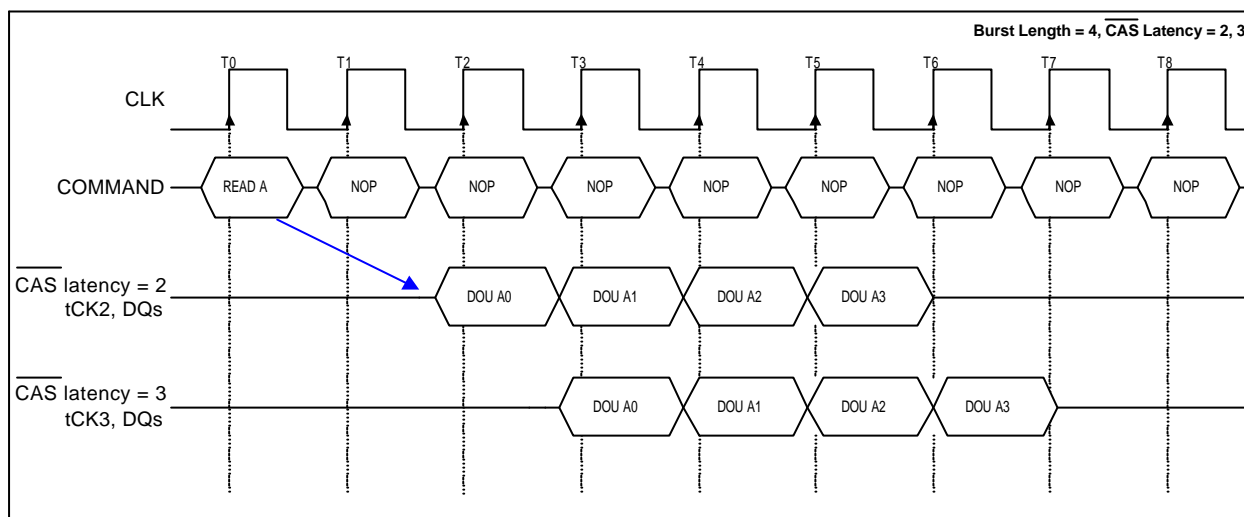


## Read Interrupted by a Read

A Burst Read may be interrupted before completion of the burst by another Read Command, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. The data from the first Read Command continues to appear on the outputs until the /CAS latency from the interrupting Read Command is satisfied, at this point the data from the interrupting Read Command appears.

## Read Interrupted by a Read
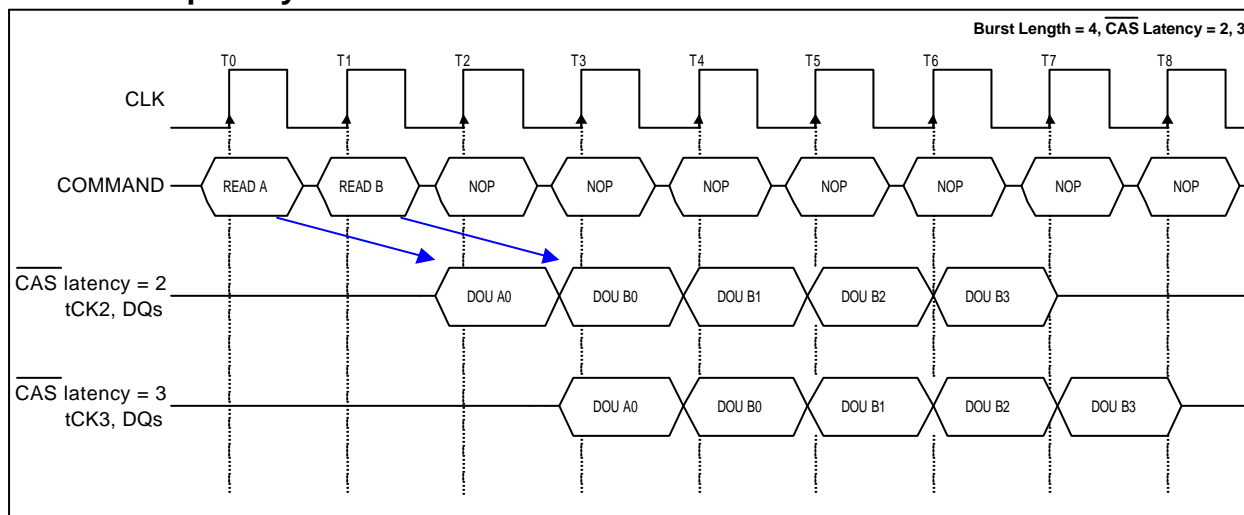
## Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus.

## Minimum Read to Write Interval
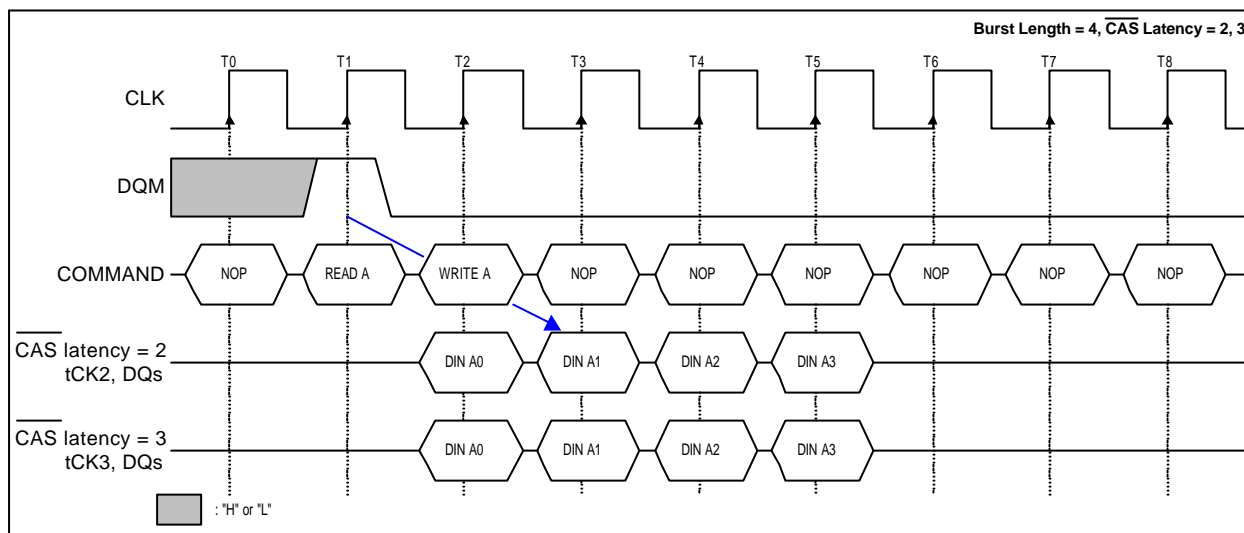


## Non-Minimum Read to Write Interval
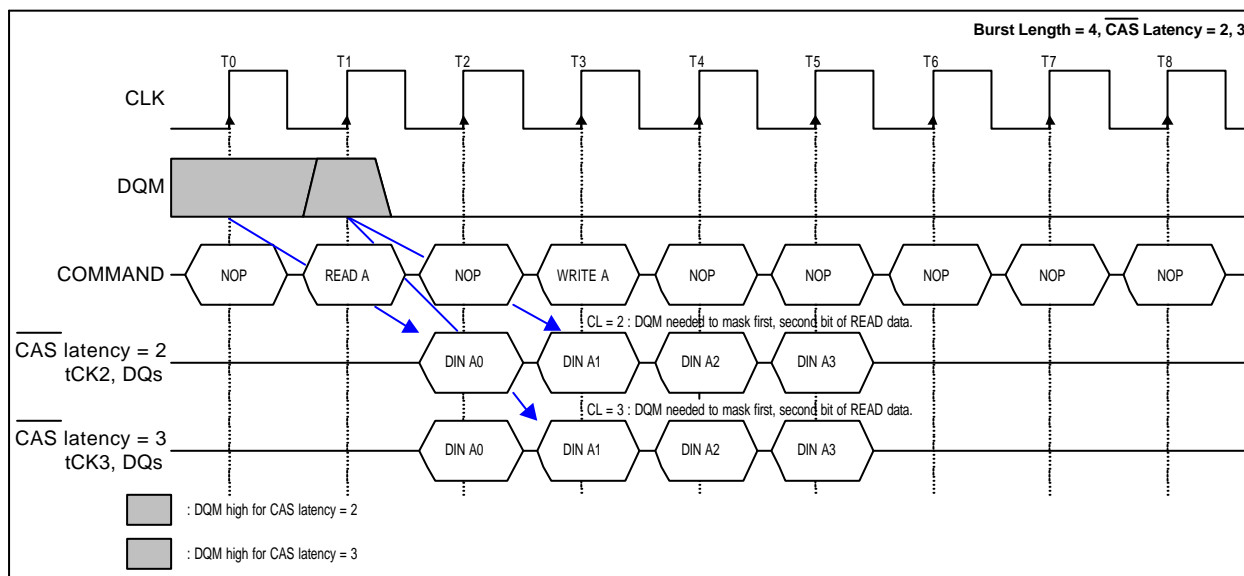
## Burst Write Command

The Burst Write command is initiated by having /CS, /CAS, and /WE low while holding /RAS high at the rising edge of the clock. The address inputs determine the starting column address. There is no /CAS latency required for burst write cycles. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.

## Burst Write Operation
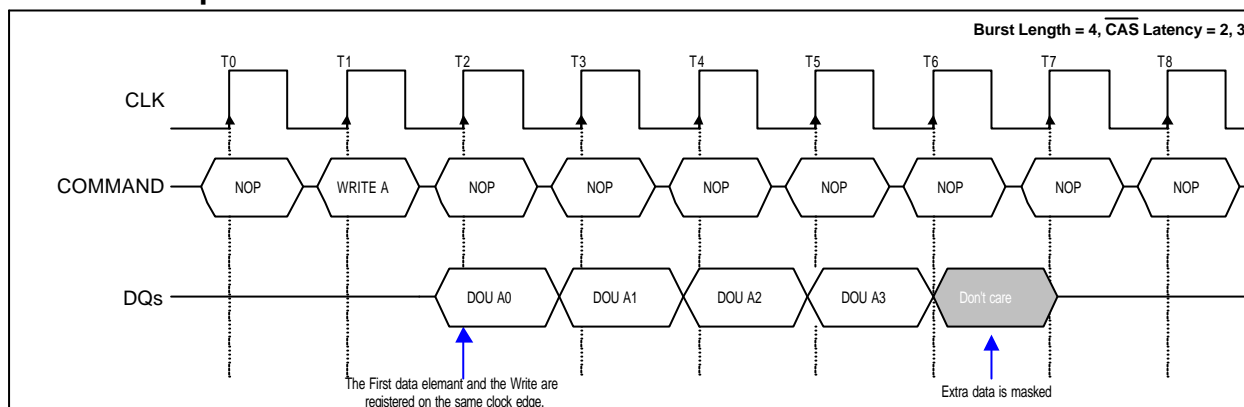


## Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

## Write Interrupted by a Write
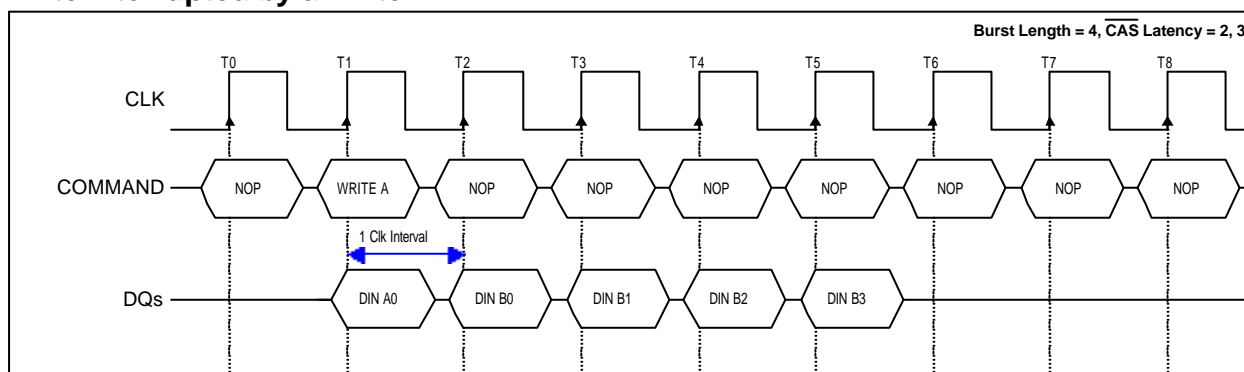
## Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is registered. The DQs must be in the high impedance state at least one cycle before the interrupting read data appears on the outputs to avoid data contention. When the Read Command is registered, any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Read Command is initiated will actually be written to the memory.

## Minimum Write to Read Interval
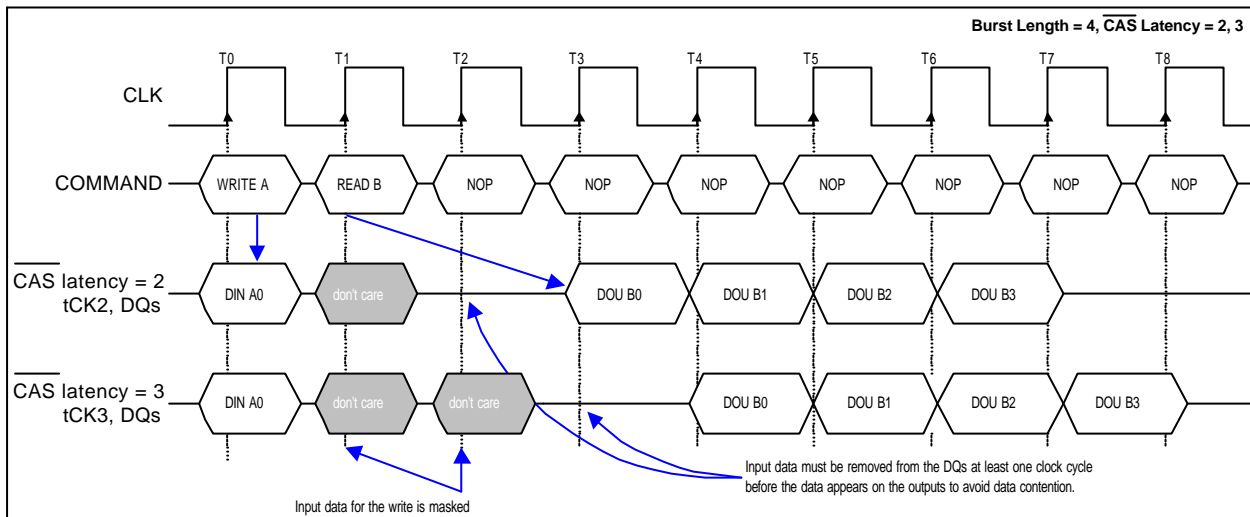


## Non-Minimum Write to Read Interval
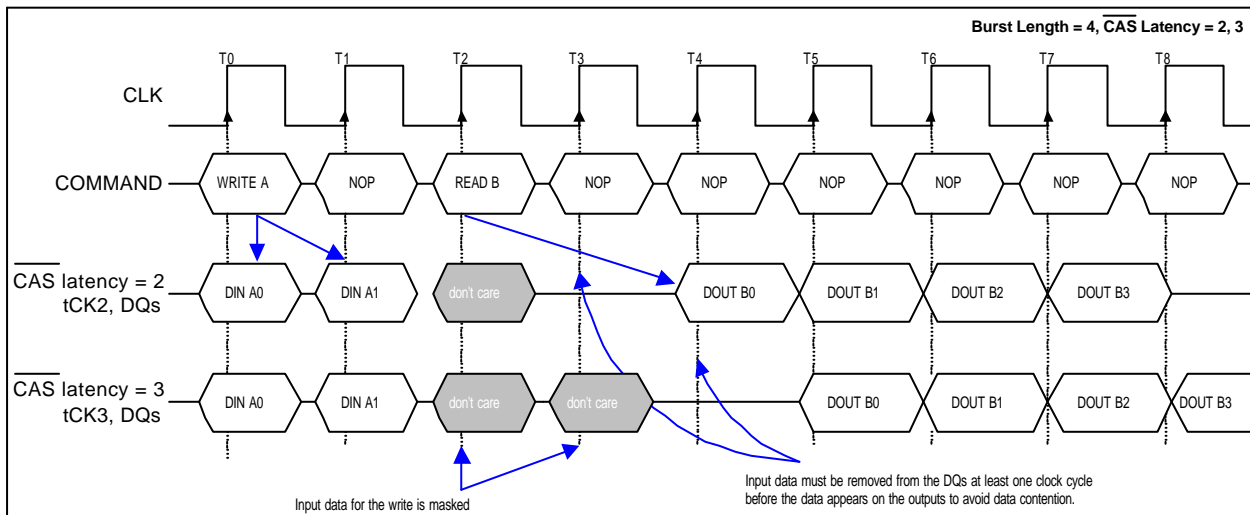


## Burst Stop Command

Once a burst read or write operation has been initiated, there exist several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation or using a Precharge Command to interrupt a burst cycle and close the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid DQ contention.

If the burst length is full page, the Burst Stop Command may also be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. Use of the Burst Stop Command during other burst length

operations is illegal. The Burst Stop Command is defined by having /RAS and /CAS high with /CS and /WE low at the rising edge of the clock.

When using the Burst Stop Command during a burst read cycle, the data DQs go to a high impedance state after a delay which is equal to the /CAS Latency set in the Mode Register.

## Termination of a Burst Read Operation



Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2, 3
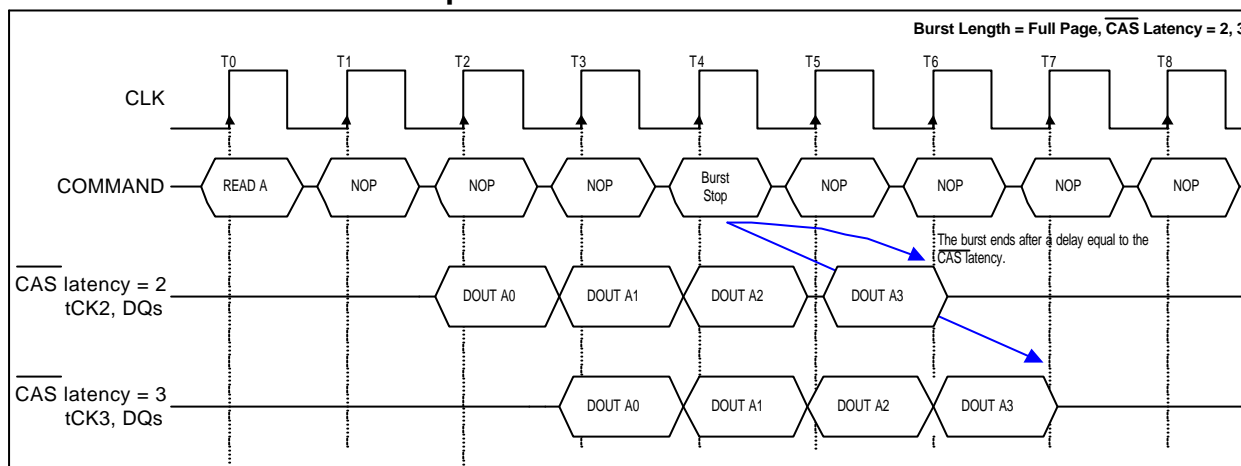
If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the DQ pins before the Burst Stop Command is registered will be written to the memory.

## Termination of a Burst Write Operation



Burst Length = Full Page, $\overline{\text{CAS}}$ Latency = 2, 3
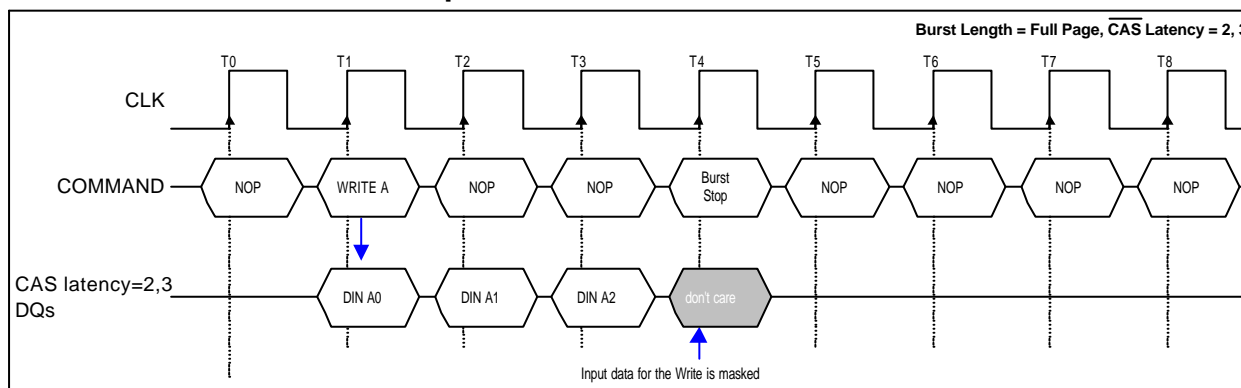
## Auto-Precharge Operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge Command or the auto-precharge function. When a Read or a Write Command is given to the SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is low when the Read or Write Command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is high when the Read or Write Command is issued, then the auto-precharge function is engaged. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge before all burst read cycles have been completed. Regardless of burst length, the precharge will begin (/CAS latency - 1) clocks prior to the last data output. Auto-precharge can also be implemented during Write commands.

A Read or Write Command without auto-precharge can be terminated in the midst of a burst operation. However, a Read or Write Command with auto-precharge can not be interrupted by a command to the same bank. Therefore use of a Read, Write, or Precharge Command to the same bank is prohibited during a read or write cycle with auto-precharge until the entire burst operation is completed. Once the precharge operation has started the bank cannot be reactivated until the Precharge time (tRP) has been satisfied. It should be noted that the device will not respond to the Auto-Precharge command if the device is programmed for full page burst read or write cycles, or full page burst read cycles with single write operation.

When using the Auto-Precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy tRAS(min). If this interval does not satisfy tRAS(min) then tRCD must be extended.

## Burst Read with Auto-Precharge
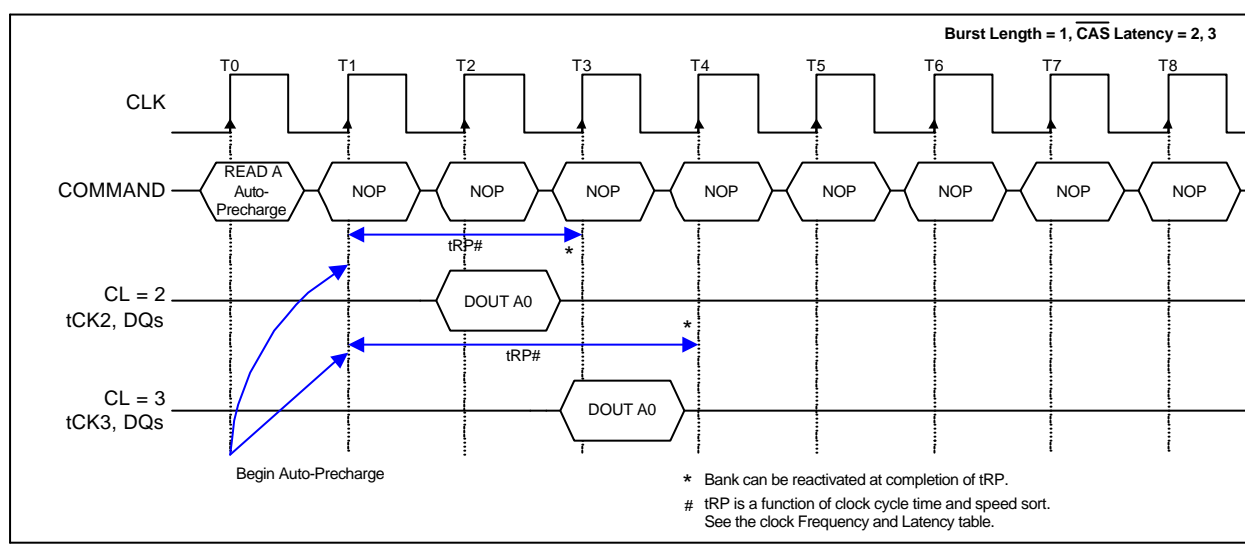
## Burst Read with Auto-Precharge
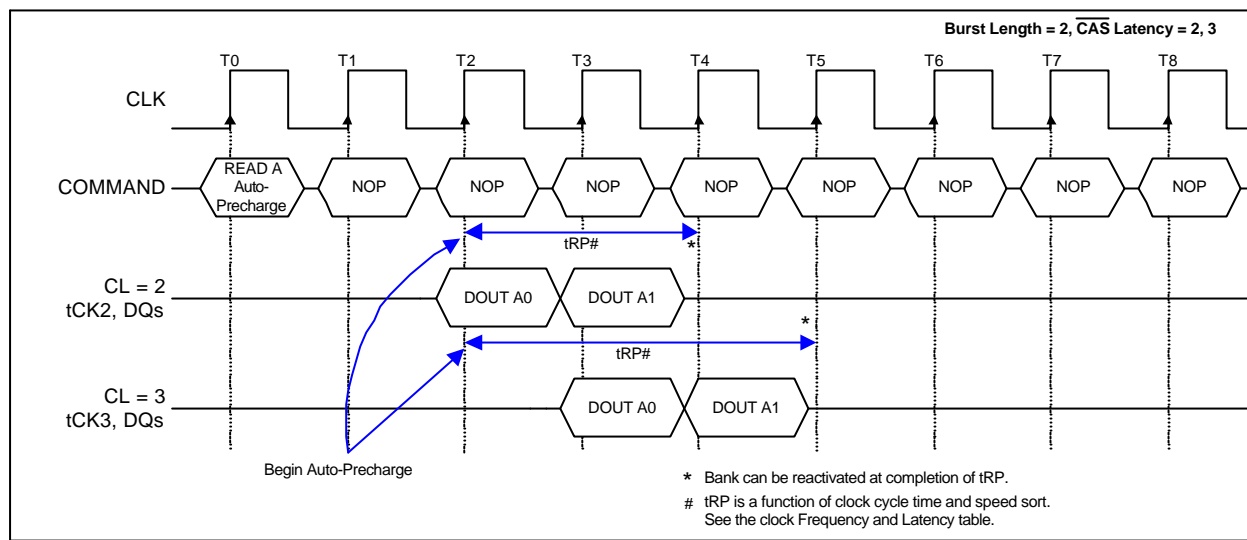


## Burst Read with Auto-Precharge
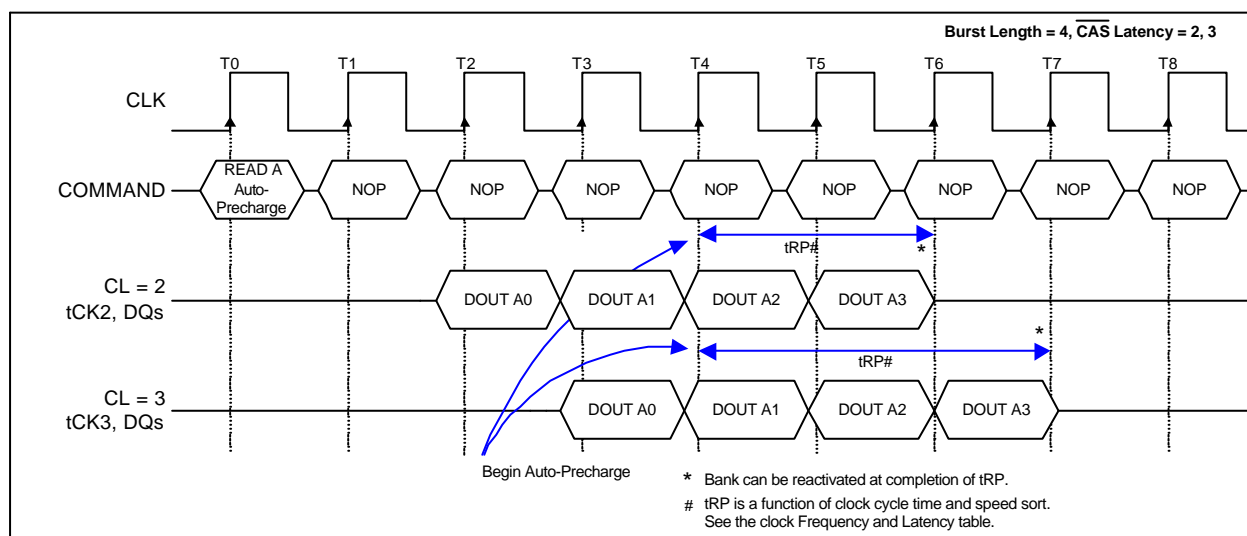
Although a Read Command with auto-precharge cannot be interrupted by a command to the same bank, it can be interrupted by a Read or Write Command to a different bank. If the interrupting command is issued before auto-precharge begins then the precharge function will begin with the new command. The bank being auto-precharged may be reactivated after the delay tRP.
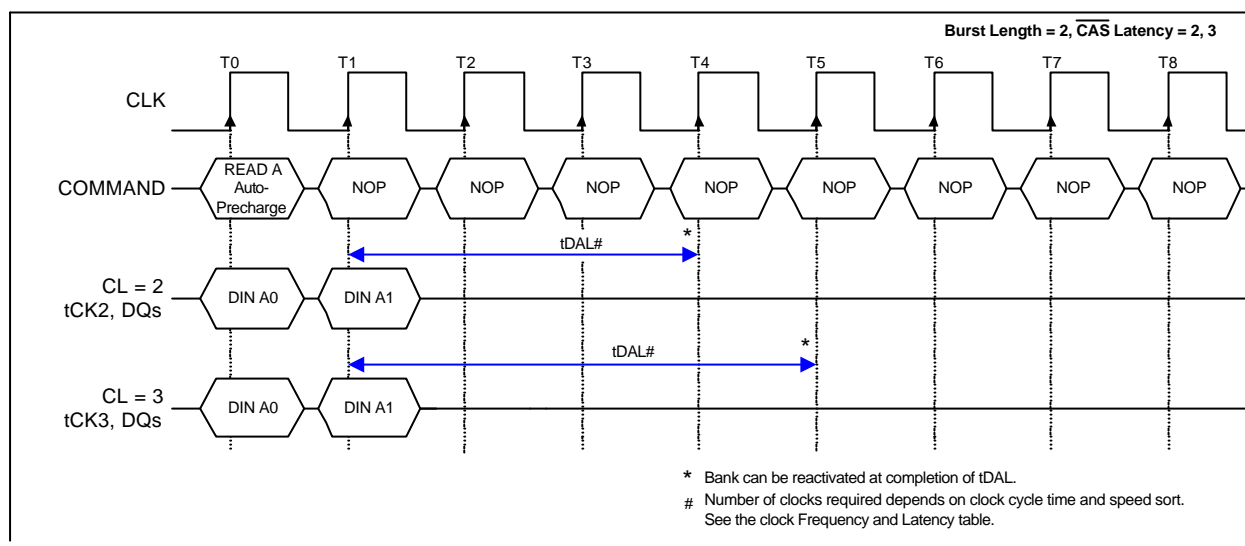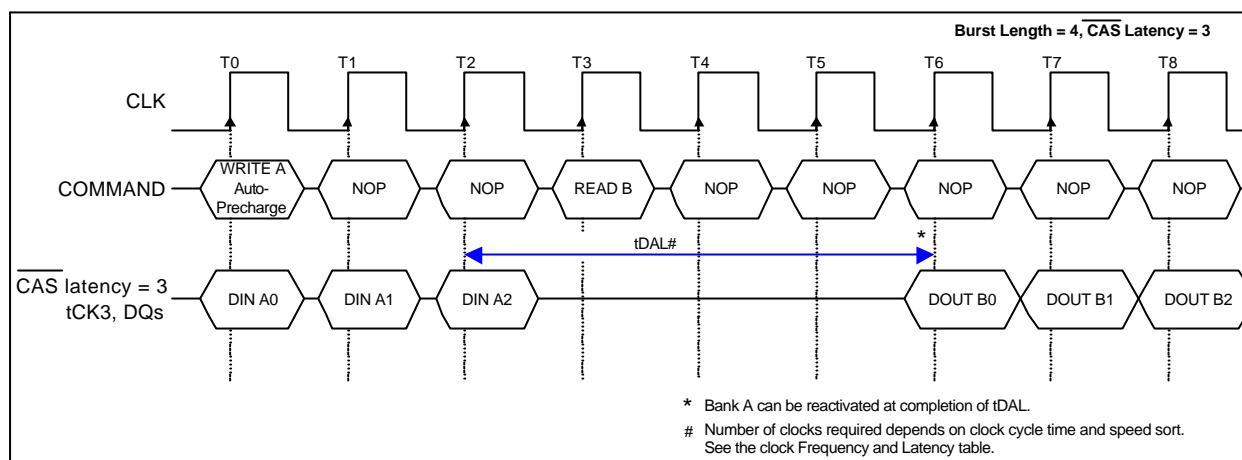
## Burst Read with Auto-Precharge Interrupted by Read
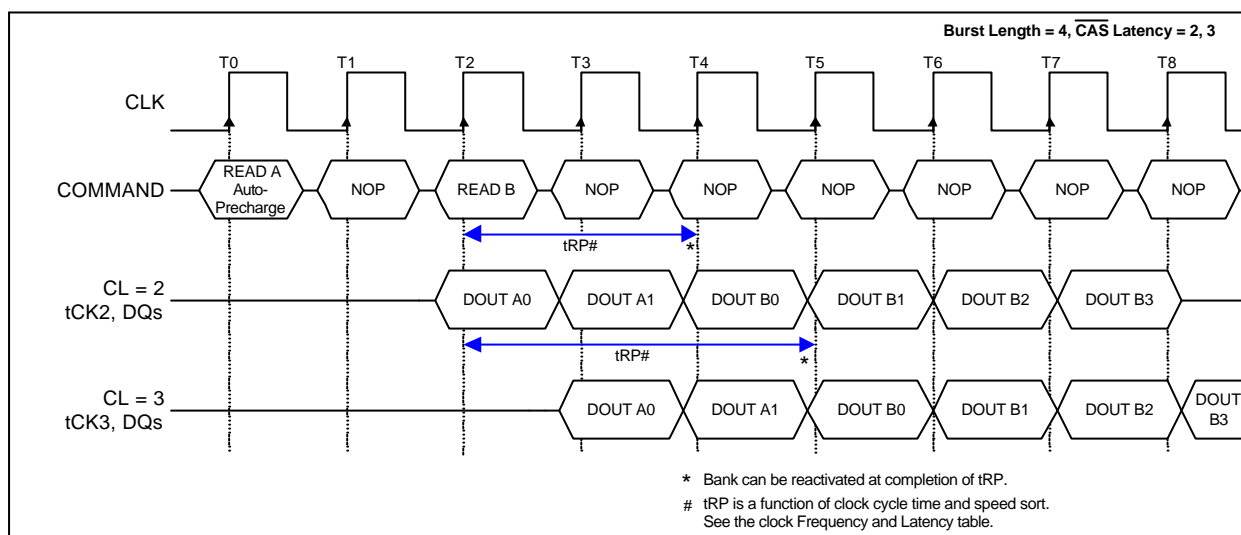


If interrupting a Read Command with auto-precharge with a Write Command, DQM must be used to avoid DQ contention.

## Burst Read with Auto-Precharge Interrupted by Write
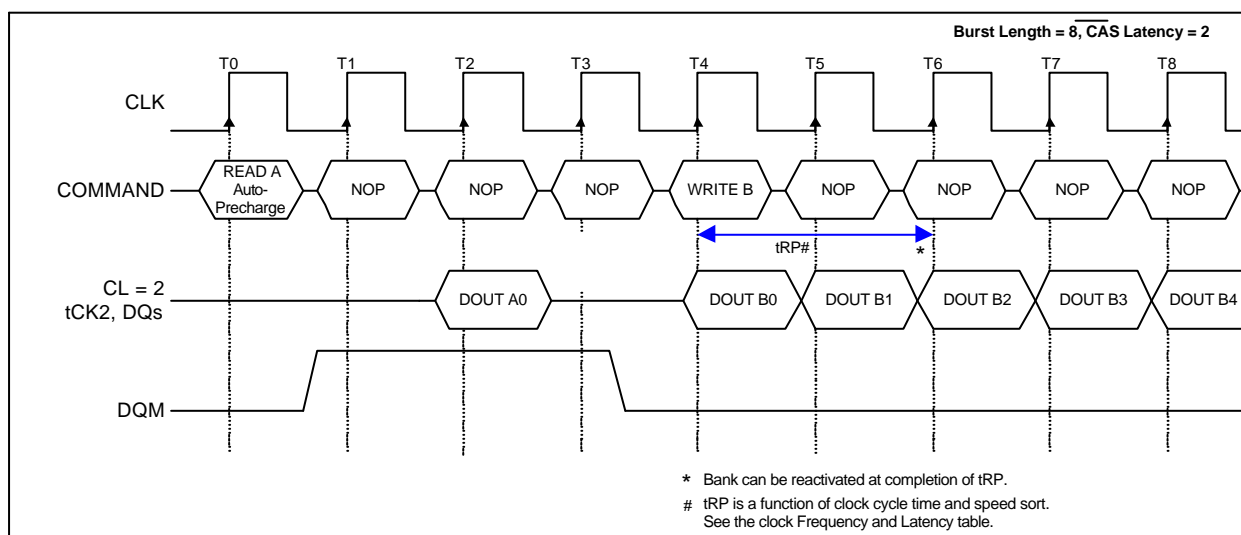
If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The bank undergoing auto-precharge can not be reactivated until tDAL, Data-in to Active delay , is satisfied.

## Burst Write with Auto-Precharge



Similar to the Read Command, a Write Command with auto-precharge can not be interrupted by a command to the same bank. It can be interrupted by a Read or Write Command to a different bank, however. The precharge function will begin with the new command. The bank may be reactivated after tRP is satisfied.

## Burst Write with Auto-Precharge Interrupted by Write

## Burst Write with Auto-Precharge Interrupted by Read



Burst Length = 4, $\overline{CAS}$ Latency = 3

* Bank A can be reactivated at completion of tDAL.
# Number of clocks required depends on clock cycle time and speed sort. See the clock Frequency and Latency table.
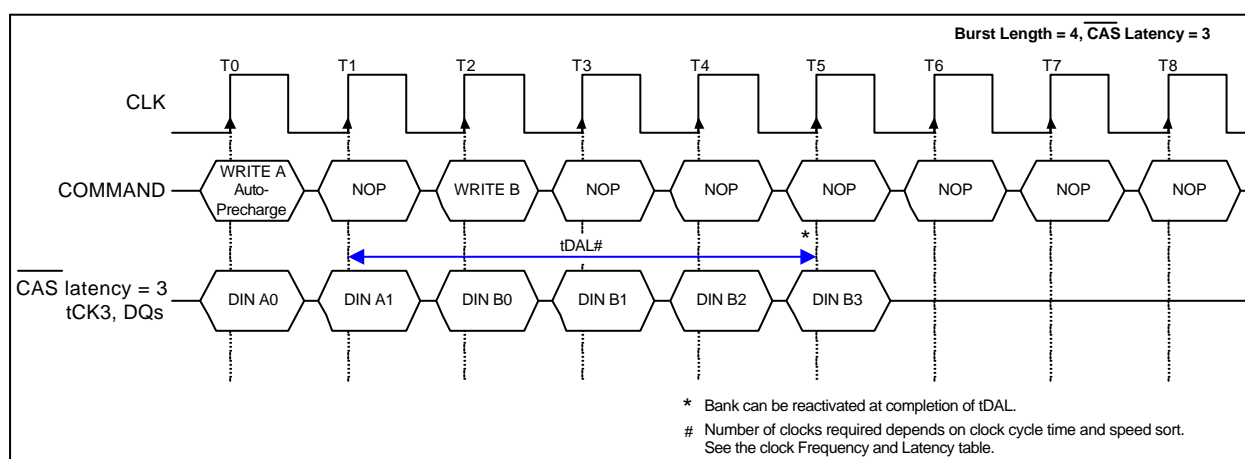
## Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is triggered when /CS, /RAS, and /WE are low and /CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Three address bits --A10, A12, and A13--are used to define which bank(s) is to be precharged when the command is issued.

## Bank Selection for Precharge by Address Bits

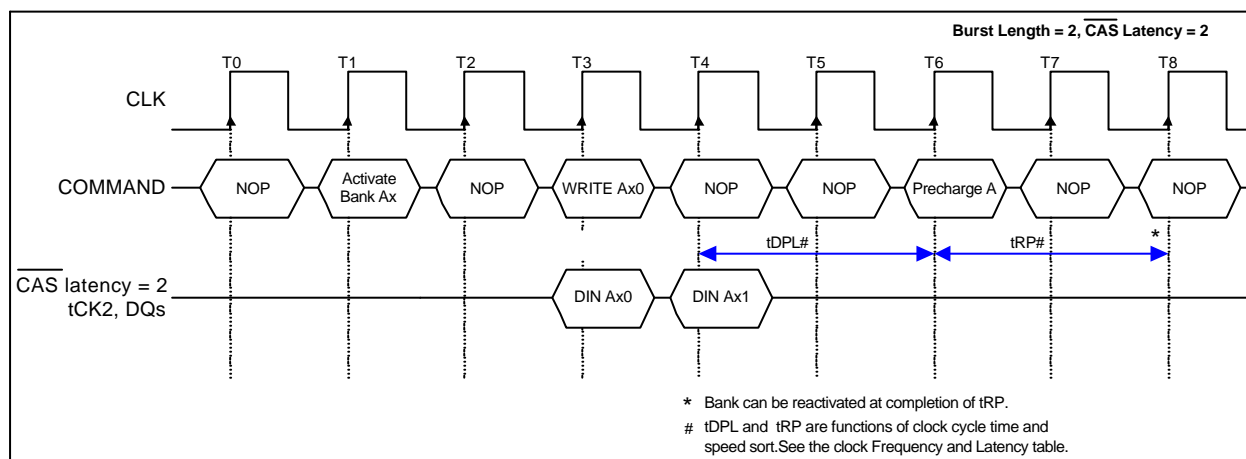| A10 | Bank Select | Precharged Bank(s) |
|-----|-------------|--------------------|
| LOW | BS0, BS1 | Bank defined by BS0, BS1 only |
| HIGH | DON'T CARE | All Banks |

For read cycles, the Precharge Command may be applied (/CAS latency - 1) clocks prior to the last data output. For write cycles, a delay must be satisfied from the start of the last burst write cycle until the Precharge Command can be issued. This delay is known as tDPL, Data-in to Precharge delay.

After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (tRP).
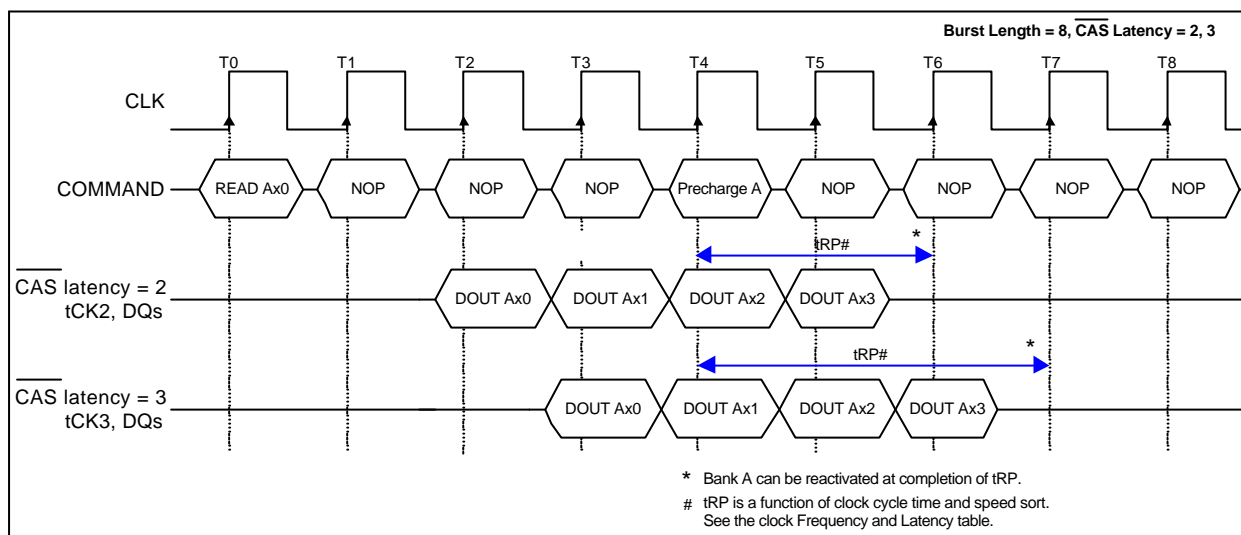
## Burst Read followed by the Precharge Command



**Burst Length = 4, $\overline{CAS}$ Latency = 2**

\* Bank A can be reactivated at completion of tRP.
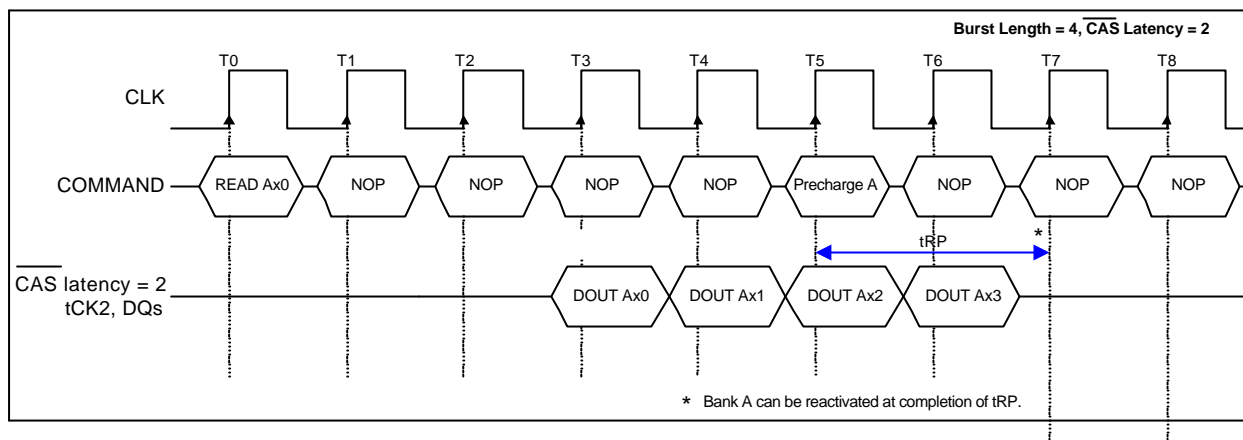
## Burst Write followed by the Precharge Command



**Burst Length = 2, $\overline{CAS}$ Latency = 2**

\* Bank can be reactivated at completion of tRP.

\# tDPL and tRP are functions of clock cycle time and speed sort. See the clock Frequency and Latency table.

## Precharge Termination

The Precharge Command may be used to terminate either a burst read or burst write operation. When the Precharge command is issued, the burst operation is terminated and bank precharge begins. For burst read operations, valid data will continue to appear on the data bus as a function of /CAS Latency.

## Burst Read Interrupted by Precharge



* Bank A can be reactivated at completion of tRP.
# tRP is a function of clock cycle time and speed sort. See the clock Frequency and Latency table.

Burst write operations will be terminated by the Precharge command. The last write data that will be properly stored in the device is that write data that is presented to the device a number of clock cycles prior to the Precharge command equal to the Data-in to Precharge delay, tDPL.

## Precharge Termination of a Burst Write



Burst Length = 8, $\overline{CAS}$ Latency = 2, 3

# tDPL is an asynchronous timing and may be completed in one or two clock cycles depending on clock cycle time .
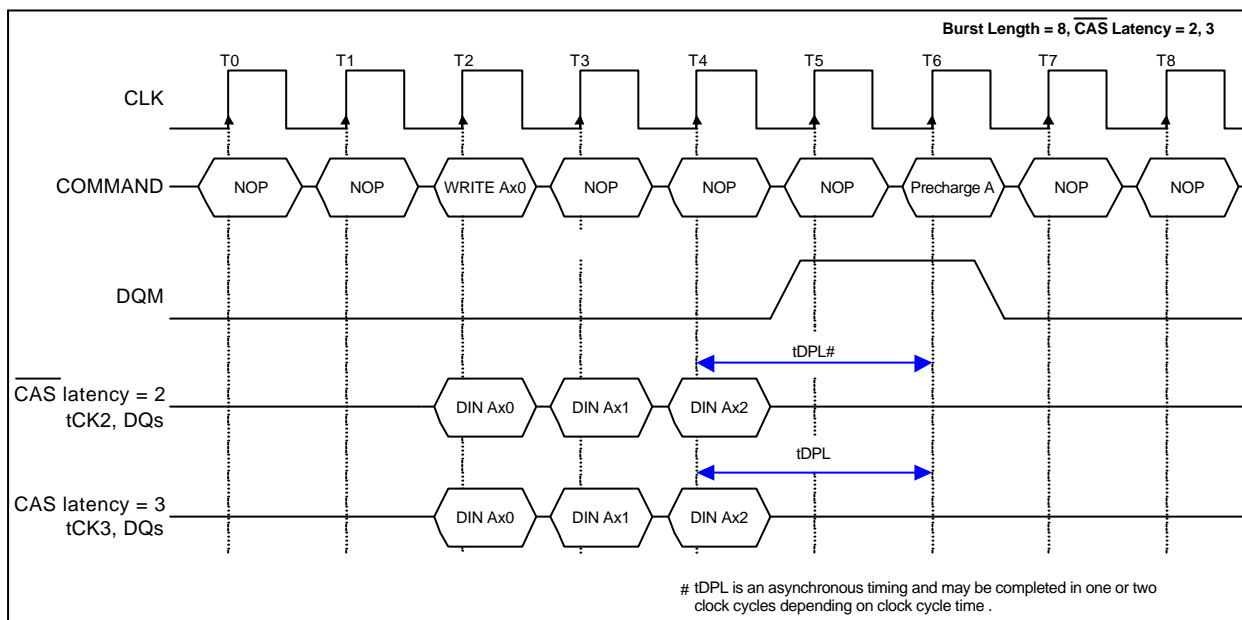
## Automatic Refresh Command ( /CAS before /RAS Refresh)

When /CS, /RAS, and /CAS are held low with CKE and /WE high at the rising edge of the clock, the chip enters the Automatic Refresh mode (CBR). All banks of the SDRAM must be precharged and idle for a minimum of the Precharge time (tRP) before the Auto Refresh Command (CBR) can be applied. For a stacked device, both decks may be refreshed at the same time using Automatic Refresh Mode. An address counter, internal to the device provides the address during the refresh cycle. No control of the external address pins is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Auto Refresh Command (CBR) and the next Activate Command or subsequent Auto Refresh Command must be greater than or equal to the /RAS cycle time (tRC).

## Self Refresh Command

The SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having /CS, /RAS, /CAS, and CKE held low with /WE high at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The user may halt the external clock while the device is in Self Refresh mode, however, the clock must be restarted before the device can exit Self Refresh operation. Once the clock is cycling, the device will exit Self Refresh operation after CKE is returned high. A minimum delay time is required when the device exits Self Refresh Operation and before the next command can be issued. This delay is equal to the /RAS cycle time (tRC) plus the Self Refresh exit time (tSREX). When using Self Refresh, both decks of a stacked device may be refreshed at the same time.

## Power Down Mode

In order to reduce standby power consumption, two power down modes are available: Precharge and Active Power Down mode. To enter Precharge Power Down mode, all banks must be precharged and the necessary precharge delay (tRP) must occur before the SDRAM can enter the power down mode. If a bank is activated but not performing a Read or Write operation, Active Power Down mode will be entered. (Issuing a Power Down Mode Command when the device is performing a Read or Write operation causes the device to enter Clock Suspend mode. See the following section.) Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can't remain in Power Down mode longer than the Refresh period (tREF) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command (or a Device Deselect Command) is required on the next rising clock edge.

## Power Down Mode Exit Timing
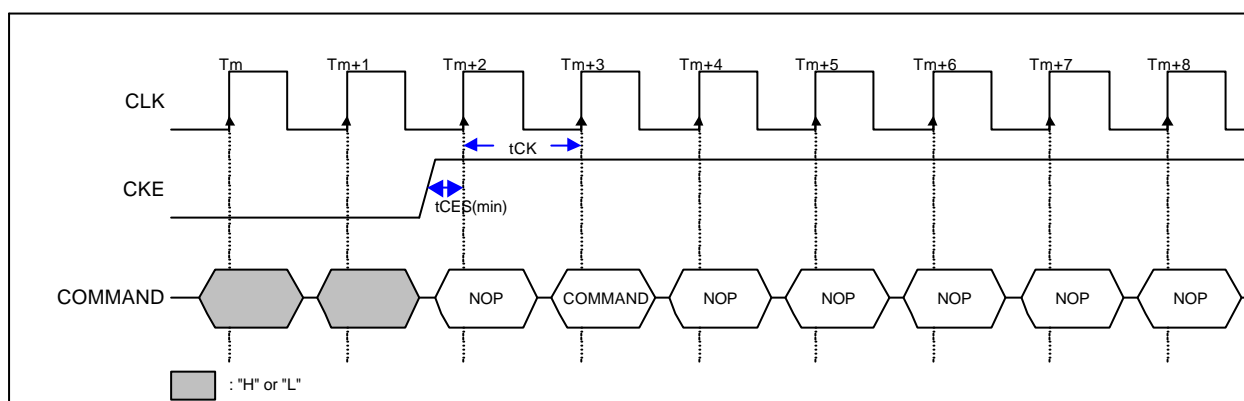


## Data Mask

The SDRAM has a Data Mask function that can be used in conjunction with data read and write cycles. When the Data Mask is activated (DQM high) during a write cycle, the write operation is prohibited immediately (zero clock latency). If the Data Mask is activated during a read cycle, the data outputs are disabled and become high impedance after a two clock delay, independent of /CAS latency.

## Data Mask Activated During a Read Cycle
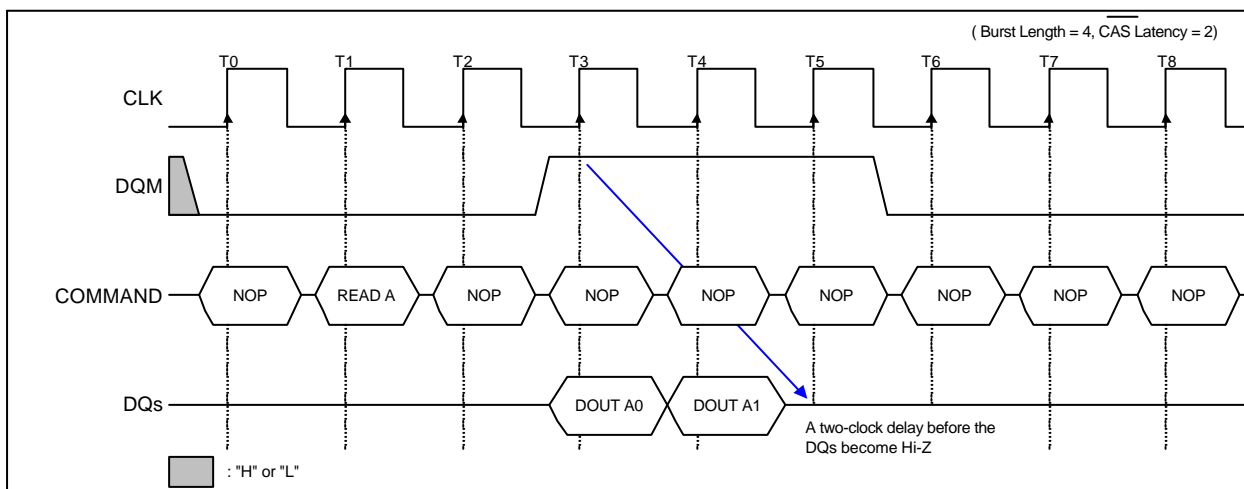
## No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state. The purpose of the No Operation Command is to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when /CS is low with /RAS, /CAS, and /WE held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

## Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when /CS is brought high, the /RAS, /CAS, and /WE signals become don't cares.

## Clock Suspend Mode

During normal access mode, CKE is held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends or "freezes" any clocked operation that was currently being executed. There is a one clock delay between the registration of CKE low and the time at which the SDRAM's operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

When the operation of the SDRAM is suspended during the execution of a Burst Read operation, the last valid data output onto the DQ pins will be actively held valid until Clock Suspend mode is exited.
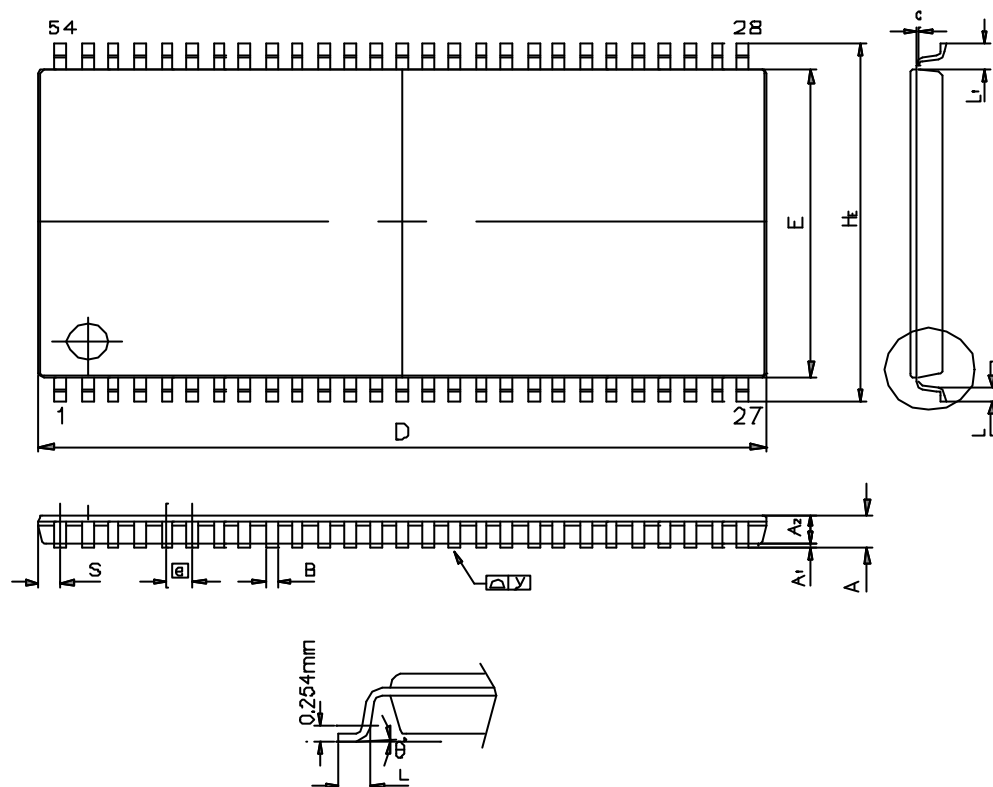
## Clock Suspend During a Read Cycle
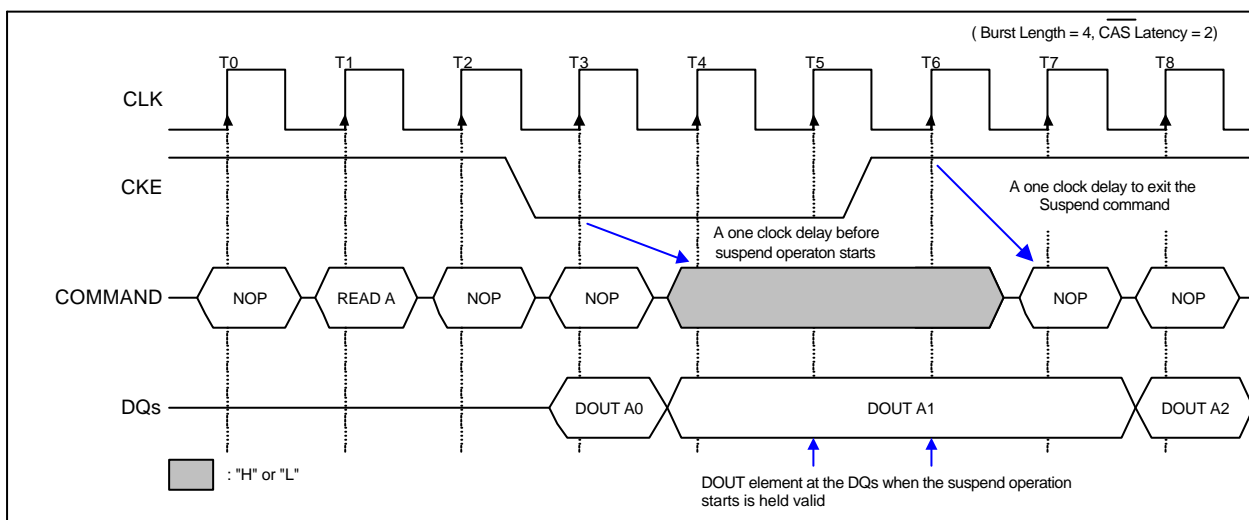


If Clock Suspend mode is initiated during a burst write operation, then the input data is masked and ignored until the Clock Suspend mode is exited.

## Clock Suspend During a Write Cycle



( Burst Length = 4, CAS Latency = 2)
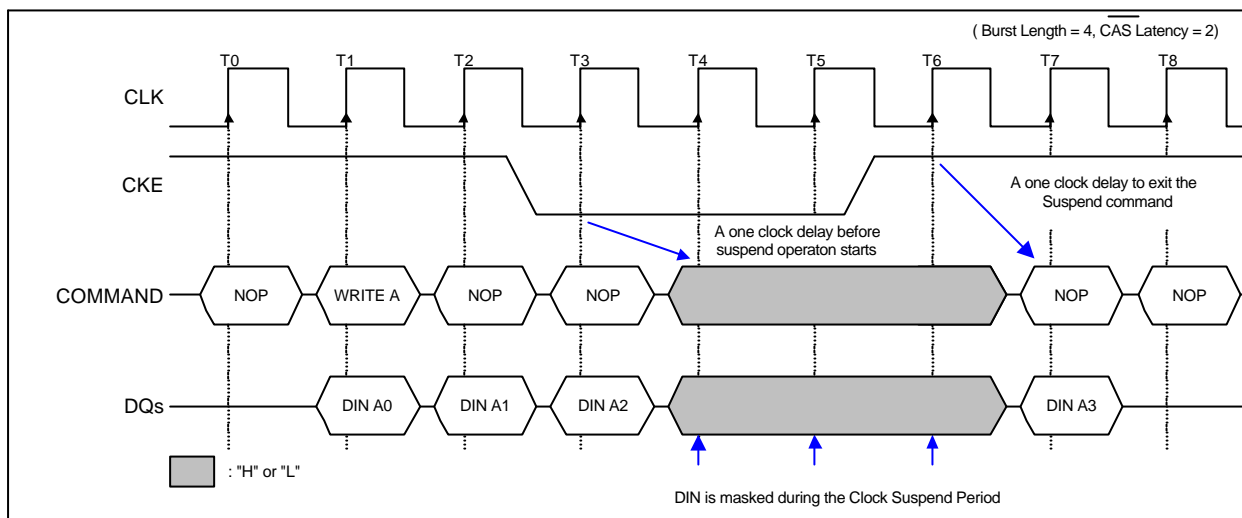
## Package Dimension
( 400 mil; 54 pin; Thin Small Outline Package )



| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | | | 1.20 | | | 0.047 |
| A1 | 0.05 | 0.10 | 0.15 | 0.002 | 0.004 | 0.006 |
| A2 | 0.95 | 1.00 | 1.05 | 0.037 | 0.039 | 0.041 |
| B | 0.30 | 0.35 | 0.45 | 0.012 | 0.014 | 0.018 |
| c | 0.12 | | 0.21 | 0.005 | | 0.008 |
| D | | 22.22 BSC | | | 0.875 BSC | |
| $H_E$ | 11.56 | 11.76 | 11.96 | 0.460 | 0.463 | 0.470 |
| E | 10.03 | 10.16 | 10.29 | 0.390 | 0.400 | 0.410 |
| e | 0.80 BSC | | | 0.031 | | |
| L | 0.40 | 0.50 | 0.60 | 0.016 | 0.020 | 0.024 |
| L1 | | 0.80 REF | | | 0.031 REF | |
| S | | 0.71 REF | | | 0.028 REF | |
| θ | 0 ° | - | 8 ° | 0 ° | - | 8 ° |

## Note:
1. Dimension D odes not include mold protrusions or gate burrs.
2. Mold protrusion and gate burrs shall exceed 0.15 mm per side.
3. Dimension E1 does not include interlead mold protrusions.
4. Interlead mold protrusions shall not exceed 0.25 mm per side.