

NUD3048

FET Switch

100 V, 800 mΩ, N-Channel, TSOP-6

The NUD3048 provides a single device solution for a number of applications requiring a low power, high voltage, FET switch. The package includes a gate resistor and gate to source zener clamp. This switch can accommodate a wide range of input voltages, making it compatible with most current logic levels. Its 100 V rating makes it compatible with 48 V telecom applications.

Features

- 100 V Rating On Gate 2
- Integrated 100 K R_g Option
- Integrated ESD Diode Protection
- Low Threshold Voltage

Typical Applications

- FET Switch
- Inverter
- Level Shifter
- Inrush Limiter
- Relay Driver

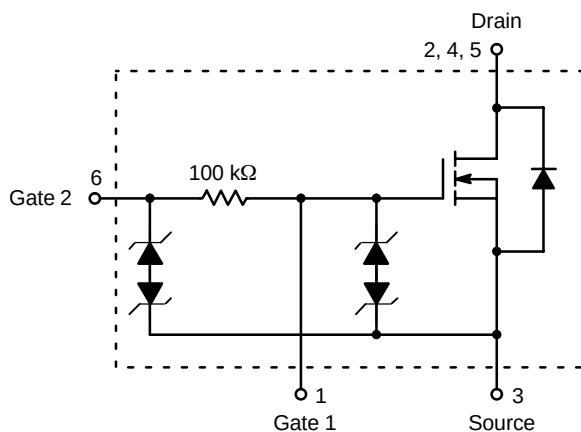


Figure 1. Block Diagram



ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



JW7 = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
NUD3048MT1	TSOP-6	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NUD3048

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{DSS}	Drain to Source Voltage – Continuous	100	V
V_{G1SS}	Gate to Source Voltage – Continuous @ 1.0 mA	15	V
I_D	Drain Current – Continuous	500	mA
V_{G2SS}	Gate Resistor to Source Voltage – Continuous	100	V
T_{Jmax}	Maximum Junction Temperature	150	°C
$R_{\theta JA}$	Thermal Impedance (Junction to Ambient) (Note 1) Thermal Impedance (Junction to Ambient) (Note 2)	190 80	°C/W
ESD	Human Body Model (HBM) Class 2 Machine Model Class A According to EIA/JESD22/A114 Specification	2000 100	V V

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain to Source Leakage Current ($V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$)	I_{DSS}	–	20	100	μA
Gate Body Leakage Current ($V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$) ($V_{GS} = 10\text{ V}$, $V_{DS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$)	I_{GSS} I_{GSS}	– –	3.0 6.0	10 20	μA

ON CHARACTERISTICS

Gate Threshold Voltage ($I_D = 1.0\text{ mA}$)	V_{GS}	1.3	1.7	2.0	V
Drain to Source Resistance ($V_{GS} = 4.5\text{ V}$, $I_D = 100\text{ mA}$)	$R_{DS(on)}$	–	0.65	0.82	Ω
Drain to Source Resistance ($V_{GS} = 10\text{ V}$, $I_D = 100\text{ mA}$)	$R_{DS(on)}$	–	0.6	0.72	Ω

DYNAMIC CHARACTERISTICS

Input Capacitance ($V_{DS} = 5.0\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$)	C_{iss}	–	135	–	pF
Output Capacitance ($V_{DS} = 5.0\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$)	C_{oss}	–	75	–	pF
Transfer Capacitance ($V_{DS} = 5.0\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 10\text{ kHz}$)	C_{rss}	–	26	–	pF

GATE BIAS CHARACTERISTICS

Gate Resistor	R_G	75	100	125	k Ω
Gate Zener Breakdown Voltage ($I_Z = 1.0\text{ mA}$) (Note 3)	V_Z	15	17	–	V
Gate Zener Breakdown Voltage ($I_Z = 3.0\text{ mA}$) (Note 4)		100	115	–	

1. Min pad, 1 oz. Cu.
2. 1 inch pad, 1 oz Cu.
3. Measured from gate 1 to source.
4. Measured from gate 2 to source.

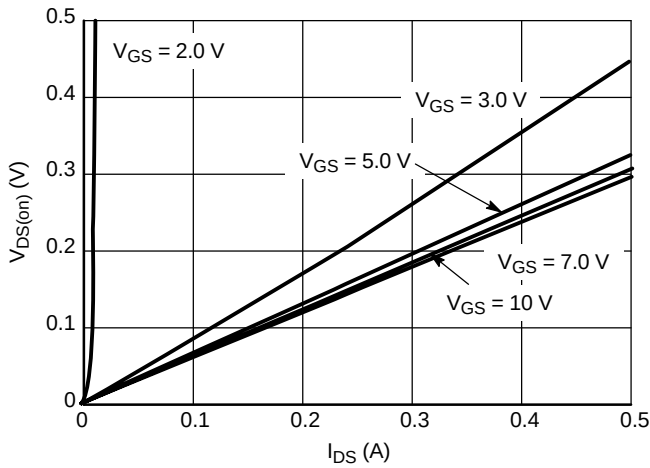


Figure 2. $V_{DS(on)}$ Variation with I_{DS} and Gate Voltage

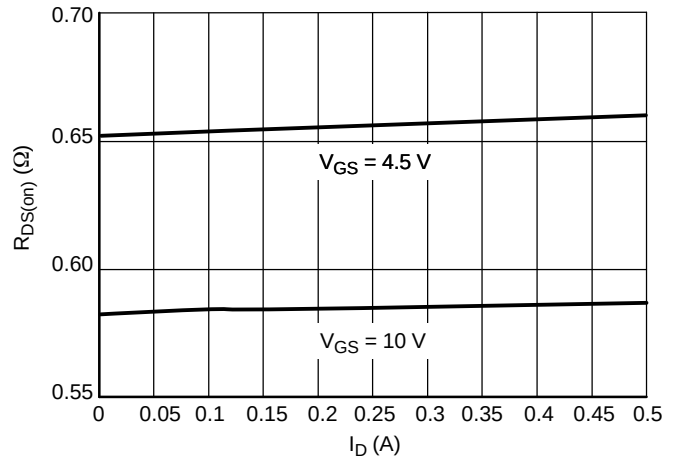


Figure 3. On Resistance Variation with Drain Current and Gate Voltage

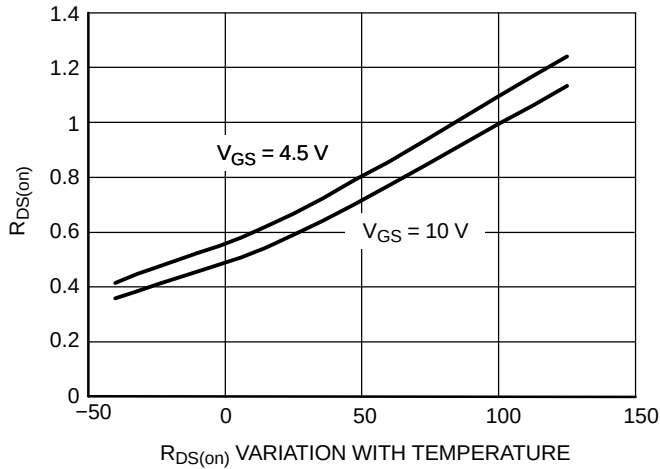


Figure 4. Variation of $R_{DS(on)}$ with Temperature and Gate Voltage at $I_D = 100$ mA

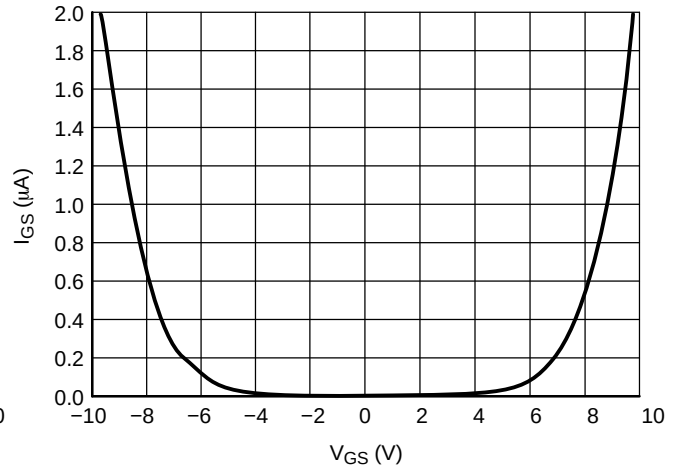


Figure 5. Gate Leakage Current Variation with Gate Voltage

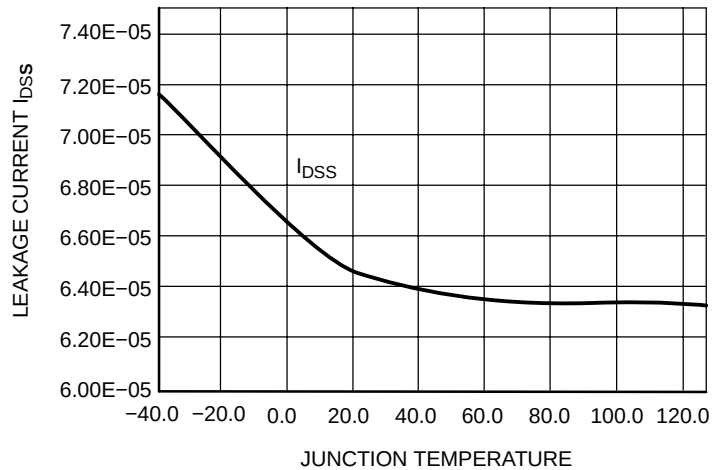
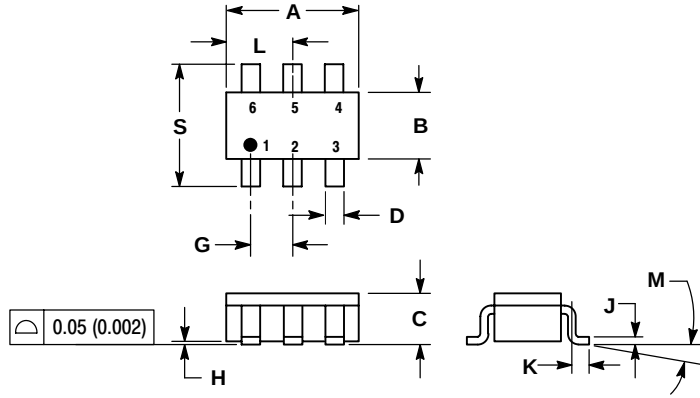


Figure 6. Variation of Leakage Current I_{DSS} (A) with $V_{GS} = 0$ V and $V_{DS} = 100$ V

NUD3048

PACKAGE DIMENSIONS

TSOP-6 CASE 318G-02 ISSUE L



NOTES:

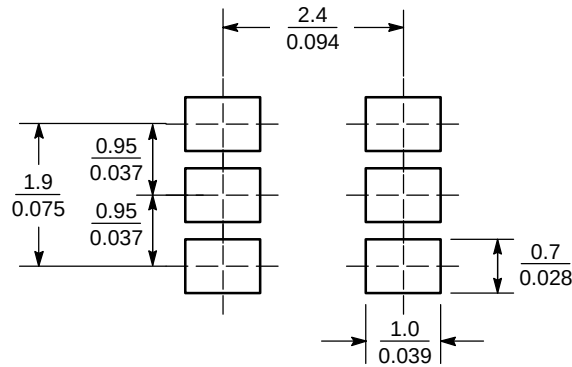
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0°	10°	0°	10°
S	2.50	3.00	0.0985	0.1181

STYLE 9:

- PIN 1: LOW VOLTAGE GATE
- DRAIN
- SOURCE
- DRAIN
- DRAIN
- HIGH VOLTAGE GATE

SOLDERING FOOTPRINT



TSOP-6 SCALE 10:1 (mm / inches)

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.