PRELIMINARY DATA SHEET

NEC

LDMOS FIELD EFFECT TRANSISTOR
NEM090303M-28

N-CHANNEL SILICON POWER MOS FET FOR UHF-BAND POWER AMPLIFIER

DESCRIPTION

The NEM090303M-28 is an N-channel enhancement-mode lateral MOS FET designed for driver stage in 0.5 to 1.0 GHz PA, such as, analog/digital TV-transmitter and GSM/D-AMPS/PDC cellular base station amplifiers. Dies are manufactured using our NEWMOS technology (our WSi gate lateral MOS FET), and its nitride surface passivation and triple layer aluminum silicon metalization offer a high degree of reliability.

FEATURES

- High 1 dB compression output power : $P_{O\ (1\ dB)}$ = 40 W TYP. (V_{DS} = 28 V, I_{Dset} = 250 mA, f = 960 MHz)
- High linear gain : G_L = 20.0 dB TYP. (V_{DS} = 28 V, I_{Dset} = 250 mA, f = 960 MHz)
- High drain efficiency : η_d = 63% TYP. (V_{DS} = 28 V, I_{Dset} = 250 mA, f = 960 MHz)
- Low intermodulation distortion : IM_3 = –42 dBc TYP. (V_{DS} = 28 V, I_{Dset} = 250 mA, f = 960, 961 MHz, P_{out} = 36 dBm (2 tones))
- Excellent thermal stability
- Low cost hollow plastic packages
- Integrated ESD protection
- Excellent stability against HCI

APPLICATIONS

- Digital cellular base station PA : GSM/D-AMPS/PDC/N-CDMA etc.
- UHF-band TV-transmitter PA

ORDERING INFORMATION

Part Number	Package
NEM090303M-28	3M (T-91M)

Remark To order evaluation samples, contact your nearby sales office.
The unit sample quantity is 1 pcs.

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DS}	65	V
Gate to Source Voltage	V_{GSO}	±7	V
Drain Current	I_D	8	A
Total Device Dissipation	P_D	79.5	W
Input Power	P_{in} Note	2.2	W
Channel Temperature	T_{ch}	200	°C
Storage Temperature	T_{stg}	–65 to +150	°C

Note f = 960 MHz, V_{DS} = 28 V

THERMAL RESISTANCE (T_A = +25°C)

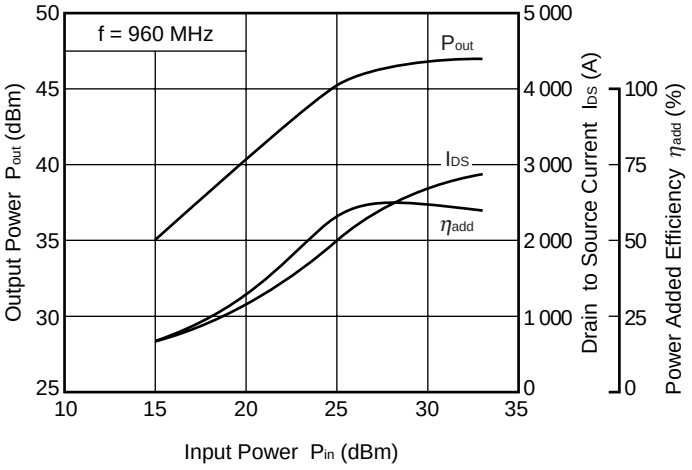
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Channel to Case Resistance	$R_{th\ (ch-c)}$	–	2.0	2.2	°C/W

ELECTRICAL CHARACTERISTICS (T_A = +25°C)

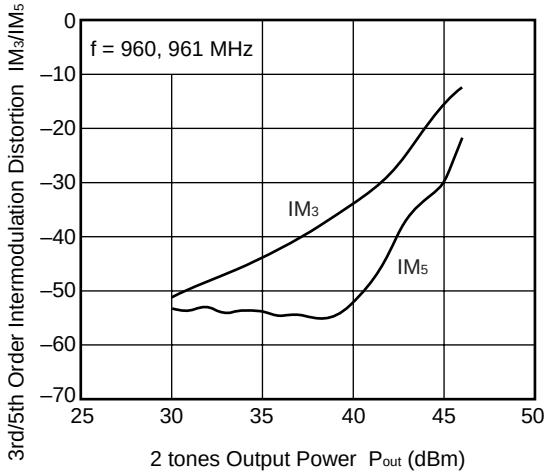
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
DC Characteristics						
Gate to Source Leak Current	I_{GSO}	V_{GS} = 5V	–	–	1	μA
Saturated Drain Current	I_{DSS}	V_{DS} = 65 V	–	–	1	mA
Gate Threshold Voltage	V_{th}	V_{DS} = 10 V, I_{DS} = 1 mA	1.0	1.4	2.0	V
Transconductance	g_m	V_{DS} = 28 V, I_{DS} = 250 mA	–	1.8	–	S
Drain to Source Breakdown Voltage	BV_{DS}	I_{DSS} = 10 μA	65	75	–	V
RF Characteristics						
Gain 1 dB Compression Output Power	$P_{O\ (1\ dB)}$	f = 960 MHz, V_{DS} = 28 V,	–	46	–	dBm
Linear Gain	G_L	I_{Dset} = 250 mA	18.5	20	–	dB
Output Power	P_{out}	f = 960 MHz, V_{DS} = 28 V,	45	46.5	–	dBm
Drain Efficiency	η_d	I_{Dset} = 250 mA, P_{in} = 28 dBm	50	63	–	%
Power Added Efficiency	η_{add}		–	62	–	%
3rd Order Intermodulation Distortion	IM_3	f = 960, 961 MHz, V_{DS} = 28 V, I_{Dset} = 250 mA, 2 tones P_{out} = 36 dBm	–	–42	–	dBc

TYPICAL CHARACTERISTICS (T_A = +25°C, V_{DS} = 28 V, I_{Dset} = 250 mA)

OUTPUT POWER, DRAIN TO SOURCE CURRENT, POWER ADDED EFFICIENCY vs. INPUT POWER

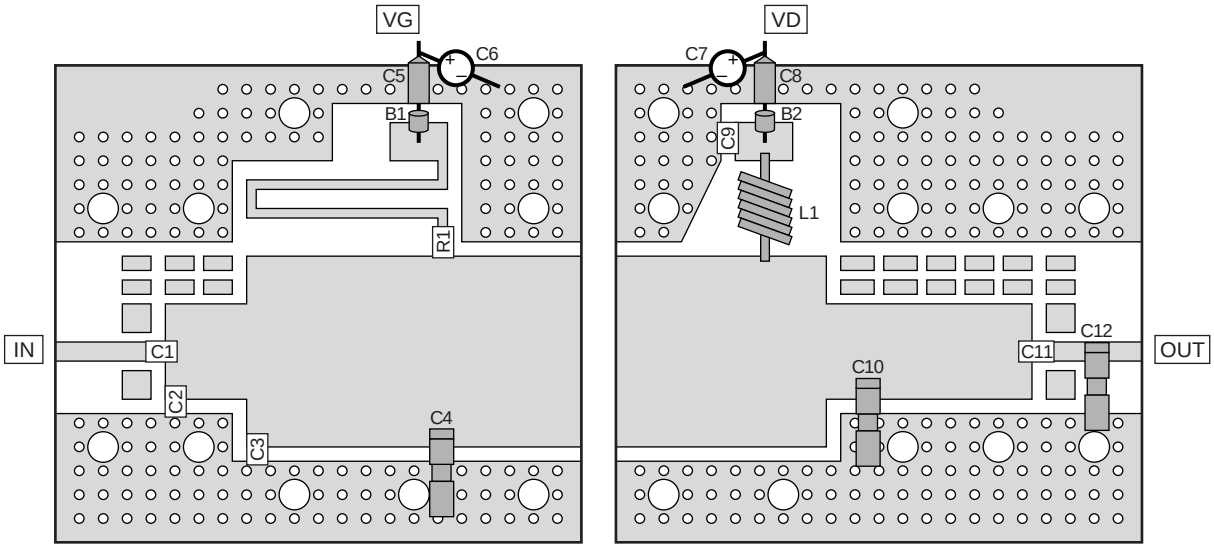


3RD/5TH ORDER INTERMODULATION DISTORTION vs. 2 TONES OUTPUT POWER

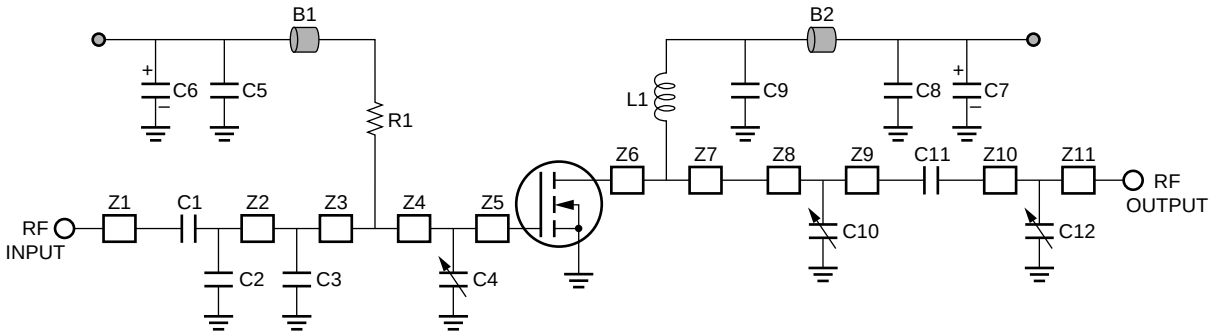


Remark The graphs indicate nominal characteristics.

COMPONENT LAYOUT OF TEST CIRCUIT FOR 850 TO 900 MHz

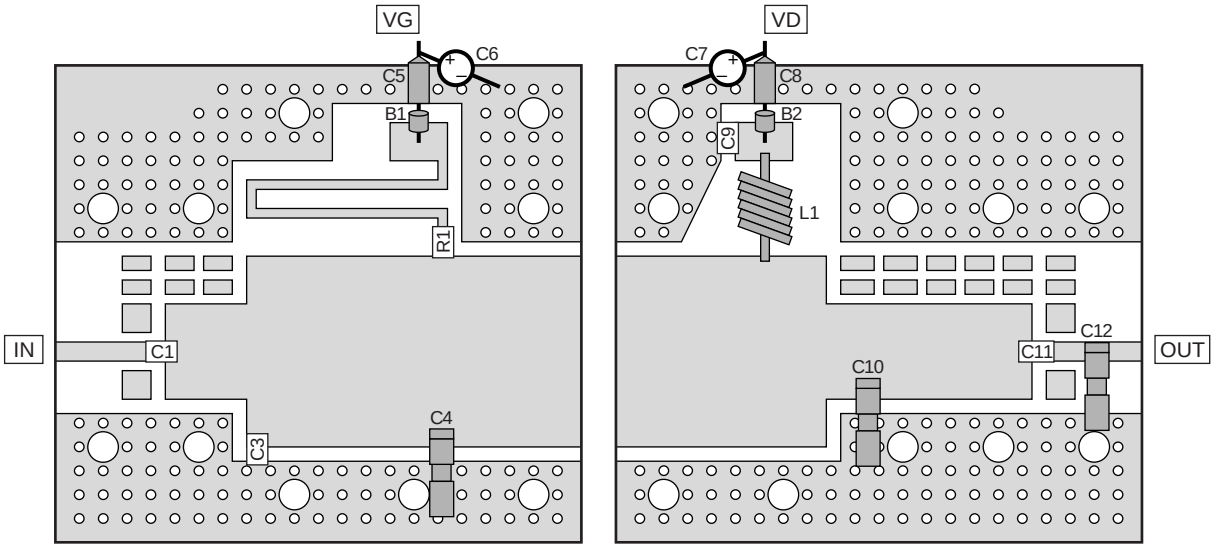


TEST CIRCUIT SCHEMATIC FOR 850 TO 900 MHz

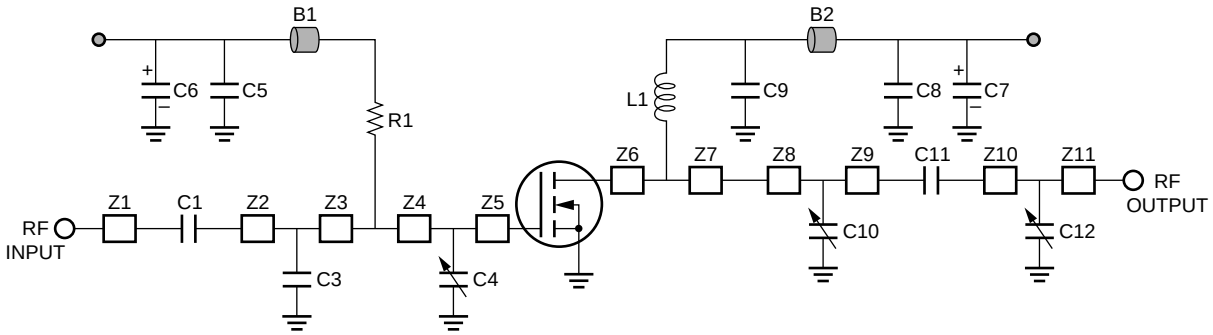


Symbol	Value	Symbol	Value
B1, B2	Ferrite bead	Z1	Line, 10.0 × 2.0 mm
C1, C11	20 pF chip capacitor	Z2	Line, 8.0 × 10.0 mm
C2, C3	2 pF chip capacitor	Z3	Line, 20.5 × 20.0 mm
C4, C10, C12	Variable capacitor: 0.8 to 8 pF	Z4	Line, 3.0 × 20.0 mm
C5, C8	EMI suppression filter 1 000 pF	Z5	Line, 11.5 × 20.0 mm
C6, C7	47 μF Electrolytic capacitor	Z6	Line, 10.0 × 20.0 mm
C9	0.47 nF chip capacitor × 2	Z7	Line, 12.0 × 20.0 mm
L1	Coil (1.0 mm × 5 to 7 turn)	Z8	Line, 4.5 × 10.0 mm
R1	2 000 Ω chip resistor	Z9	Line, 15.5 × 10.0 mm
Circuit Board	Teflon, Er = 2.6, Thickness 0.8 mm	Z10, Z11	Line, 5.0 × 2.0 mm

COMPONENT LAYOUT OF TEST CIRCUIT FOR 920 TO 960 MHz



TEST CIRCUIT SCHEMATIC FOR 920 TO 960 MHz



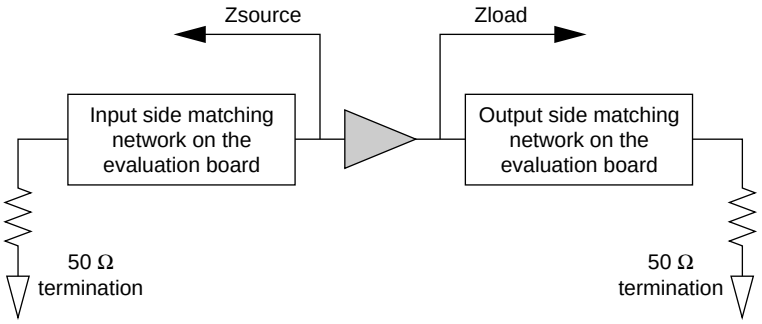
Symbol	Value	Symbol	Value
B1, B2	Ferrite bead	Z1	Line, 10.0 × 2.0 mm
C1, C11	20 pF chip capacitor	Z2	Line, 8.0 × 10.0 mm
C3	2 pF chip capacitor	Z3	Line, 20.5 × 20.0 mm
C4, C10, C12	Variable capacitor: 0.8 to 8 pF	Z4	Line, 3.0 × 20.0 mm
C5, C8	EMI suppression filter 1 000 pF	Z5	Line, 11.5 × 20.0 mm
C6, C7	47 μF Electrolytic capacitor	Z6	Line, 10.0 × 20.0 mm
C9	0.47 nF chip capacitor × 2	Z7	Line, 12.0 × 20.0 mm
L1	Coil (1.0 mm × 5 to 7 turn)	Z8	Line, 4.5 × 10.0 mm
R1	2 000 Ω chip resistor	Z9	Line, 15.5 × 10.0 mm
Circuit Board	Teflon, Er = 2.6, Thickness 0.8 mm	Z10, Z11	Line, 5.0 × 2.0 mm

LARGE SIGNAL IMPEDANCE OF TEST BOARD FOR 850 TO 900 MHz

Measurement Condition: V_{DS} = 28 V, I_{Dset} = 250 mA

f (MHz)	Z_{in} (Ω)	Z_{out} (Ω)
850	1.33–j0.86	2.26–j2.33
860	1.33–j1.00	2.23–j2.56
870	1.33–j1.13	2.35–j2.82
880	1.33–j1.29	2.38–j3.11
890	1.33–j1.39	2.47–j3.31
900	1.34–j1.51	2.52–j3.55

Remark Z_{in} = Conjugate of Zsource, Z_{out} = Conjugate of Zload



S-PARAMETERS

S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

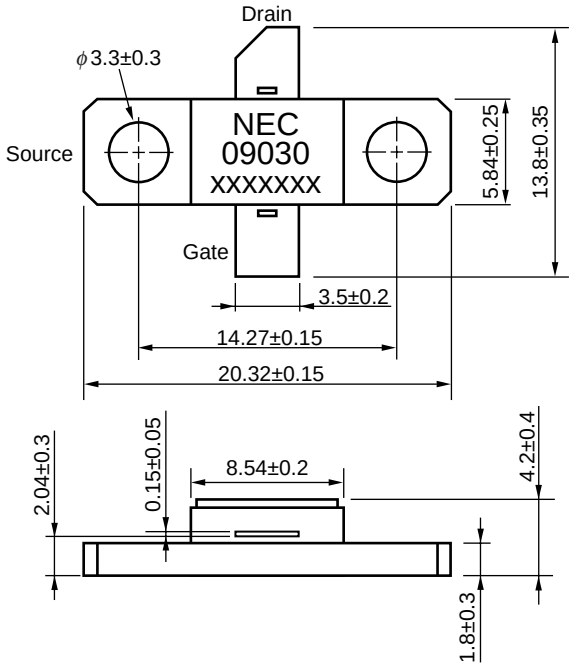
Click here to download S-parameters.

[RF and Microwave] → [Device Parameters]

URL http://www.csd-nec.com/

PACKAGE DIMENSIONS

3M (T-91M) (UNIT: mm)



RECOMMENDED MOUNTING CONDITIONS FOR CORRECT USE

(1) Fix to a heat sink or mount surface completely with screws at the two holes of the flange.

(2) The recommended torque strength of the screws is 29.4 N·cm typical using M3 type screws.

(3) The recommended flatness of the mount surface is less than ±10 μm (roughness of surface is $\nabla\nabla\nabla$).

RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions		Condition Symbol
Partial Heating	Peak temperature (pin temperature) Soldering time (per pin of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350-P3

Caution Do not use different soldering methods together (except for partial heating).

- **The information in this document is current as of February, 2003. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC's data sheets or data books, etc., for the most up-to-date specifications of NEC semiconductor products. Not all products and/or types are available in every country. Please check with an NEC sales representative for availability and additional information.**
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  (2) "NEC semiconductor products" means any semiconductor product developed or manufactured by or for NEC (as defined above).

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