SaRonix

Crystal Clock Oscillator — 3.3 & 5V, HCMOS, TTL, SMD

Technical Data — NTH / NTT Series, Type H

ACTUAL SIZE

Description

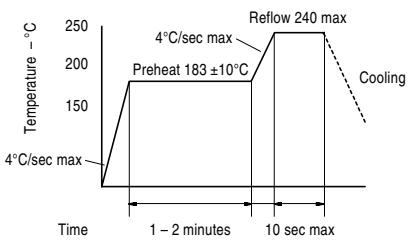
A crystal controlled, 3.3 or 5 volt, low current oscillator designed to drive low power, high performance microprocessors. The plastic-molded surface mountable package is ideal for today's automated assembly environments. J-leads are compatible with EIA standard footprints. The HCMOS device is capable of driving both CMOS and TTL loads.

Applications & Features

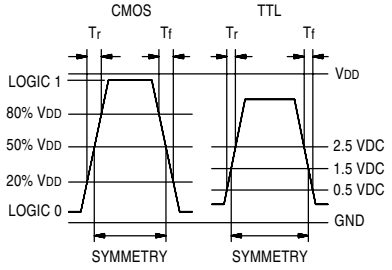
- Footprint compatible and direct replacement for SG615 series
- Frequency range from 1 to 70 MHz
- 3.3V and 5V versions
- Tri-State output standard
- Low voltage CMOS, HCMOS and TTL compatible
- Ideally suited for use with contemporary MPUs and custom ASICs
- Perfect for PCs, laptop, portable applications; disc drives - anywhere small size, low power and surface mountability are a priority
- Matches EIA standard SO-J-20 footprint
- Compact, plastic-molded, surface mountable package
- Available on tape & reel; 24mm tape, 1000pcs per reel

Frequency Range:	1 MHz to 70 MHz		
Frequency Stability:	±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.		
Temperature Range:			
Operating:	0°C to +70°C or -40°C to +85°C		
Storage:	-55°C to +125°C		
Supply Voltage:			
Recommended Operating:	5V ±10% or 3.3V ±10% (HCMOS only)		
Supply Current:	5V, 10TTL/30pF	5V, 50pF	@ 3.3V
1 MHz to 26 MHz:	15mA max	35mA max	15mA max
26+ MHz to 50 MHz:	30mA max	45mA max	20mA max
50+ MHz to 70 MHz:	45mA max		25mA max
Output Drive:			
HCMOS			
Symmetry:	40/60% or 45/55% max @ 50% V_{DD}, See Part Numbering Guide		
Rise & Fall Times:	8ns max 20% to 80% V_{DD} @ 5V 5ns max 20% to 80% V_{DD} @ 3.3V		
Logic 0:	10% V_{DD} max or 0.4V max @ 3.3V		
Logic 1:	90% V_{DD} min or V_{DD} -0.4 min @ 3.3V		
Load:	50 pF max to 50 MHz, 30 pF 50+ to 70 MHz, 15 pF @ 3.3V operation		
Period Jitter RMS:	8ps max		
TTL (5V)			
Symmetry:	40/60% or 45/55% max @ 1.5V level, See Part Numbering Guide		
Rise & Fall Times:	8ns max 0.5 to 2.5V		
Logic 0:	0.5V max		
Logic 1:	2.5V min		
Load:	10 TTL to 50 MHz, 5 TTL 50+ to 70 MHz		
Period Jitter RMS:	8ps max		
Mechanical:			
Shock:	MIL-STD-883, Method 2002, Condition B		
Solderability:	MIL-STD-883, Method 2003		
Terminal Strength:	MIL-STD-883, Method 2004, Condition B2		
Vibration:	MIL-STD-883, Method 2007, Condition A		
Solvent Resistance:	MIL-STD-202, Method 215		
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition I or J		
Environmental:			
Thermal Shock:	MIL-STD-883, Method 1011, Condition A		
Moisture Resistance:	MIL-STD-883, Method 1004		

Solder Reflow Guide



Output Waveform



DS-111 REV J

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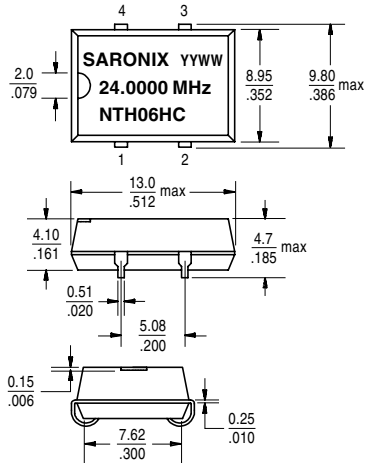
Tri-State Logic Table

Pin 1 Input	Pin 3 Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 1:
Logic 1 = 2.0V min
Logic 0 = 0.8V max or 0.2V max @ 3.3V

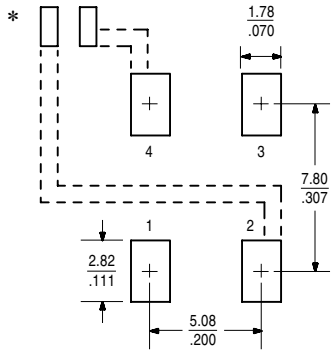
Package Details, Type H



Pin Function:

Pin 1: Tri-State Control
Pin 2: GND
Pin 3: Output
Pin 4: +5 VDC

Recommended Land Pattern



*External high frequency power supply decoupling required.

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

NTH 0 6 H C - 24.0000 (T)

Series
NTH = CMOS - compatible
NTT = TTL - compatible (5V only)

Symmetry
0 = 40/60% max, 0 to +70°C
A = 45/55% max, 0 to +70°C
2 = 40/60% max, -40 to +85°C, 5V: 70 MHz max, 3.3V: 64 MHz max
4 = 45/55% max, -40 to +85°C, 50 MHz max

Frequency Range
3 = 1.0 to 4 MHz
6 = 4+ to 24 MHz
8 = 24+ to 70 MHz

Package Type H

Stability Tolerance
C = ±100 ppm
B = ±50 ppm

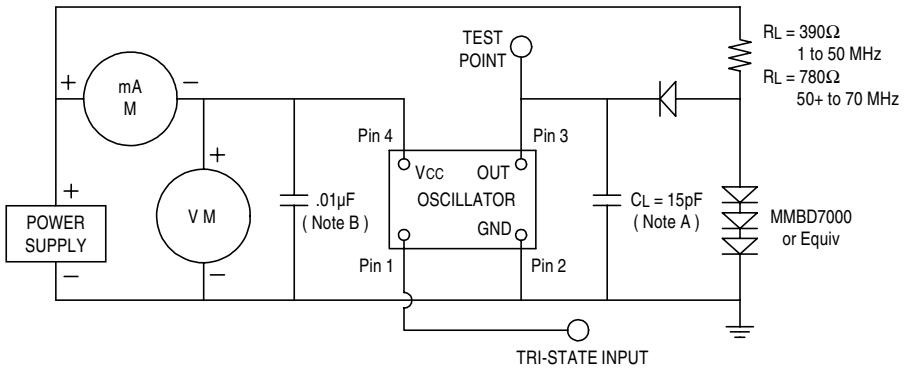
Supply Voltage
Blank = 5V operation
3 = 3.3V, 69.1 MHz max, 0 to +70°C
64 MHz max, -40 to +85°C

Frequency

(T) = Tape & Reel
full reel increments only

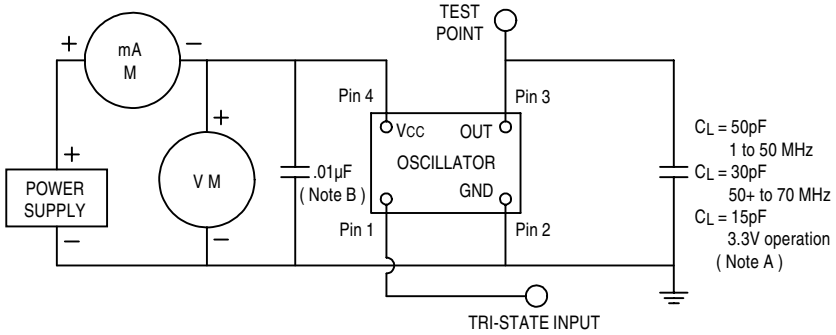
Example PN: NTH06HC - 24.0000 (T)

Test Circuits



NOTE: A. C_L includes probe and fixture capacitance.
NOTE: B. An external .01µF bypass capacitor close to package ground and V_{CC} pin is required

FIGURE 1 - TTL TEST CIRCUIT, 5V OPERATION



NOTE: A. C_L includes probe and fixture capacitance.
NOTE: B. An external .01µF bypass capacitor close to package ground and V_{CC} pin is required

FIGURE 2 - HCMOS TEST CIRCUIT, 3.3V OR 5V OPERATION

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