

# HETERO JUNCTION FIELD EFFECT TRANSISTOR

## NE32500, NE27200

### C to Ka BAND SUPER LOW NOISE AMPLIFIER N-CHANNEL HJ-FET CHIP

#### DESCRIPTION

NE32500 and NE27200 are Hetero Junction FET chip that utilizes the hetero junction between Si-doped AlGaAs and undoped InGaAs to create high mobility electrons. Its excellent low noise and high associated gain make it suitable for commercial systems, industrial and space applications.

#### FEATURES

- Super Low Noise Figure & High Associated Gain  
NF = 0.45 dB TYP.,  $G_a = 12.5$  dB TYP. at  $f = 12$  GHz
- Gate Length:  $L_g = 0.2 \mu\text{m}$
- Gate Width :  $W_g = 200 \mu\text{m}$

#### ORDERING INFORMATION

PART NUMBER	QUALITY GRADE
NE32500	Standard (Grade D)
NE27200	Special, specific (Grade C and B)

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

Drain to Source Voltage	$V_{DS}$	4.0	V
Gate to Source Voltage	$V_{GS}$	-3.0	V
Drain Current	$I_D$	$I_{DSS}$	mA
Total Power Dissipation	$P_{tot}^*$	200	mW
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to +175	$^\circ\text{C}$

\* Chip mounted on a Alumina heatsink (size:  $3 \times 3 \times 0.6^t$ )

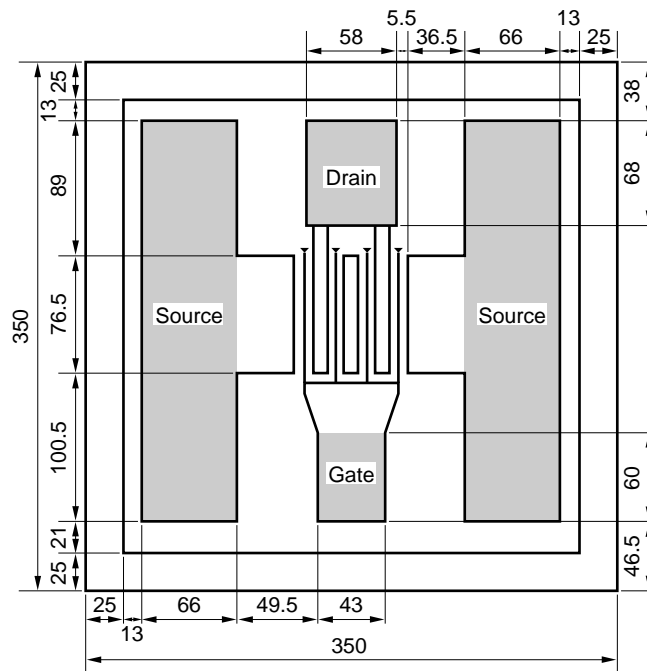
#### ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Gate to Source Leak Current	$I_{GSO}$	-	0.5	10	$\mu\text{A}$	$V_{GS} = -3 \text{ V}$
Saturated Drain Current	$I_{DSS}$	20	60	90	mA	$V_{DS} = 2 \text{ V}, V_{GS} = 0 \text{ V}$
Gate to Source Cutoff Voltage	$V_{GS(off)}$	-0.2	-0.7	-2.0	V	$V_{DS} = 2 \text{ V}, I_D = 100 \mu\text{A}$
Transconductance	$g_m$	45	60	-	mS	$V_{DS} = 2 \text{ V}, I_D = 10 \text{ mA}$
Thermal Resistance	$R_{th}^*$	-	-	260	$^\circ\text{C/W}$	channel to case
Noise Figure	NF	-	0.45	0.55	dB	$V_{DS} = 2 \text{ V}, I_D = 10 \text{ mA}, f = 12 \text{ GHz}$
Associated Gain	$G_a$	11.0	12.5	-	dB	

RF performance is determined by packaging and testing 10 chips per wafer.

Wafer rejection criteria for standard devices is 2 rejects per 10 samples.

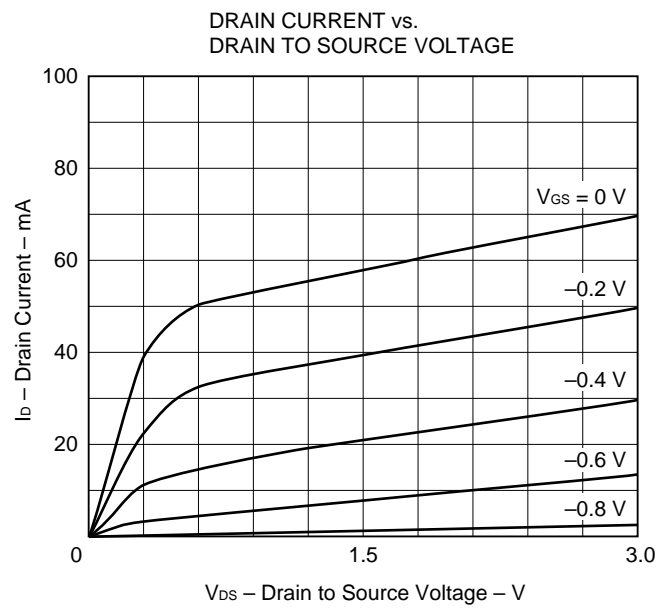
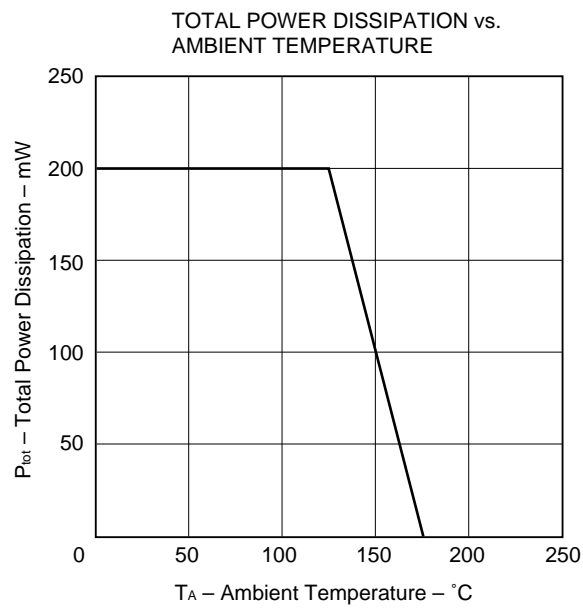
**CHIP DIMENSIONS** (Unit:  $\mu\text{m}$ )

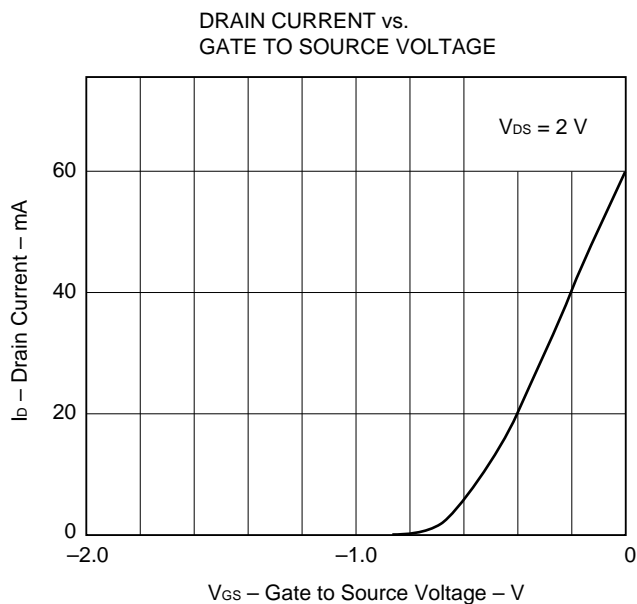


Thickness = 140  $\mu\text{m}$

■ : BONDING AREA

**TYPICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ )





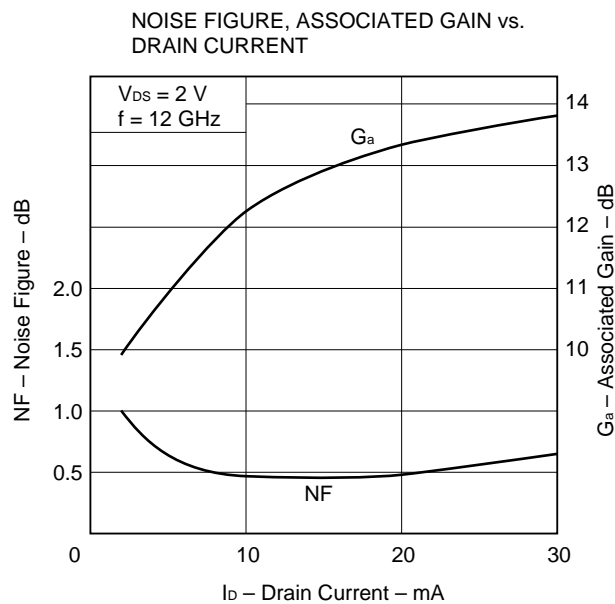
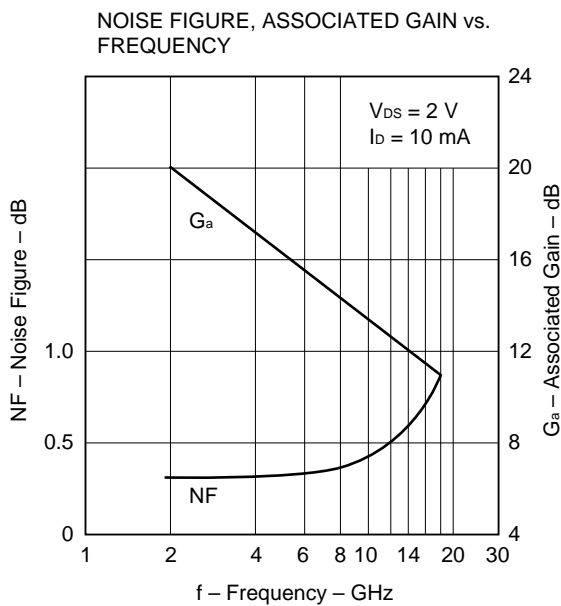
### Gain Calculations

$$MSG. = \frac{|S_{21}|}{|S_{12}|}$$

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{12}| |S_{21}|}$$

$$MAG. = \frac{|S_{21}|}{|S_{12}|} (K \pm \sqrt{K^2 - 1})$$

$$\Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$



**S-PARAMETERS MAG. AND ANG.** $V_{DS} = 2 \text{ V}$ ,  $I_D = 10 \text{ mA}$ 

FREQUENCY (MHz)	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAG.	ANG. (deg.)	MAG.	ANG. (deg.)	MAG.	ANG. (deg.)	MAG.	ANG. (deg.)
500	0.999	-4	4.34	177	0.006	82	0.564	-3
1000	0.998	-7	4.33	174	0.012	84	0.562	-6
2000	0.996	-14	4.28	168	0.025	81	0.559	-11
3000	0.992	-20	4.26	163	0.037	76	0.557	-17
4000	0.976	-28	4.24	158	0.048	71	0.551	-23
5000	0.962	-36	4.11	152	0.060	66	0.546	-29
6000	0.962	-42	4.06	148	0.070	62	0.539	-34
7000	0.943	-48	3.95	143	0.079	58	0.533	-40
8000	0.928	-55	3.83	139	0.087	55	0.526	-44
9000	0.920	-60	3.73	134	0.095	51	0.519	-49
10000	0.900	-67	3.58	129	0.104	47	0.508	-54
11000	0.881	-72	3.46	126	0.109	43	0.503	-58
12000	0.869	-77	3.34	122	0.114	40	0.494	-62
13000	0.856	-82	3.23	118	0.120	37	0.488	-66
14000	0.839	-86	3.11	115	0.123	34	0.483	-69
15000	0.831	-91	3.01	112	0.127	32	0.476	-72
16000	0.818	-96	2.88	108	0.131	29	0.472	-76
17000	0.804	-99	2.78	105	0.134	27	0.468	-79
18000	0.796	-103	2.68	103	0.137	24	0.464	-81
19000	0.784	-106	2.59	100	0.141	22	0.460	-84
20000	0.782	-111	2.49	96	0.142	20	0.456	-88
21000	0.772	-114	2.42	95	0.144	19	0.457	-90
22000	0.761	-117	2.33	93	0.147	17	0.450	-92
23000	0.758	-119	2.25	90	0.147	15	0.454	-94
24000	0.753	-122	2.20	88	0.148	14	0.453	-95
25000	0.748	-125	2.11	86	0.150	12	0.453	-98
26000	0.746	-127	2.06	84	0.152	11	0.460	-100
27000	0.750	-129	2.01	82	0.154	9	0.453	-101
28000	0.738	-133	1.93	79	0.151	7	0.453	-104
29000	0.744	-135	1.90	77	0.153	7	0.453	-105
30000	0.742	-138	1.84	75	0.156	4	0.454	-107

## CHIP HANDLING

### DIE ATTACHMENT

Die attach operation can be accomplished with Au-Sn (within a 300 °C – 10 s) performs in a forming gas environment.

Epoxy die attach is not recommend.

### BONDING

Bonding wires should be minimum length, semi hard gold wire (3-8 % elongation) 20 microns in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Bonding time should be kept to minimum.

As a general rule, the bonding operation should be kept within a 280 °C, 2 minutes for all bonding wires.

If longer periods are required, the temperature should be lowered.

### PRECAUTIONS

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

Avoid high static voltage and electric fields, because this device is Hetero Junction field effect transistor with shottky barrier gate.

## CAUTION

**The Great Care must be taken in dealing with the devices in this guide.**

**The reason is that the material of the devices is GaAs (Gallium Arsenide), which is designated as harmful substance according to the law concerned.**

**Keep the law concerned and so on, especially in case of removal.**

[MEMO]

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Anti-radioactive design is not implemented in this product.