

14-CHARACTER 1-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6624C is a Dot Matrix LCD controller driver for 14-character 1-line with icon display in single chip.

It contains bleeder resistance, general output port, keyscan circuit, CR oscillator, microprocessor interface circuit, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers, and others.

The character generator ROM consisting of 7,840 bits stores 224 kinds of character Font. Each 1,120 bits CG RAM and Icon display RAM can store 32 kinds of special character displayed on the dot matrix display area or 70 kinds of Icon on the Icon display area.

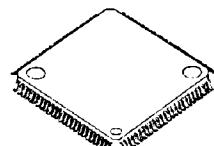
The 8-common (7 for character, 1 for icon) and 70-segment drivers operate 14-character 1-line with 70 Icon LCD display and LED driver drives 4 LED which can use like as indicator.

The 16th display contrast control function is incorporated. Therefore, the contrast adjustment is operated easily by only simple power supply circuit on-chip.

The complete CR oscillator requires no external components.

The serial interface which operates by 1MHz, communicates with external MCUs.

■ PACKAGE OUTLINE



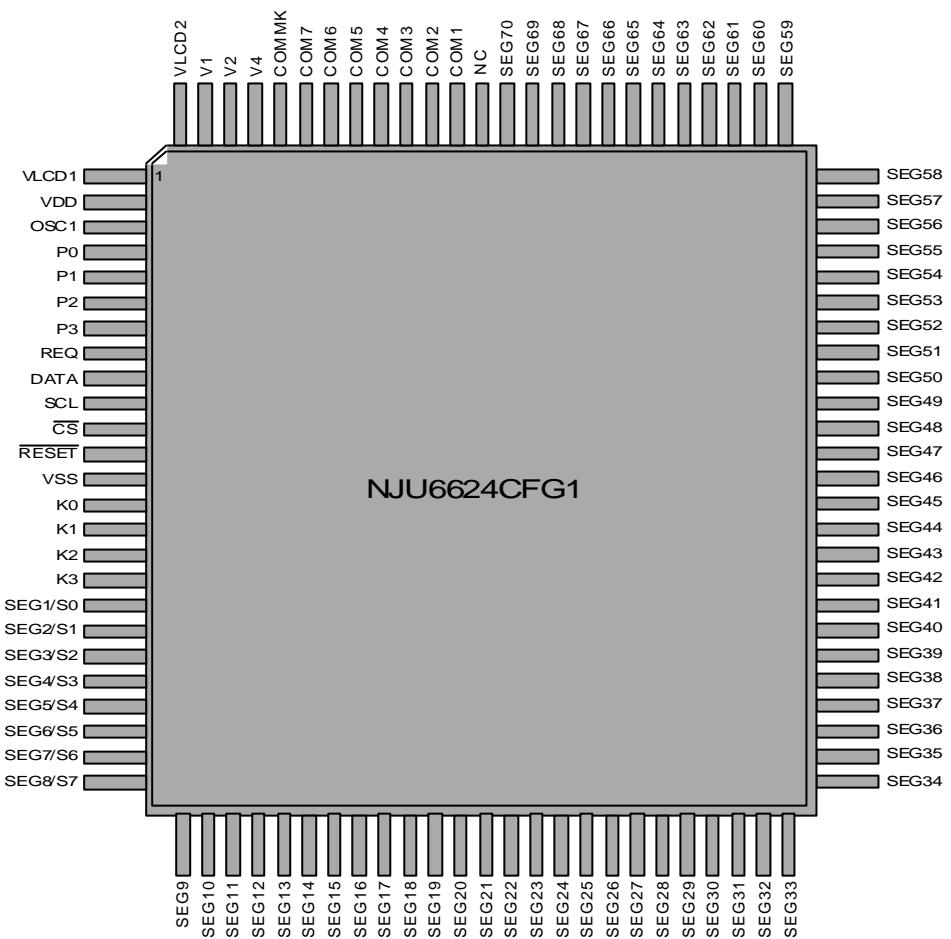
NJU6624CFG1

■ FEATURES

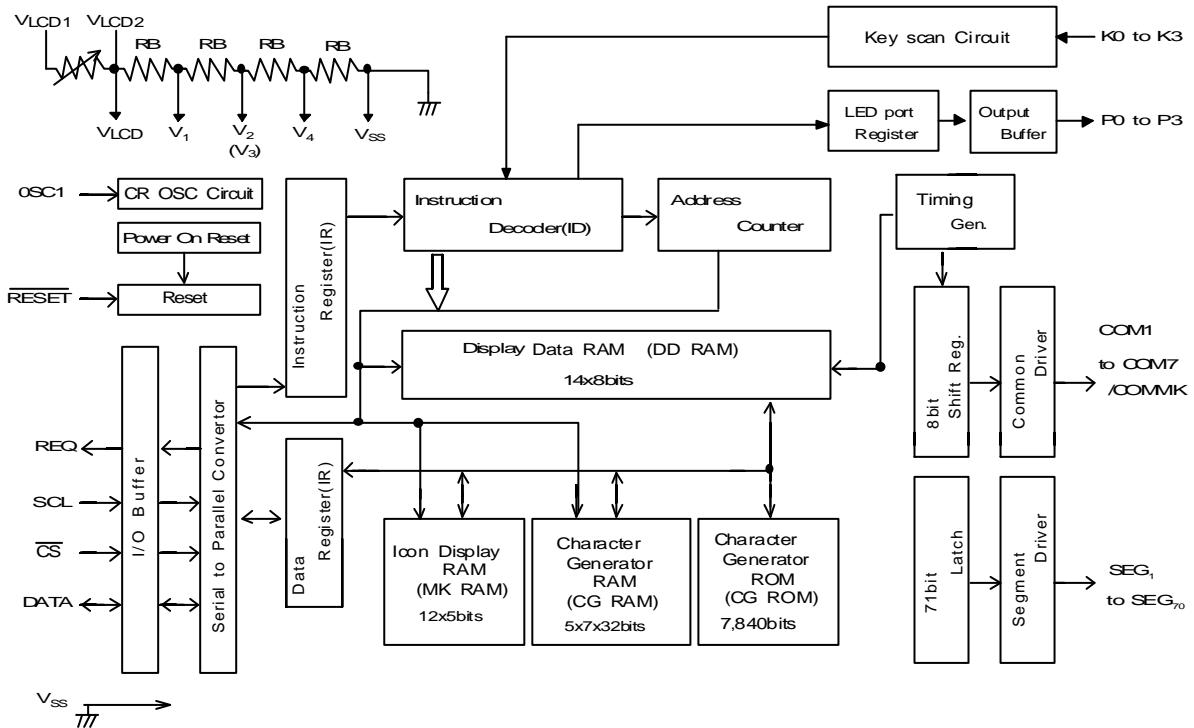
- 14-character 1-line Dot Matrix LCD Controller Driver
- Maximum 70 Icon Display
- Serial Direct Interface with Microprocessor
- Display Data RAM - 14 x 8 bits : Maximum 14-character 1-line Display
- Character Generator ROM - 7,840 bits : 224 Characters for 5 x 7 Dots
- Character Generator RAM - 1,120 bits : 32 Patterns(5 x 7 Dots)
- Icon Display RAM - Maximum 70 Icons
- High Voltage LCD Driver : 8-common / 70-segment
- Duty and Bias Ratio : 1/8 duty, 1/4 bias
- Useful Instruction Set : Clear Display, Address Home, Display ON/OFF Cont., Display Blink, Address Shift, Character Shift, Keyscan ON/OFF Cont. e.t.c.
- 32Key Input (4x8 keys)
- General output port (4 ports)
- Power On Initialization / Hardware Reset
- Bleeder Resistance on-chip
- Software contrast control(16 step)
- Oscillation Circuit on-chip
- Low Power Consumption
- Operating Voltage --- 2.4 to 5.5 V
- Package Outline --- QFP 100
- C-MOS Technology

Apr.2004

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ TERMINAL DESCRIPTION

No.	SYMBOL	I/O	FUNCTION
2,13	VDD,VSS	-	Power Source:VDD=+5V,GND:VSS=0V
1	VLCD1	I	LCD driving voltage input terminal
100 99 98 97	VLCD2 V1 V2 V4	I	LCD driving voltage stabilization capacitor terminals. Connect the capacitor between VLCD2 and VSS, V1 and VSS, V2 and VSS, V4 and VSS. typ. : 0.1uF
3	OSC1	I	System clock input terminal This terminal should be open for internal clock operation.
11	<u>CS</u>	I	Chip select signal input of serial I/F.
10	SCL	I	Sift clock input of serial I/F.
9	DATA	I	Serial Data Input of serial I/F.
12	<u>RESET</u>	I	Reset Terminal. When the "L" level is input over than 1.2ms to this terminal, the system will be reset (at fosc 145KHz).
4-7	P0-P3	O	General output port LED driver drives LED as indicator on athers.
8	REQ	O	Key request signal output terminal.
14-17	K0-K3	I	Key scanning input terminals.
18-25	SEG1/S0 - SEG8/S7	O	LCD segment driving signal output / Key scanning output terminals.
26-87	SEG9-SEG70	O	LCD segment driving signal output terminals
88	NC		Non connection terminal
89-95	COM1-COM7	O	LCD common driving signal output terminals
96	COMMK	O	Icon common driving signal output terminals

■ FUNCTIONAL DESCRIPTION

(1-1) Register

The NJU6624C incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register(DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift" or address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM (MK RAM).

The Register(DR) is a temporary register, the data in the Register(DR) is written into the DD RAM, CG RAM or MK RAM.

The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation.

These two registers are selected by the selection signal RS as shown below.

(1-2) Address Counter (AC)

The address counter(AC) addresses the DD RAM, CG RAM or MK RAM.

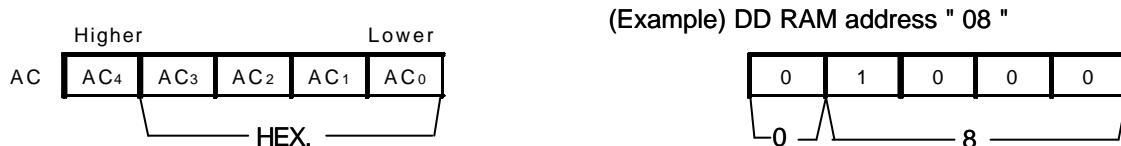
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.

After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter(AC) increments (or decrements) automatically.

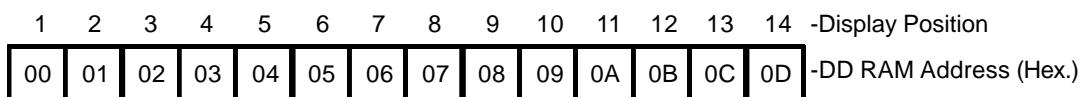
(1-3) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consist of 14x 8 bits stores up to 14-character display data represented in 8-bit code. (2 out of the 14characters are used for scroll RAM.)

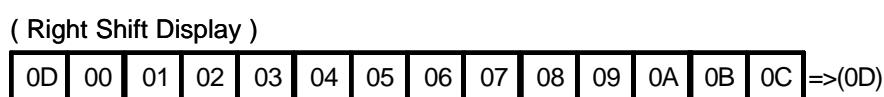
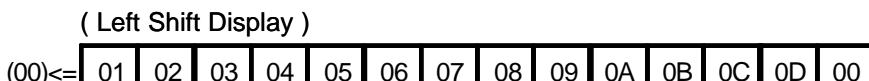
The DD RAM address data set in the address counter(AC) is represented in Hexadecimal.



The relation between DD RAM address and display position on the LCD is shown below.



When the display shift is performed, the DD RAM address changes as follows:



(1-4) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 7 dots character pattern represented in 8-bit character code.

The storage capacity is up to 224 kinds of 5 x 7 dots character pattern (available address is (20)_H through (FF)_H).

The correspondence between character code and standard character pattern of NJU6624C is shown in Table 2.

User-defined character patterns (Custom Font) are also available by mask option.

Table 2. CG ROM Character Pattern (ROM version -02)

		Upper 4bit(HEX.)																
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
Lower 4bit(HEX.)	0	CG RAM (01)	(17)		0	0	P	^	P	G	É		9	3	0	P	
	1	(02)		1	A	Q	a	q	Q	æ	s	7	4	5	9			
	2	(03)		2	B	R	b	r	6	E	^	4	9	X	E			
	3	(04)		3	C	S	c	s	6	o	^	7	E	8				
	4	(05)		4	D	T	d	t	8	ö	^	I	T	7	0			
	5	(06)		5	E	U	e	u	8	ö	^	Ö	7	0				
	6	(07)		6	F	U	f	u	8	ö	^	Ö	7	0				
	7	(08)		7	G	W	g	w	8	ö	^	Ö	7	0				
	8	(09)		8	H	X	h	x	8	9	4	^	Ö	7	0			
	9	(10)		9	I	Y	i	y	8	ö	^	Ö	7	0				
	A	(11)		A	J	Z	z	z	0	ö	^	Ö	7	0				
	B	(12)		B	K	C	k	c	0	ö	^	Ö	7	0				
	C	(13)		C	L	Y	l	y	1	^	Ö	7	0					
	D	(14)		D	M	J	m	j	1	^	Ö	7	0					
	E	(15)		E	N	^	n	^	A	R	a	t	7	0				
	F	(16)		F	?	O	o	o	A	f	o	?	7	0				

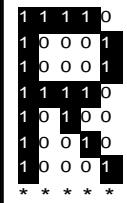
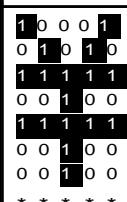
(1-5)Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 7 dots written by the user program to display user's original character pattern. The CG RAM can store 32 kind of character in 5 x 7 dots mode.

To display user's original character pattern stored in the CG RAM, the address data (00)_H-(1F)_H should be written to the DD RAM as shown in Table 2.

Table 3. shows the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots)

Character Code (DD RAM Data)	CG RAM Address		Character Pattern (CG RAM Data)
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0		4 3 2 1 0
Upperbit	Lower bit	Upperbit	Lower bit
0 0 0 0 0 0 0 0	0 0 0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 1 1 1 1 0 1 0 0 0 1 1 0 0 0 1 1 1 1 1 0 1 0 1 0 0 1 0 0 1 0 1 0 0 0 1 * * * * *
0 0 0 0 0 0 0 1	0 0 0 0 1	0 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 1 0 0 0 1 0 1 0 1 0 1 1 1 1 1 0 0 1 0 0 1 1 1 1 1 0 0 1 0 0 0 0 1 0 0 * * * * *
		0 0 0 0 0 1	
		⋮	⋮
		⋮	⋮
		⋮	⋮
		⋮	⋮
0 0 0 1 1 1 1 1	1 1 1 1 1	1 0 0 1 0 1 1 1 0 1 1 1	

* =Don't care

Notes :

1. Character code bit 0 to 4 correspond to the CG RAM address bit 3 to 7(5bits:32 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is Don't care line. In case of input CG RAM data continuously, invalid address are Cursor position automatically.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code of DD RAM bits 5 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display On and "0" to display Off.

(1-6)Icon Display RAM (MK RAM)

The NJU6624C can display maximum 70 Icons.

The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.

The relation between MK RAM address and Icon Display position is shown below:

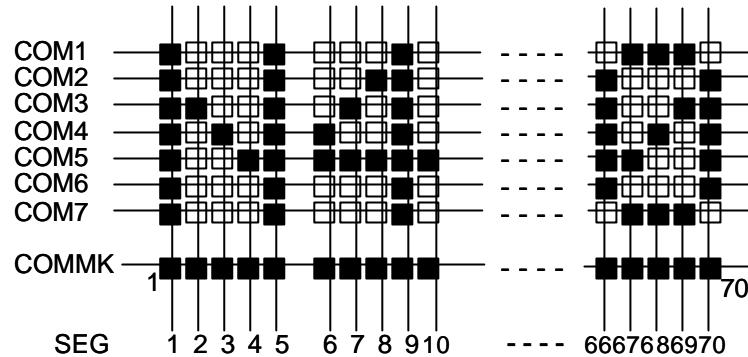


Table 4. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address (10H-1DH)		Bits for Icon Display Position							
		D7	D6	D5	D4	D3	D2	D1	D0
1 0000	10H	0	0	0	"1"	"2"	"3"	"4"	"5"
1 0001	11H	0	0	0	"5"	"7"	"8"	"9"	"10"
1 0010	12H	0	0	0	"11"	"12"	"13"	"14"	"15"
1 0011	13H	0	0	0	"16"	"17"	"18"	"19"	"20"
:	:	:							
1 1101	1DH	0	0	0	"66"	"67"	"68"	"69"	"70"

(1-7)Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.

RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.

Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-8)LCD Driver

LCD Driver consists of 8-common driver and 70-segment driver.

The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

(1-9)Keyscan circuit

The Keyscan circuit consists of a detector block of key pressing and a fetching block of key status. It scans 4x8 key matrix and fetches conditions of 32 keys. Furthermore, it operates correctly against the key roll over input.

-Request signal output

When the NJU6624C detect the key pressing by the key scan circuit, it outputs "H" signal as the request signal from the "REQ" terminal to notice the key pressing information to an application system.

-Contents of key register renewal

Contents of key register are "0000 0000" in case of no key operation. Contents of key register are not changed in busy of key data reading operation. Key data is fetched into the key register after 2 clock of the end of a keyscale cycle and kept by the start of next cycle.

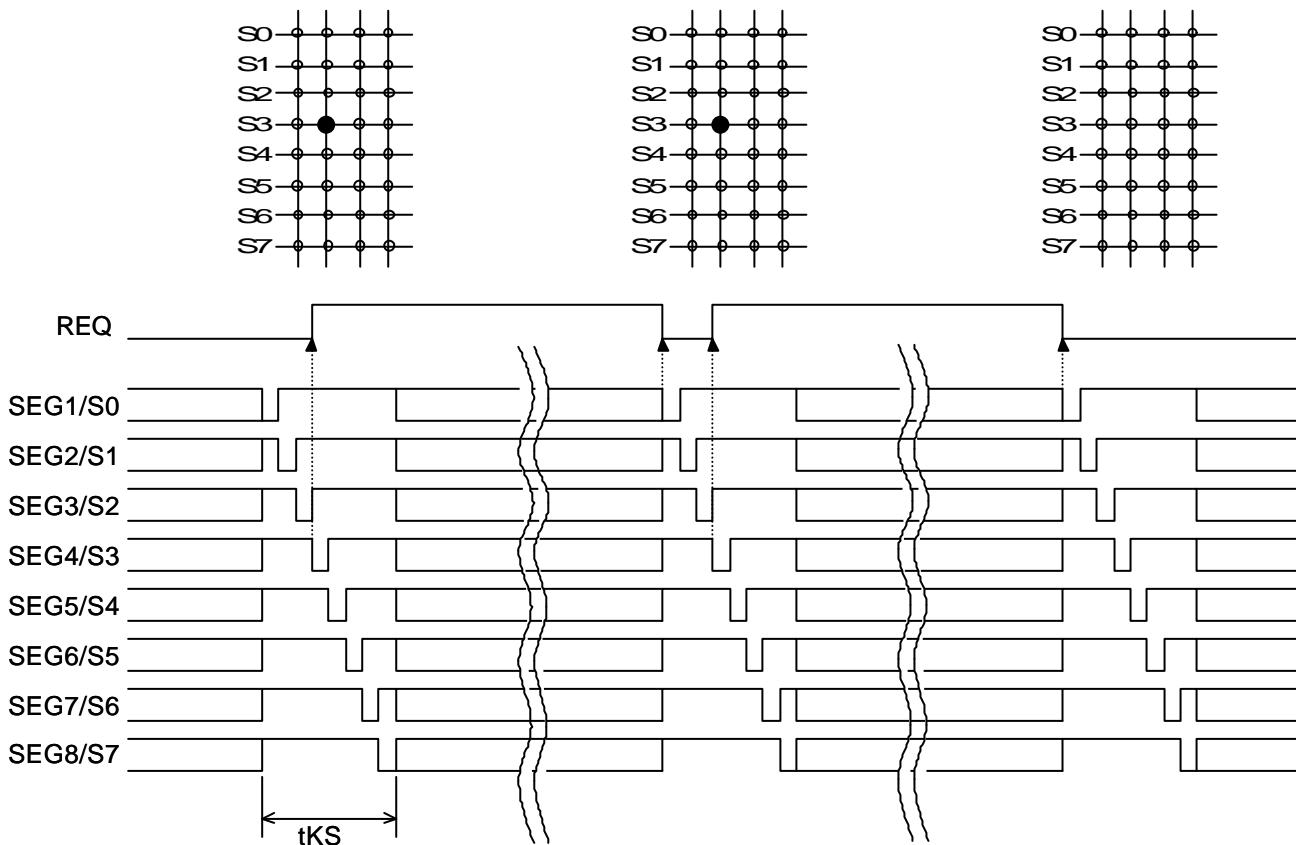
-Key data input terminal and segment terminal

Keyscan signal output terminals operate as segment terminals (SEG1 to SEG8) also and keyscale signals are output in interval period of segment signals. Key data input terminals (K0 to K3) are pulled up to VDD in busy of keyscale operation (tKS). In this period, terminals of SEG9 to SEG70 output the voltage of V2 or VLCD2.

-Keyscan OFF mode

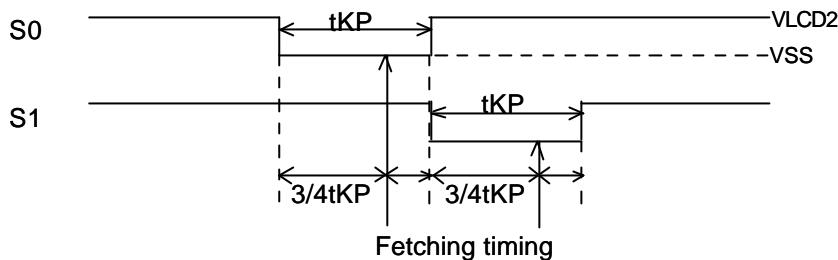
Keyscan operation is turned ON or OFF by the instruction. In case of keyscale OFF, the detector of key pressing is not operating and key data input terminals (K0 to K3) are not pulled up during the period of keyscale (tKS). In the period of keyscale (tKS), all of segment terminals (SEG1 to SEG70) output the voltage of V2 or VLCD2.

-Example Keyscan



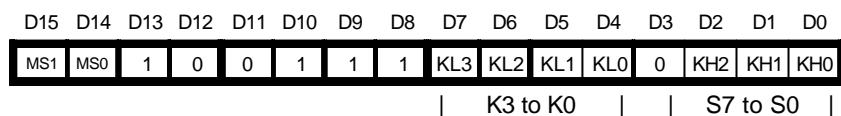
-Key status fetching timing

Key status is fetched at third quarter of "L" period (tKP) of scan signals (S0 to S7) as shown below;



-Keyscan data format

Scanned 8-bit data of key are read out through the serial I/F.

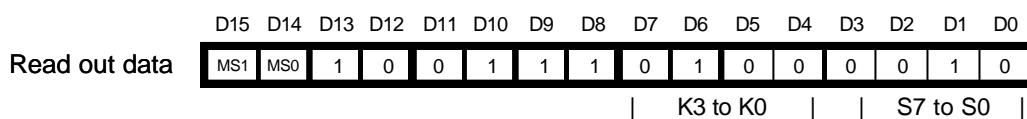
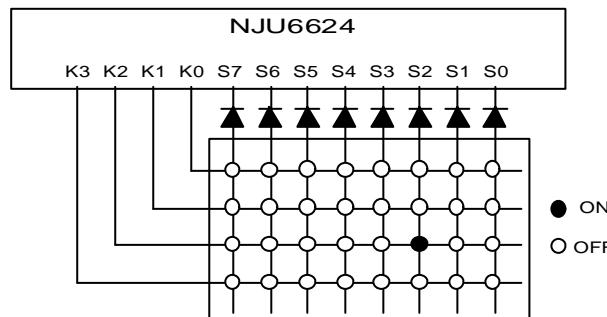


Keyscan output data	KH2	KH1	KH0
S7	1	1	1
S6	1	1	0
S5	1	0	1
S4	1	0	0
S3	0	1	1
S2	0	1	0
S1	0	0	1
S0	0	0	0

When a key on the key matrix is pressed, the bit corresponding to terminals (K3 to K0, S7 to S0) connected the switch goes to "1" and another bits go to "0".

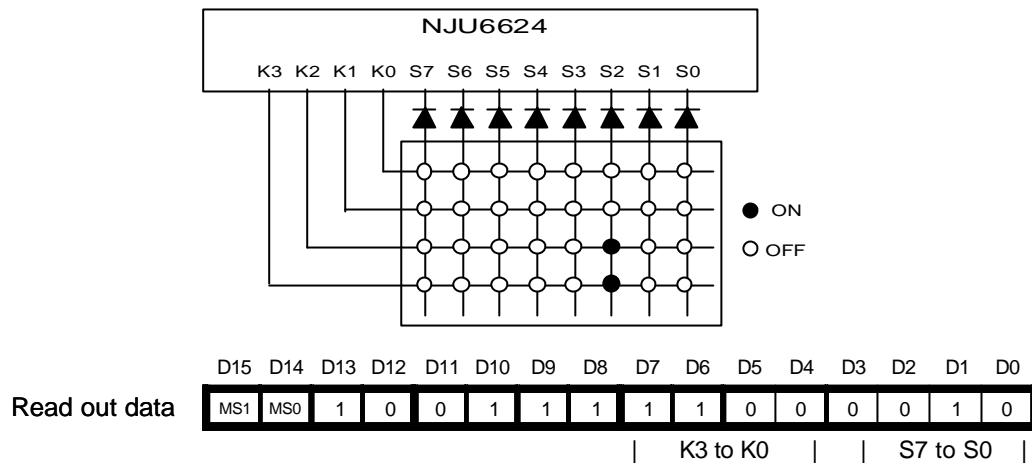
In case of Example 1, when the switch connecting to K2 and S2 is pressed, bit(D6) corresponding to K2 and bit(D1) corresponding to S2 go to "1" but another bits go to "0".

Example 1. One key is pressed

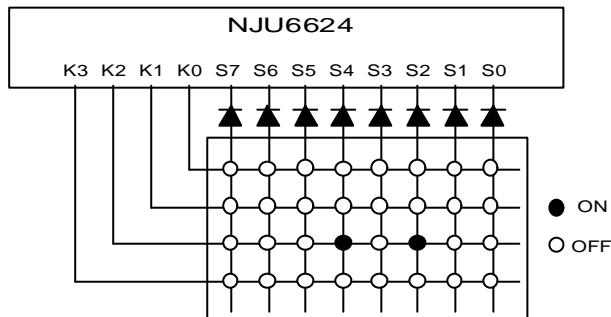


The key roll over input is the vertical line as shown below (Example 2) can be accepted with the keyscan circuit. But in case of Example 3, the key roll over input in the horizontal line can not be accepted. The key roll over input must be taken care for key data judgement.

Example 2. The key roll over input (1)



Example 3. The key roll over input (2)

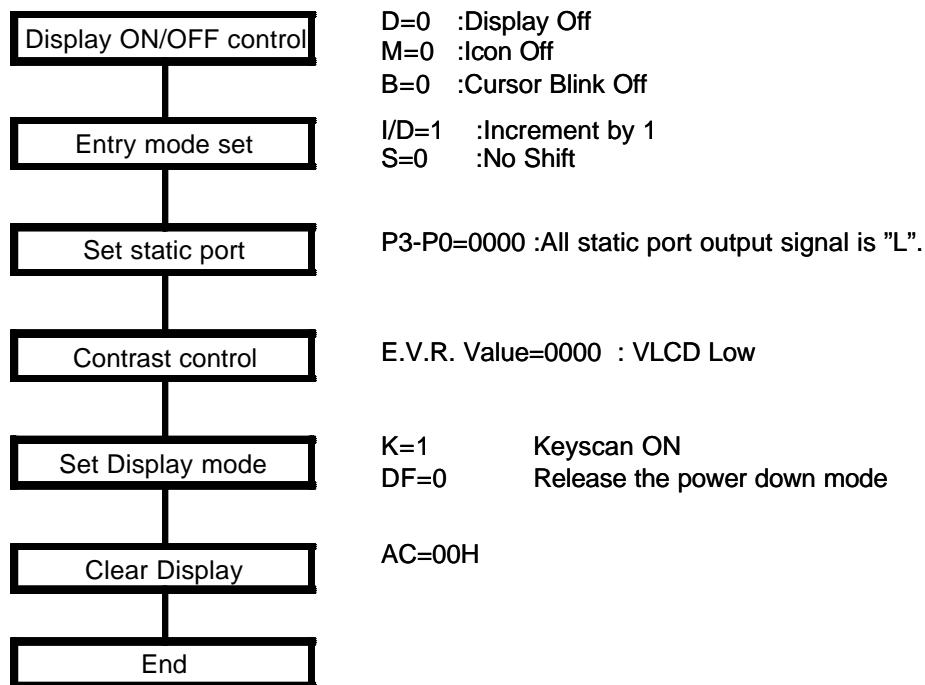


Note : In case of can not read out correct.

(2)Power on Initialization by internal circuits

(2-1)Initialization By Internal Reset Circuits

The NJU6624C is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 1.5ms (fosc=145kHz) after V_{DD} rises to 2.4V. Initialization flow is shown below:

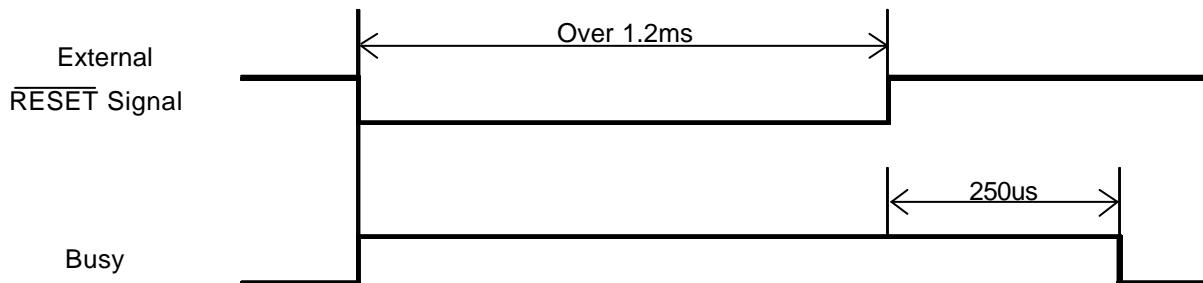


Note : If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operate and initialization will not be performed. In this case the initialization by MPU software is required.

(2-2)Initialization By Hardware

The NJU6624C incorporates RESET terminal to initialize the entire system. When the "L" level input over 1.2ms to the RESET terminal, a reset sequence is executed. In this time, a busy signal output during 250us (fosc=145kHz) after the RESET terminal goes to "H". During this 250us period, any other instruction must not be input to the NJU6624C.

-Timing Chart



(4)Instructions

The NJU6624C incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6624C and MPU or peripheral ICs operating different cycles.

Table 4. Table of Instructions

INSTRUCTION		CODE															Execute Time		
		D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
(a)	Marker Testing	1	0	0	1	1	1	1	1									-	
(b)	Clear Display	1	0	0	1	1	0	0	1	*	*	*	*	*	*	*	234.48uS		
(c)	Return Home	1	0	0	1	0	0	0	1	*	*	*	*	*	*	*	0uS		
(d)	Entry Mode Set	1	0	0	0	1	0	0	0	*	*	*	*	*	*	I/D	S	0uS	
(e)	Display ON/OFF Control	1	0	0	0	1	0	0	1	*	*	*	*	*	D	M	B	0uS	
(f)	Address Shift	1	0	0	1	0	0	1	0	*	*	*	*	*	*	*	ARL	0uS	
(g)	Display Shift	1	0	0	0	1	0	1	0	*	*	*	*	*	*	*	DRL	0uS	
(h)	Set Static Port	1	0	0	0	1	0	1	1	*	*	*	*	*	P3	P2	P1	P0	0uS
(i)	Contrast Control	1	0	0	0	1	1	0	0	*	*	*	*	*	E.V.R. Value			0uS	
(j)	Set Display Mode	1	0	0	0	1	1	1	0	*	*	*	*	*	*	K	PD	0uS	
(k)	Set DD/MK RAM Address	1	0	0	1	0	0	1	1	*	*	*			DD RAM(00 to 0D)H MK RAM(10 to 1D)H			0uS	
(l)	Set CG RAM Address	1	0	0	1	0	0	0	0	CG RAM(00 to FE)H								0uS	
(m)	Write DD RAM Data	1	0	0	1	1	0	0	0	Write data(DD RAM)								41.38uS	
	Write MK RAM Data	1	0	0	1	1	0	0	0	*	*	*			Write data(MK RAM)			41.38uS	
	Write CG RAM Data	1	0	0	1	1	0	0	0	*	*	*			Write data(CGRAM)			41.38uS	
(n)	Read Keypress Data	1	0	1	0	0	1	1	1	Key Data								0uS	

Note : fosc=145KHz. If the oscillation frequency is changed, the execution time is also changed.

(4-1)Description of each instructions

(a)Maker Testing

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	1	1	1	1	1	*	*	*	*	*	*	*	*

This code is using for device testing mode (only for maker).

Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".

(Especially please check the output condition of Enable signal when the power turns on.)

(b)Clear Display

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	1	1	0	0	1	*	*	*	*	*	*	*	*

When this instruction is executed, the space code (20_H) is written into every DD RAM address, the DD RAM address (00_H) is set into the address counter and entry mode is set to increment. The S of entry mode does not change.

Note: The character pattern for character code (20_H) must be blank code in the user-defined character pattern (Custom font).

(c)Return Home

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	1	0	0	0	1	*	*	*	*	*	*	*	*

Return home instruction is executed, the DD RAM address (00_H) is set into the address counter. Display is returned its original position if shifted. The DD RAM contents do not change.

(d)Entry Mode Set

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	0	1	0	0	0	*	*	*	*	*	*	I/D	S

Entry mode set instruction which sets the address moving direction and display shift On/Off, is executed when the codes of (I/D) and (S) are written into DB₁(I/D) and DB₀(S), as shown below.

(I/D) sets the address increment or decrement, and the (S) sets the whole display shift in the DD RAM writing.

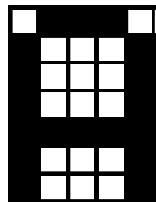
I/D	F u n c t i o n
1	Address increment: The address of the DD RAM or MK RAM or CG RAM increment (+1) when the write.
0	Address decrement: The address of the DD RAM or MK RAM or CG RAM decrement: (-1) when the write.
S	F u n c t i o n
1	Whole display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The display does not shift when writing into CG, MK RAM.
0	The display does not shift.

(e) Display ON/OFF Control

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
	1	0	0	0	1	0	0	1	*	*	*	*	*	*	D	M	B

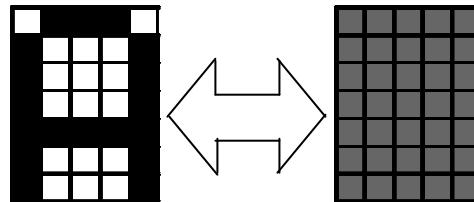
Display On/Off control instruction which controls the whole display On/Off and the addressed position character blink, is executed when the codes of (D) and (B) are written into DB₂(D) and DB₀(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.
M	Function
1	Icon display ON.
0	Icon display OFF.
B	Function
1	The addressed position character is blinking. Blinking rate is 500ms at f _{osc} =145kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 7 dots

(1) Cursor display example



Alternating display

(2) Blink display example

When the number of dot-shift is not set "0" in (j)Dot shift instruction, the blink operation will be appeared at the irregular position.

(f) Address Shift

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	1	0	0	1	0	*	*	*	*	*	*	*	ARL

The Address shift instruction shifts the Address to the right or left without writing or reading display data.

ARL	Function
0	Shifts the address position to the left ((AC) is decremented by 1)
1	Shifts the address position to the right ((AC) is incremented by 1)

(g)Display Shift

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	0	1	0	1	0	*	*	*	*	*	*	*	DRL

The Display shift instruction shifts the Display to the right or left without writing or reading display data. The contents of address counter(AC) does not change by operation of the display shift only.

DRL	Function
0	Shifts the whole display to the left and the cursor follows it.
1	Shifts the whole display to the right and the cursor follows it.

(h)Set Static Port

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
	1	0	0	0	1	0	1	1	*	*	*	*	*	P3	P2	P1	P0

It sets Static Output Port signal which can drive LED directly like as indicator. Initial status is "L".

(i)Contrast Control

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	0	1	1	0	0	*	*	*	*	C3	C2	C1	C0

Contrast Control instruction which adjusts the contrast of the LCD, is executed when the code "1" is written into DB₆ and the codes of C₃ to C₀ are written into DB₃ to DB₀ as shown below.

The contrast of LCD can be adjusted one of 16 voltage-stages by setting this 4-bit register.

See (5-1) "how to adjust the Contrast of LCD".

Set the binary code "0000" when contrast adjustment is unused.

C ₃	C ₂	C ₁	C ₀	V _{LCD}	V _{LCD} = V _{LCD2} - V _{SS}
0	0	0	0	low	
1	1	1	1	high	

(j) Set Display Mode

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	0	1	1	1	0	*	*	*	*	*	*	K	PD

The Set Display Mode instruction control the function of key scan and power down mode.

K	Function
1	Key scan ON
0	Key scan OFF In busy of keyscan (tKS), all of segment terminal (S0 to S7) output the voltage of V2.or VLCD2
PD	Function
1	Power down mode. All of common and segment terminal set the voltage level of VLCD2
0	Release the power down mode.

In busy of Power down mode, do not input any instructions except for release the power down mode.

The power down mode should be set before power off because any irregular display appearance at power off is prevented.

The key scan operation when switching to the power down mode during key scan.

When switching to the power down mode during key scan operation, it stops key scan operation in the period and after power down mode cancellation too.

After power down mode cancellation, the REQ signal maintains "H" when detects key-in signal before switches to power down mode and REQ signal rises to "H".

However, the key scan operation becomes invalid data even if it reads key-in data because it stopped. The key data becomes to valid with the key scan by the next key scan of frame.

(k) Set DD/MK RAM Address

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	1	0	0	1	1	*	*	*	AD4	AD3	AD2	AD1	AD0

The address data (DB₄ to DB₀) is written into the address counter (AC) by this instruction.

After this instruction execution, the data writing is performed into the addressed DD/MK RAM.

The RAM includes DD RAM and MK RAM, and these RAMs are shared by address as shown below.

RAM address	
DD RAM	: (00) _H - (0D) _H
MK RAM	: (10) _H - (1D) _H

(l) Set CG RAM Address

Code	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	1	0	0	1	0	0	0	0	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0

The CG RAM address set instruction is executed when the "H" level input to the AC terminal and the address is written into DB₇ to DB₀ as shown above.

The address data (DB₇ to DB₀) is written into the address counter (AC) by this instruction.

After this instruction execution, the data writing is performed into the addressed RAM.

The RAM includes CG RAM address as shown below.

RAM address	
CG RAM	: (00) _H - (FE) _H

(m)Write Data to CG, DD or MK RAM

By the execution of this instruction, the binary 8-bit data (A_7 to A_0) are written into the DD RAM, and the binary 5-bit data (A_4 to A_0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment (+1) or decrement(-1) is performed automatically according to the entry mode set. And the display shift is also executed according to the previous entry mode set. However, the data in MK RAM (1C)H and (1D)H are not displayed, bat the automatic address increment is performed. And the display is not changed by the data written into MK RAM (1C)H and (1D)H

-Write Data to DD RAM

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	1	1	0	0	0	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

-Write Data to MK RAM

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	1	0	0	0	0	*	*	*	DM4	DM3	DM2	DM1	DM0

-Write Data to CG RAM

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	0	1	0	0	0	0	*	*	*	DC4	DC3	DC2	DC1	DC0

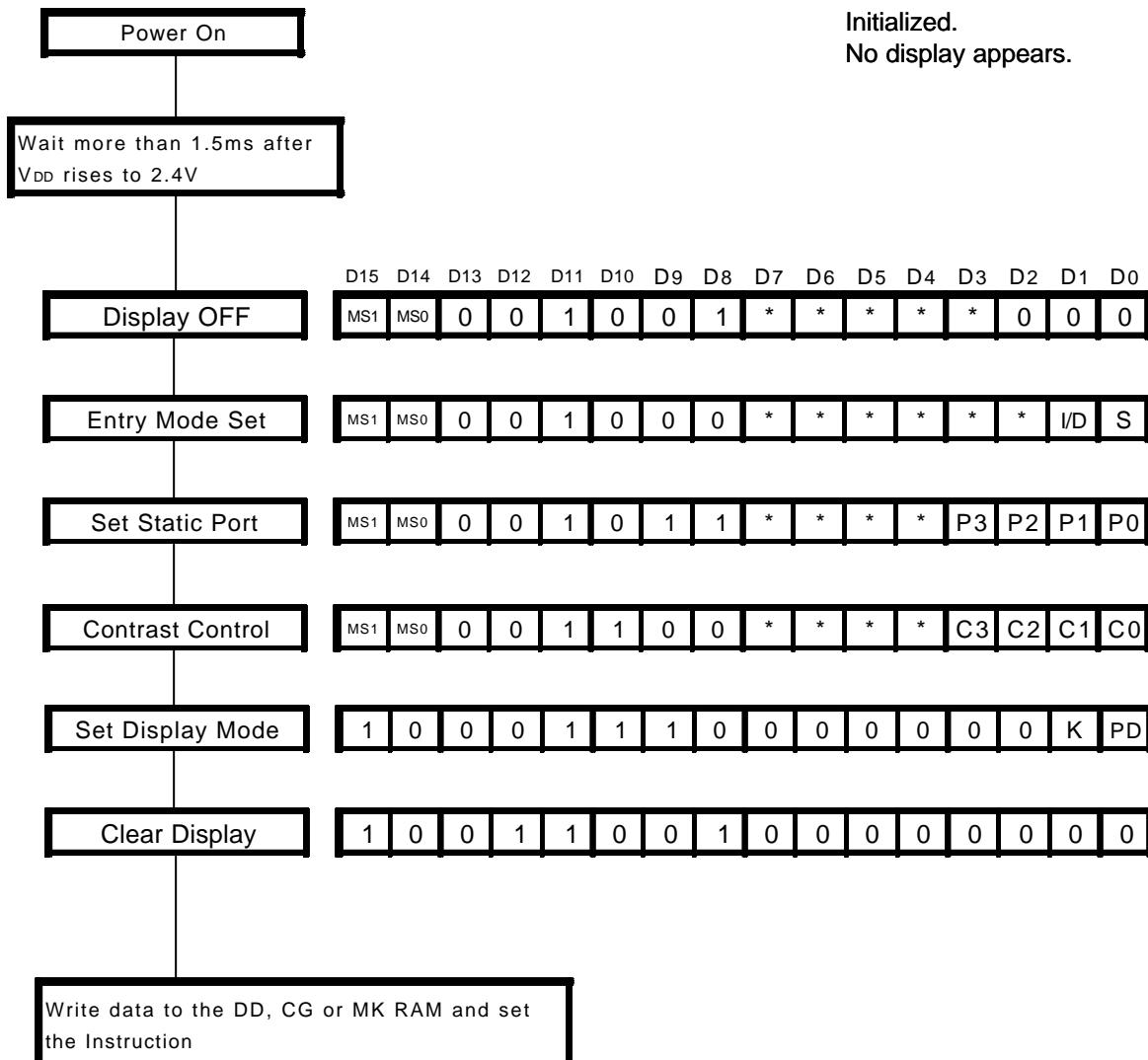
(n)Read Data Key

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Code	1	0	1	0	0	1	1	1	KL3	KL2	KL1	KL0	0	KH2	KH1	KH0

Read data key is a instruction for data reading out of keyscan. However, the bit 8 to 15 are input data. After this 8-bit data were input, the operation change to output from input at the falling edge of 8th SCK clock.

(4-2)Initialization by instruction

If the power supply conditions for the correct operation of the internal reset circuits are not satisfied, the NJU6624C must be initialized by the instruction.



Note : When the Icon display function using, the system should be initialized by software initialization.

(5)LCD display

(5-1)Bleeder Resistance

Each LCD driving voltage (V_1 , V_2 , V_3 , V_4) is LCD driving high voltage input to the VLCD1 terminal, generated by the E.V.R. and high impedance bleeder resistance.

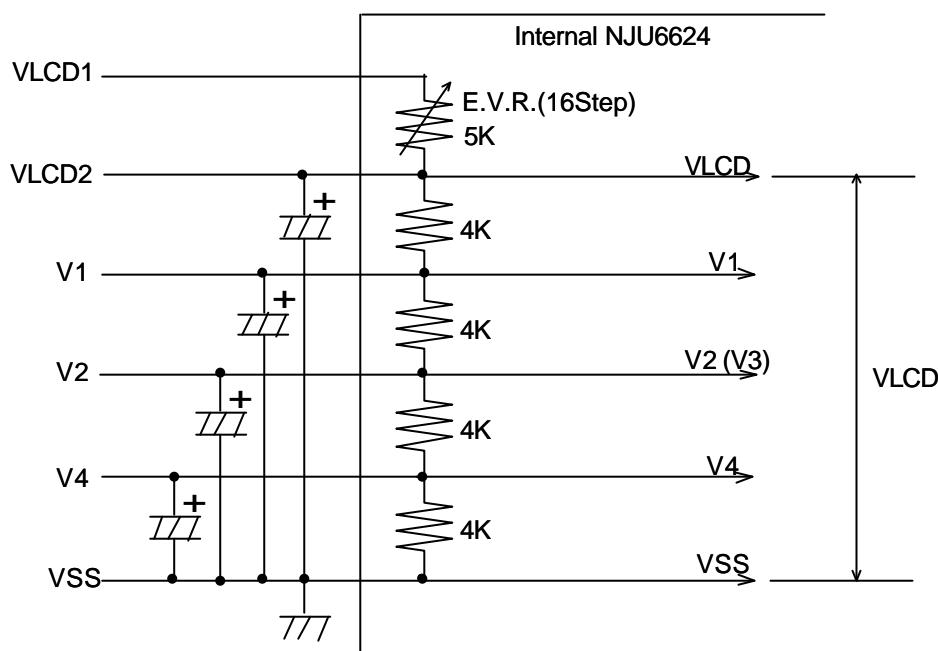
The bleeder resistance is set 1/4 bias suitable for 1/8 duty ratio.

The capacitor connected between VLCD2 and Vss is needed for stabilizing VLCD. The determination of the each capacitance requires to operate with the LCD panel actually.

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/8
	Bias	1/4
	V_{LCD}	VLCD2- VSS

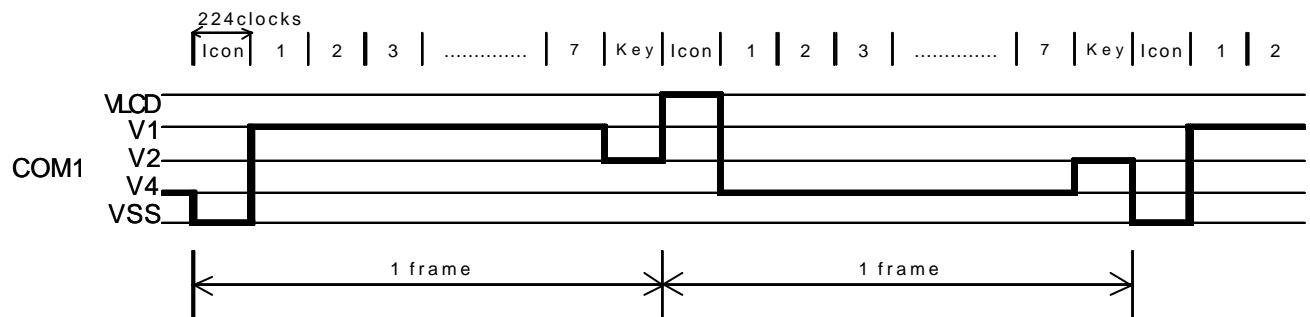
V_{LCD} is the maximum amplitude for LCD driving voltage.



(5-2)Relation between oscillation frequency and LCD frame frequency

As the NJU6624C incorporate oscillation capacitor and resistor for CR oscillation, 145kHz oscillation is available without any external components.

The LCD frame frequency example mentioned below is based on 145kHz oscillation.(1clock = 6.90us)



$$1 \text{ frame} = 6.90(\text{us}) \times 224 \times 8 = 12.36(\text{ms})$$

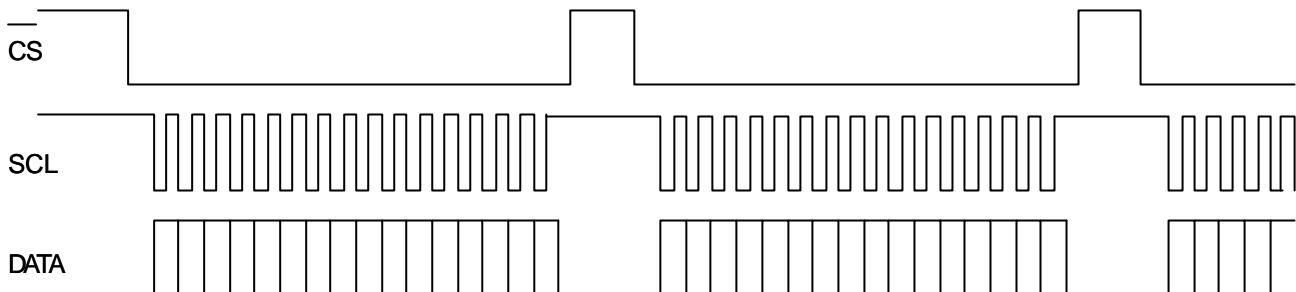
$$\text{Frame frequency} = 1 / 12.36(\text{ms}) = 79.50(\text{Hz})$$

$$\text{Key scan time} = 220.70(\mu\text{s})$$

(6)Interface with MPU

The instructions and data are communicated with the serial port which is a clock synchronization type based on 16-bit per word.

The NJU6624C can be controlled by the serial data as shown below.



The serial interface circuit operates in CS=L.

A communication unit consists of 16-bit data. The communication period is from the falling edge of CS terminal to the rising edge. The inputs data and latched at rising edge of shift clock (SCL) and the first 16-bit data are fetched into the NJU6624C at the rising edge of chip select (CS). The data over than 16 bits are ignored. If the input data are less than 16 bits, they are ignored at the rising edge of "CS". Therefore, just 16 bits data should be input for the correct communication. In case of RAM data input, the RAM address is changed automatically as increment or decrement.

The data to input is MSB first. Although the output data is just only key scan, data bits D8 to D15 in the key data read out instruction are input. After these 8-bit instruction is input, this serial data input terminal is changed to the output terminal at the 8th falling edge of SCL clock.

The electrical short between the NJU6624C and external circuit must be prevented in the application.

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage(1)	VDD	-0.3 to +7.0	V	
Supply Voltage(2)	VLCD1	VSS+10.5 to VSS+0.3	V	VLCD1 Terminal
Input Voltage	V _{IN}	-0.3 to VDD+0.3	V	
Operating Temperature	T _{opr}	-40 to +85	°C	
Storage Temperature	T _{stg}	-55 to +125	°C	
Power Dissipation	PD	500	mW	

Note 1 : If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed.

Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause mal function and poor reliability.

Note 2 : Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the Voltage converter.

Note 3 : All voltage values are specified as V_{SS} = 0V

The relation : VLCD1 ≥ VLCD2 > VDD > V_{SS} , V_{SS}=0V must be maintained.

■ ELECTRICAL CHARACTERISTICS

(VDD=4.5V to 5.5V, Ta=-40 to +80°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input Voltage	VIH1		0.8VDD	-	VDD	V	4
	VIL1		VSS	-	0.2VDD	V	4
Input Voltage	VIH2		0.8VDD	-	VLCD1	V	5
	VIL2		VSS	-	0.2VDD	V	5
Output Voltage	VOH	-IOH=2mA, VDD=5V	4.0	-	-	V	6
	VOL	IOL=2mA, VDD=5V	-	-	0.5	V	6
Driver On-resist.(COM)	RCOM	±Id=1uA(COM Terminal) Vo=VLCD,VSS,V1,V4	-	-	40	KΩ	8
Driver On-resist.(SEG)	RSEG	±Id=1uA(SEG Terminal) Vo=VLCD,VSS,V2	-	-	40	KΩ	8
Pull-up MOS Current 1	-Ip1	VDD=5V	5	25	50	uA	5
Pull-up MOS Current 2	-Ip2	VDD=5V	10	25	50	uA	5
Input Leakage Current	ILI	VIN=0 to VDD	-1.0	-	1.0	uA	10
Operating Current	IDD1	VDD=5V fosc=145KHz Ta=25°C, Display, keyscanON	-	-	500	uA	7
	IDD2	VDD=5V, Ta=25°C stand-by mode	-	7	10	uA	7
Bleeder resistan- ce circuit	LCD Driving Voltage	V1	VLCD1-VSS=8V,Ta=25°C E.V.R. value "1111"	5.8	6.0	6.2	V
		V2	COM/SEG terminal	3.8	4.0	4.2	V
		V4	VLCD1-VSS=8V,Ta=25°C E.V.R. value "1111"	1.8	2.0	2.2	V
Bleeder resistance	RB	VLCD1-VSS=8V,Ta=25°C E.V.R. value "1111"	11.2	16.0	20.8	KΩ	
Oscillation Frequency	fosc	VDD=5V, Ta=25°C	72	145	218	KHz	
LCD Display Voltage	VLCD1	VLCD1 Terminal, VSS=0V	VDD	-	10.0	V	9
VCD1 Current	ILCD1	VLCD1-VSS=8V			1	mA	

Note 4 : Apply to the OSC1, SCL, DATA, \overline{CS} , \overline{RESET} Terminals.

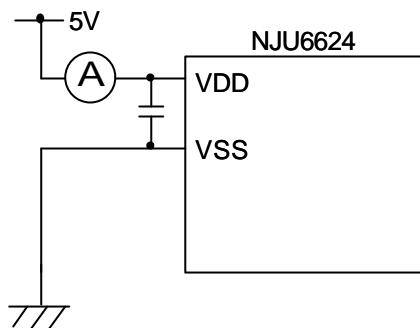
Note 5 : "Pull-up MOS Current 1" : Apply to the DATA Terminals.

"Pull-up MOS Current 2" and "Input Voltage 2" : Apply to the K0 to K3 Terminals.

Note 6 : Apply to the P0 to P3, REQ, DATA Terminals.

Note 7 : If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

-Operating Current Measurement Circuit



Note 8 : R_{COM} and R_{COM} are the resistance values between power supply terminals (V_{ss} , $VLCD2$ or V_1, V_2, V_4) and each common terminal (COM_1 to COM_7 /COMM K) and supply voltage (V_{ss} , $VLCD2$ or V_1, V_2, V_4) and each segment terminal (SEG_1 to SEG_{70}) respectively, and measured when the current I_s is flown on every common and segment terminals at a same time.

Note 9 : Apply to the output voltage from each COM and SEG are less than $\pm 0.15V$ against the LCD driving constant voltage (V_{DD} , V_{LCD1}) at no load condition.

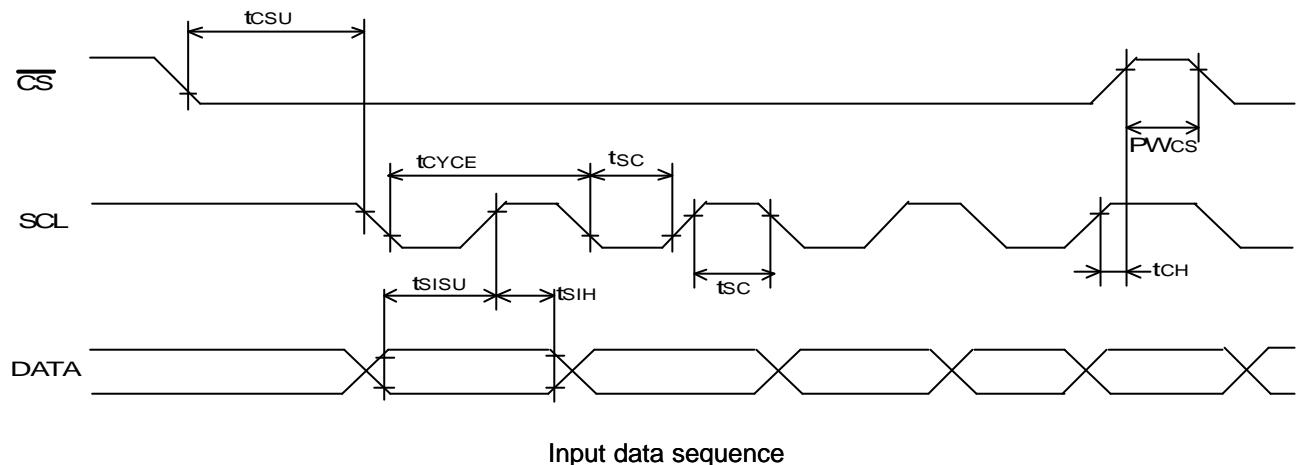
Note 10: Apply to the SCL,CS,RESET Terminals.

■ Bus timing characteristics

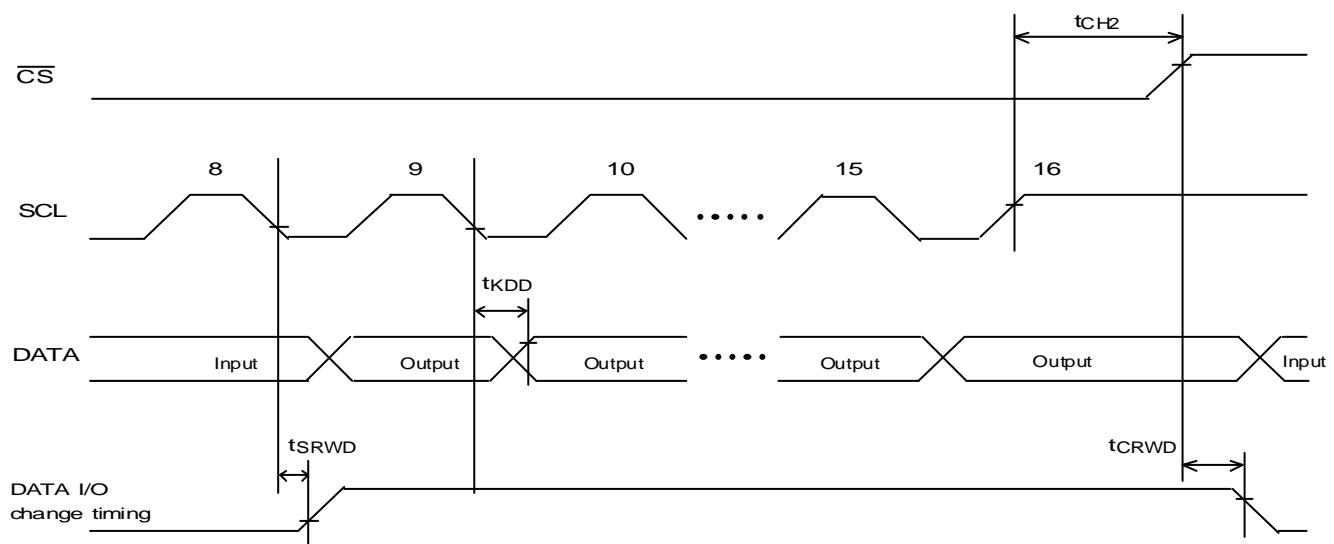
-Serial Interface Sequence

(V_{DD}=4.5V to 5.5V, VLCD1=V_{SS}+8.0V, Ta=25°C)

PARAMETER	SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial clock cycle time	t _{CYCE}	1	-	fig.1	us
Serial clock width	t _{SC}	300	-		ns
Chip select pulse width	PW _{CS}	100	-		us
Chip select set up time	t _{CSU}	300	-		ns
Chip select hold time 1	t _{CH1}	300	-		ns
Serial input data set up time	t _{ISU}	300	-		ns
Serial input data hold time	t _{SIH}	300	-		ns
Key data output delay time	t _{KDD}	-	300		ns
Data port direction change time from input to output	t _{SRWD}	-	300		ns
Data port direction change time from output to input	t _{CRWD}	-	300		ns
Chip select hold time 2	t _{CH2}	1	-		us

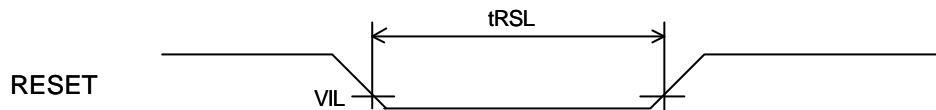


Input data sequence



Input data sequence

-The Input Condition when using the Hardware Reset Circuit

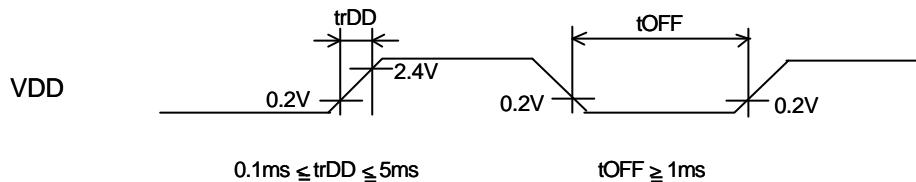


PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reset input "0" level width	t_{RSL}	$f_{OSC}=145\text{kHz}$	1.2	-	-	ms

-Power Supply Condition when using the internal initialization circuit ($T_a=25^\circ\text{C}$)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Power supply rise time	t_{DD}	-	0.1	-	5	ms
Power supply OFF time	t_{OFF}	-	1	-	-	ms

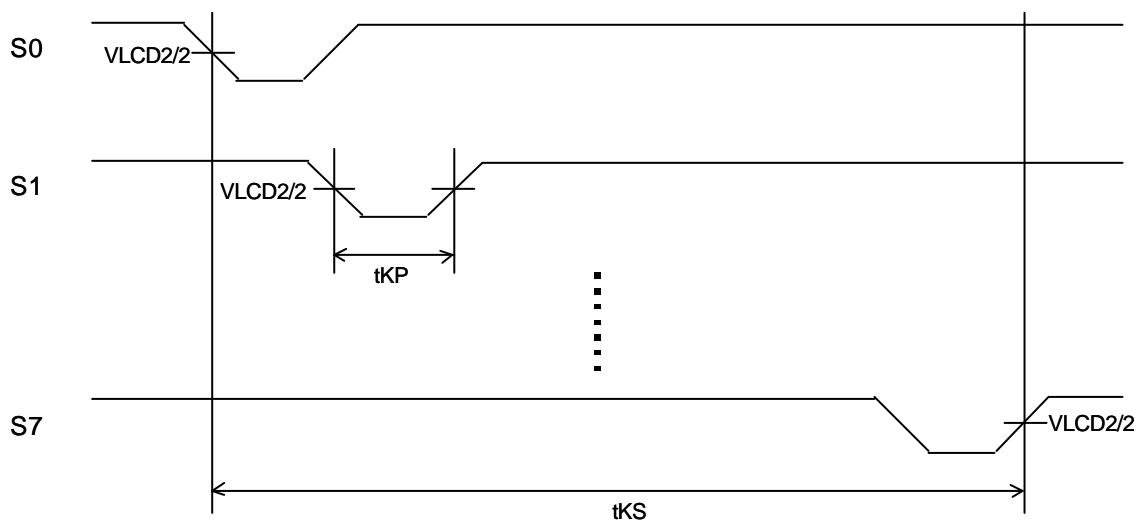
Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction. (Refer to initialization by the instruction)



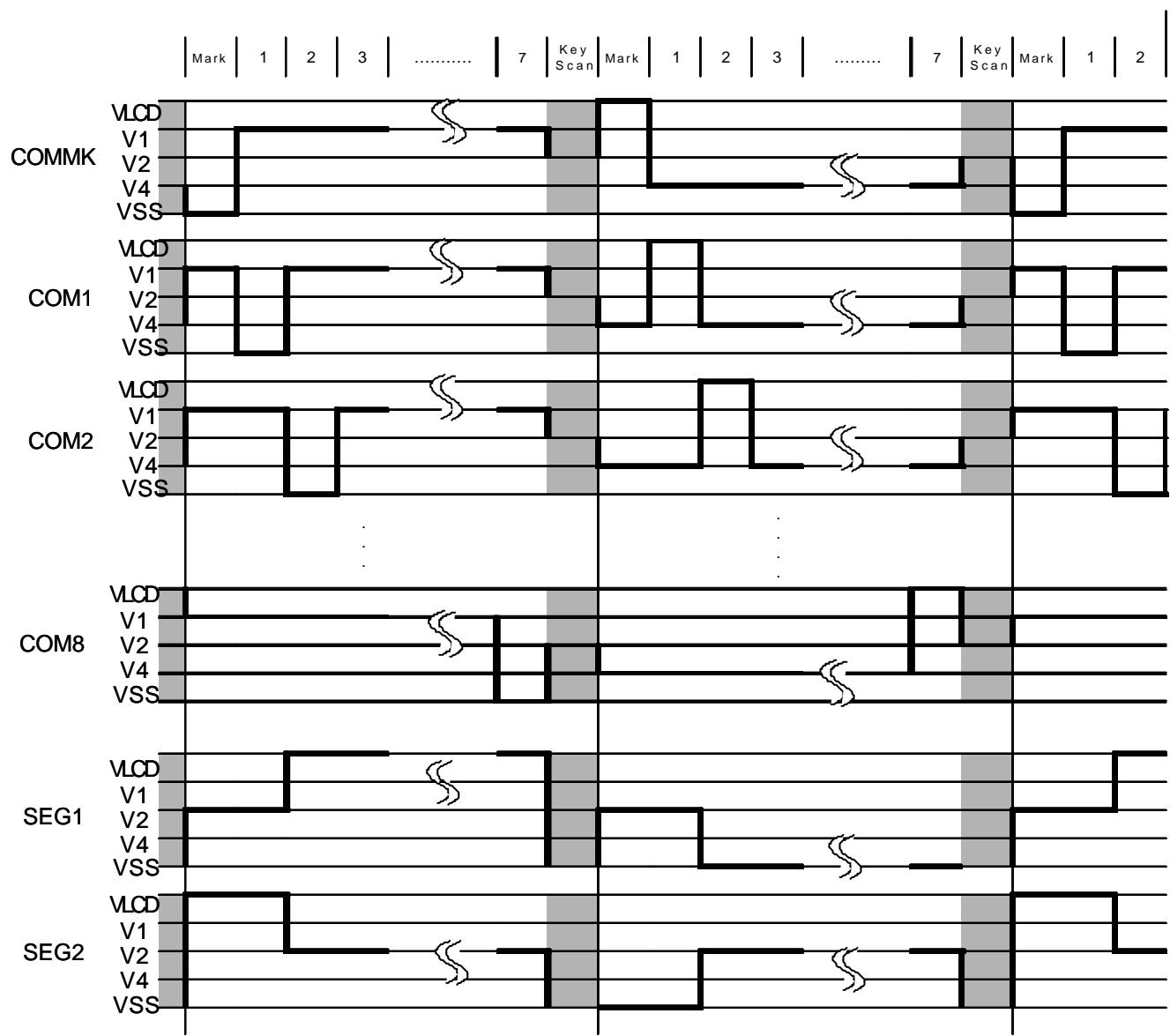
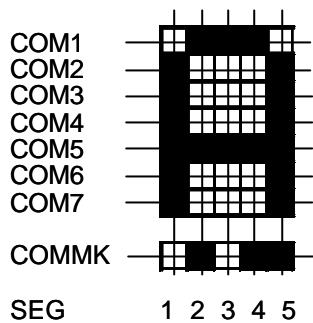
-Keyscan timing

($f_{OSC}=145\text{kHz}$)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Keyscan time	t_{DD}	-	-	221	-	us
Keyscan pulse width	t_{OFF}	-	-	27.6	-	us



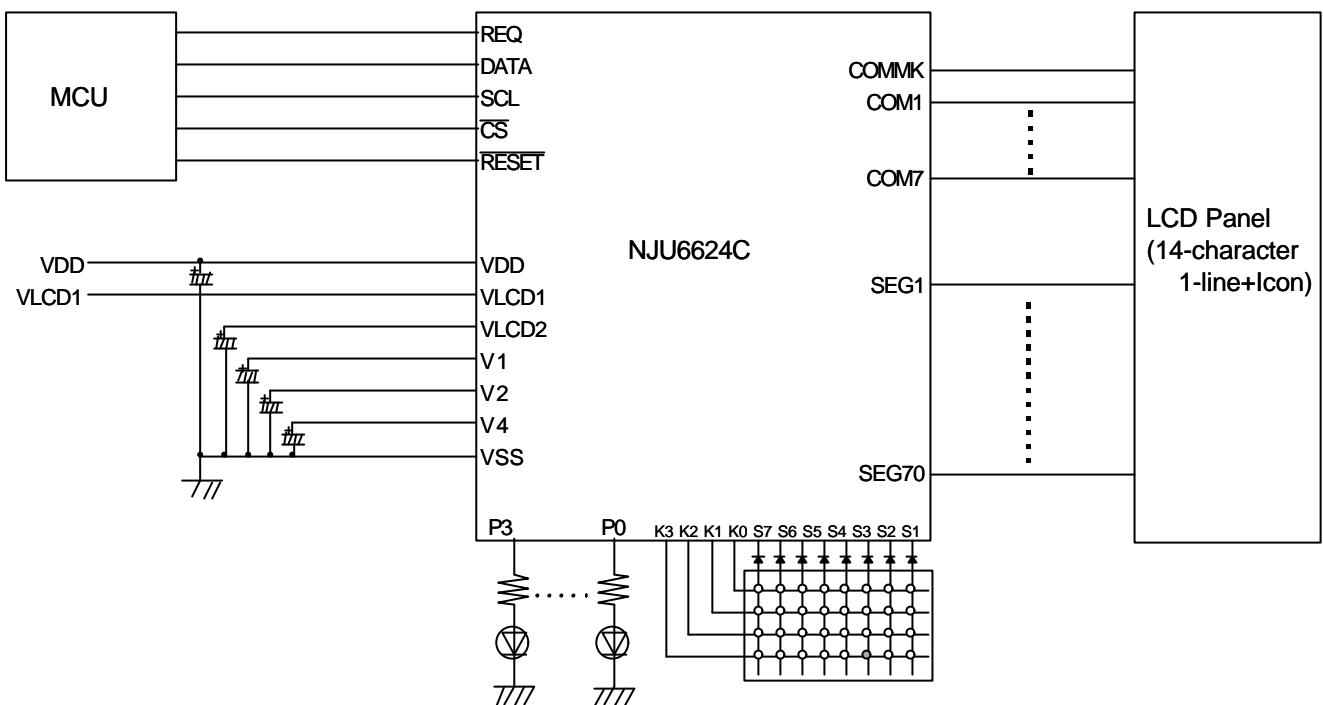
■LCD DRIVING WAVE FORM



■ is Key scan wave form

APPLICATION CIRCUITS

14-character 1-line Display Example



MEMO

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