

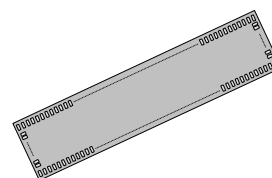
128COMMON x 128RGB LCD DRIVER FOR 4,096-COLOR STN DISPLAY

■ GENERAL DESCRIPTION

The NJU6824 is a 128COMMON x 128RGB LCD driver for 4,096-color STN display. It contains common drivers, RGB drivers, 2RGB icon-drivers, a serial and a parallel MPU interface circuit, an internal LCD power supply, grayscale palettes and 196,608-bit display data RAM. The segment drivers for RGB (Red, Green, Blue) independently produce optimum 16 grayscales from a built-in 32-grayscale palette, and the LSI achieves 4,096 colors (16x16x16). And the LSI features the display-rotation function which rotates an on-screen image in the unit of 90 degrees.

In addition, the NJU6824 operates with a low voltage of 1.7V and a low operating current, therefore it is ideally suited for battery-powered handheld applications.

■ PACKAGE



BUMP CHIP

■ FEATURES

- 4,096-color STN LCD driver
- Built-in LCD Drivers : 128-common Drivers x 128RGB Drivers (384-segment Drivers in B&W)
: 2RGB Icon-drivers
- Built-in Display Data RAM (DDRAM) : 196,608 bits for Graphic Display
- Programmable Display Mode
 - Variable 16-grayscale Mode : 4,096 Colors
 - Variable 8-grayscale Mode : 256 Colors
 - Fixed 8-grayscale Mode : 256 Colors
 - B&W Mode : Black & White
- 8-/16-bit Parallel Interface Selectable
- 8-/16-bit Bus Length for Display Data Selectable
- 3-/4-line Serial Interface Selectable
- Programmable Duty Ratio and Bias Ratio
- Programmable Internal Voltage Booster : Maximum 6 times
- Programmable Contrast Control : 128-step Electrical Variable Resistor (EVR)
- LCD Bias Adjustment Circuit
- Various Useful Instructions
- Display-rotation Function / Mirror-inversion Function
- Low Operating Current : 450uA Typical at $V_{DD}=3V$, 4-time Boost, Checker Flag Display
- Low Logic Voltage : 1.7V to 3.3V
- Wide LCD Voltage Range : 5.0V to 18.0V
- C-MOS Technology
- Slim Chip for COG
- Package : Bump Chip / TCP

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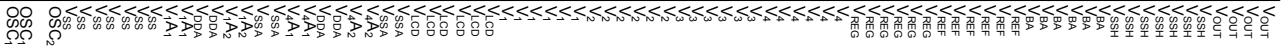
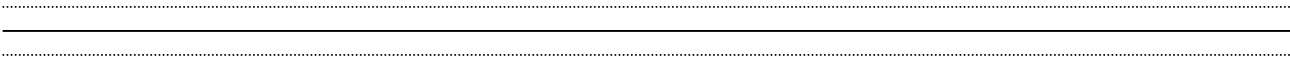
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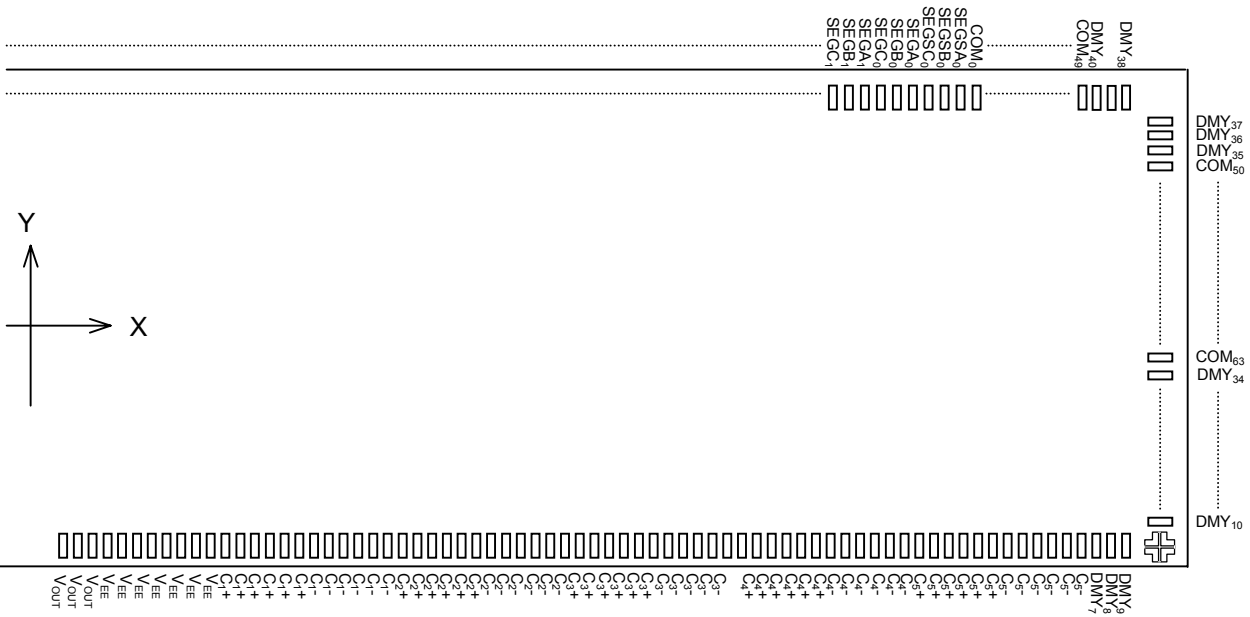
NOTE2) Dummy PADS, symbolized with DUMMY, are electrically open.

NOTE3) The purpose of this drawing is to show the order of PADs. Use "PAD COORDINATE TABLE 1 to 6" for design



Coordinates

A diagram of a square lattice structure composed of four L-shaped elements arranged in a 2x2 grid. The overall width and height of the lattice are labeled as c . The horizontal distance between the centerlines of the two columns is labeled d , and the vertical distance between the centerlines of the two rows is also labeled d . The width of each L-shaped element is labeled b , and the height of each L-shaped element is labeled a . Dashed lines indicate the centerlines and the boundaries of the elements. Arrows indicate the direction of forces: horizontal arrows pointing outwards from the top and bottom centerlines, and vertical arrows pointing inwards towards the left and right centerlines.



■ PAD COORDINATES 1

Chip Size : 22,070μm x 2,550μm (Center 0μm x 0μm)

No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)
1	DMY ₀	-10642.5	-1090.0	52	D ₁₀	-5584.5	-1090.0	103	V ₄ A ₂	-292.0	-1090.0
2	DMY ₁	-10599.5	-1090.0	53	D ₁₀	-5511.5	-1090.0	104	V _{SSA}	-182.5	-1090.0
3	DMY ₂	-10556.5	-1090.0	54	D ₁₁	-5365.5	-1090.0	105	V _{SSA}	-109.5	-1090.0
4	V _{SSA}	-10475.5	-1090.0	55	D ₁₁	-5292.5	-1090.0	106	V _{LCD}	0.0	-1090.0
5	V _{SSA}	-10402.5	-1090.0	56	D ₁₂	-5146.5	-1090.0	107	V _{LCD}	73.0	-1090.0
6	SEL68	-10293.0	-1090.0	57	D ₁₂	-5073.5	-1090.0	108	V _{LCD}	146.0	-1090.0
7	SEL68	-10220.0	-1090.0	58	D ₁₃	-4927.5	-1090.0	109	V _{LCD}	219.0	-1090.0
8	V _{DDA}	-10110.5	-1090.0	59	D ₁₃	-4854.5	-1090.0	110	V _{LCD}	292.0	-1090.0
9	V _{DDA}	-10037.5	-1090.0	60	D ₁₄	-4708.5	-1090.0	111	V _{LCD}	365.0	-1090.0
10	P/S	-9928.0	-1090.0	61	D ₁₄	-4635.5	-1090.0	112	V ₁	511.0	-1090.0
11	P/S	-9855.0	-1090.0	62	D ₁₅	-4489.5	-1090.0	113	V ₁	584.0	-1090.0
12	V _{SSA}	-9745.5	-1090.0	63	D ₁₅	-4416.5	-1090.0	114	V ₁	657.0	-1090.0
13	V _{SSA}	-9672.5	-1090.0	64	V _{DD}	-4197.5	-1090.0	115	V ₁	730.0	-1090.0
14	RESb	-9563.0	-1090.0	65	V _{DD}	-4124.5	-1090.0	116	V ₁	803.0	-1090.0
15	RESb	-9490.0	-1090.0	66	V _{DD}	-4051.5	-1090.0	117	V ₁	876.0	-1090.0
16	DMY ₃	-9380.5	-1090.0	67	V _{DD}	-3978.5	-1090.0	118	V ₂	1022.0	-1090.0
17	CSb	-9271.0	-1090.0	68	V _{DD}	-3905.5	-1090.0	119	V ₂	1095.0	-1090.0
18	CSb	-9198.0	-1090.0	69	V _{DD}	-3832.5	-1090.0	120	V ₂	1168.0	-1090.0
19	DMY ₄	-9088.5	-1090.0	70	V _{DD}	-3759.5	-1090.0	121	V ₂	1241.0	-1090.0
20	RS	-8979.0	-1090.0	71	CL	-3613.5	-1090.0	122	V ₂	1314.0	-1090.0
21	RS	-8906.0	-1090.0	72	CL	-3540.5	-1090.0	123	V ₂	1387.0	-1090.0
22	DMY ₅	-8796.5	-1090.0	73	FLM	-3394.5	-1090.0	124	V ₃	1533.0	-1090.0
23	WRb	-8687.0	-1090.0	74	FLM	-3321.5	-1090.0	125	V ₃	1606.0	-1090.0
24	WRb	-8614.0	-1090.0	75	FR	-3175.5	-1090.0	126	V ₃	1679.0	-1090.0
25	DMY ₆	-8504.5	-1090.0	76	FR	-3102.5	-1090.0	127	V ₃	1752.0	-1090.0
26	RDb	-8395.0	-1090.0	77	CLK	-2956.5	-1090.0	128	V ₃	1825.0	-1090.0
27	RDb	-8322.0	-1090.0	78	CLK	-2883.5	-1090.0	129	V ₃	1898.0	-1090.0
28	V _{DDA}	-8212.5	-1090.0	79	OSC ₁	-2701.0	-1090.0	130	V ₄	2044.0	-1090.0
29	V _{DDA}	-8139.5	-1090.0	80	OSC ₁	-2628.0	-1090.0	131	V ₄	2117.0	-1090.0
30	D ₀ /SCL	-7993.5	-1090.0	81	OSC ₂	-2409.0	-1090.0	132	V ₄	2190.0	-1090.0
31	D ₀ /SCL	-7920.5	-1090.0	82	OSC ₂	-2336.0	-1090.0	133	V ₄	2263.0	-1090.0
32	D ₁ /SDA	-7774.5	-1090.0	83	V _{SS}	-2044.0	-1090.0	134	V ₄	2336.0	-1090.0
33	D ₁ /SDA	-7701.5	-1090.0	84	V _{SS}	-1971.0	-1090.0	135	V ₄	2409.0	-1090.0
34	D ₂	-7555.5	-1090.0	85	V _{SS}	-1898.0	-1090.0	136	V _{REG}	2555.0	-1090.0
35	D ₂	-7482.5	-1090.0	86	V _{SS}	-1825.0	-1090.0	137	V _{REG}	2628.0	-1090.0
36	D ₃ /SMODE	-7336.5	-1090.0	87	V _{SS}	-1752.0	-1090.0	138	V _{REG}	2701.0	-1090.0
37	D ₃ /SMODE	-7263.5	-1090.0	88	V _{SS}	-1679.0	-1090.0	139	V _{REG}	2774.0	-1090.0
38	D ₄ /SPOL	-7117.5	-1090.0	89	V _{SS}	-1606.0	-1090.0	140	V _{REG}	2847.0	-1090.0
39	D ₄ /SPOL	-7044.5	-1090.0	90	V ₁ A ₁	-1460.0	-1090.0	141	V _{REF}	2920.0	-1090.0
40	D ₅	-6898.5	-1090.0	91	V ₁ A ₁	-1387.0	-1090.0	142	V _{REF}	3029.5	-1090.0
41	D ₅	-6825.5	-1090.0	92	V _{DDA}	-1277.5	-1090.0	143	V _{REF}	3102.5	-1090.0
42	D ₆	-6679.5	-1090.0	93	V _{DDA}	-1204.5	-1090.0	144	V _{REF}	3175.5	-1090.0
43	D ₆	-6606.5	-1090.0	94	V ₁ A ₂	-1095.0	-1090.0	145	V _{REF}	3248.5	-1090.0
44	D ₇	-6460.5	-1090.0	95	V ₁ A ₂	-1022.0	-1090.0	146	V _{REF}	3321.5	-1090.0
45	D ₇	-6387.5	-1090.0	96	V _{SSA}	-912.5	-1090.0	147	V _{REF}	3394.5	-1090.0
46	V _{SSA}	-6241.5	-1090.0	97	V _{SSA}	-839.5	-1090.0	148	V _{BA}	3504.0	-1090.0
47	V _{SSA}	-6168.5	-1090.0	98	V ₄ A ₁	-730.0	-1090.0	149	V _{BA}	3577.0	-1090.0
48	D ₈	-6022.5	-1090.0	99	V ₄ A ₁	-657.0	-1090.0	150	V _{BA}	3650.0	-1090.0
49	D ₈	-5949.5	-1090.0	100	V _{DDA}	-547.5	-1090.0	151	V _{BA}	3723.0	-1090.0
50	D ₉	-5803.5	-1090.0	101	V _{DDA}	-474.5	-1090.0	152	V _{BA}	3796.0	-1090.0
51	D ₉	-5730.5	-1090.0	102	V ₄ A ₂	-365.0	-1090.0	153	V _{BA}	3869.0	-1090.0

■ PAD COORDINATES 2

Chip Size : 22,070μm x 2,550μm (Center 0μm x 0μm)

No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)
154	V _{SSH}	4051.5	-1090.0	205	C ₃₋	8212.5	-1090.0	256	DMY ₂₈	10845.0	-107.5
155	V _{SSH}	4124.5	-1090.0	206	C ₃₋	8285.5	-1090.0	257	DMY ₂₉	10845.0	-64.5
156	V _{SSH}	4197.5	-1090.0	207	C ₃₋	8358.5	-1090.0	258	DMY ₃₀	10845.0	-21.5
157	V _{SSH}	4270.5	-1090.0	208	C ₃₋	8431.5	-1090.0	259	DMY ₃₁	10845.0	21.5
158	V _{SSH}	4343.5	-1090.0	209	C ₃₋	8504.5	-1090.0	260	DMY ₃₂	10845.0	64.5
159	V _{SSH}	4416.5	-1090.0	210	C ₃₋	8577.5	-1090.0	261	DMY ₃₃	10845.0	107.5
160	V _{SSH}	4489.5	-1090.0	211	C ₄₊	8687.0	-1090.0	262	DMY ₃₄	10845.0	150.5
161	V _{OUT}	4672.0	-1090.0	212	C ₄₊	8760.0	-1090.0	263	COM ₆₃	10845.0	193.5
162	V _{OUT}	4745.0	-1090.0	213	C ₄₊	8833.0	-1090.0	264	COM ₆₂	10845.0	236.5
163	V _{OUT}	4818.0	-1090.0	214	C ₄₊	8906.0	-1090.0	265	COM ₆₁	10845.0	279.5
164	V _{OUT}	4891.0	-1090.0	215	C ₄₊	8979.0	-1090.0	266	COM ₆₀	10845.0	322.5
165	V _{OUT}	4964.0	-1090.0	216	C ₄₊	9052.0	-1090.0	267	COM ₅₉	10845.0	365.5
166	V _{OUT}	5037.0	-1090.0	217	C ₄₋	9161.5	-1090.0	268	COM ₅₈	10845.0	408.5
167	V _{OUT}	5110.0	-1090.0	218	C ₄₋	9234.5	-1090.0	269	COM ₅₇	10845.0	451.5
168	V _{EE}	5292.5	-1090.0	219	C ₄₋	9307.5	-1090.0	270	COM ₅₆	10845.0	494.5
169	V _{EE}	5365.5	-1090.0	220	C ₄₋	9380.5	-1090.0	271	COM ₅₅	10845.0	537.5
170	V _{EE}	5438.5	-1090.0	221	C ₄₋	9453.5	-1090.0	272	COM ₅₄	10845.0	580.5
171	V _{EE}	5511.5	-1090.0	222	C ₄₋	9526.5	-1090.0	273	COM ₅₃	10845.0	623.5
172	V _{EE}	5584.5	-1090.0	223	C ₅₊	9636.0	-1090.0	274	COM ₅₂	10845.0	666.5
173	V _{EE}	5657.5	-1090.0	224	C ₅₊	9709.0	-1090.0	275	COM ₅₁	10845.0	709.5
174	V _{EE}	5730.5	-1090.0	225	C ₅₊	9782.0	-1090.0	276	COM ₅₀	10845.0	752.5
175	C ₁₊	5840.0	-1090.0	226	C ₅₊	9855.0	-1090.0	277	DMY ₃₅	10845.0	795.5
176	C ₁₊	5913.0	-1090.0	227	C ₅₊	9928.0	-1090.0	278	DMY ₃₆	10845.0	838.5
177	C ₁₊	5986.0	-1090.0	228	C ₅₊	10001.0	-1090.0	279	DMY ₃₇	10845.0	881.5
178	C ₁₊	6059.0	-1090.0	229	C ₅₋	10110.5	-1090.0	280	DMY ₃₈	10642.5	1085.0
179	C ₁₊	6132.0	-1090.0	230	C ₅₋	10183.5	-1090.0	281	DMY ₃₉	10599.5	1085.0
180	C ₁₊	6205.0	-1090.0	231	C ₅₋	10256.5	-1090.0	282	DMY ₄₀	10556.5	1085.0
181	C ₁₋	6314.5	-1090.0	232	C ₅₋	10329.5	-1090.0	283	COM ₄₉	10513.5	1085.0
182	C ₁₋	6387.5	-1090.0	233	C ₅₋	10402.5	-1090.0	284	COM ₄₈	10470.5	1085.0
183	C ₁₋	6460.5	-1090.0	234	C ₅₋	10475.5	-1090.0	285	COM ₄₇	10427.5	1085.0
184	C ₁₋	6533.5	-1090.0	235	DMY ₇	10556.5	-1090.0	286	COM ₄₆	10384.5	1085.0
185	C ₁₋	6606.5	-1090.0	236	DMY ₈	10599.5	-1090.0	287	COM ₄₅	10341.5	1085.0
186	C ₁₋	6679.5	-1090.0	237	DMY ₉	10642.5	-1090.0	288	COM ₄₄	10298.5	1085.0
187	C ₂₊	6789.0	-1090.0	238	DMY ₁₀	10845.0	-881.5	289	COM ₄₃	10255.5	1085.0
188	C ₂₊	6862.0	-1090.0	239	DMY ₁₁	10845.0	-838.5	290	COM ₄₂	10212.5	1085.0
189	C ₂₊	6935.0	-1090.0	240	DMY ₁₂	10845.0	-795.5	291	COM ₄₁	10169.5	1085.0
190	C ₂₊	7008.0	-1090.0	241	DMY ₁₃	10845.0	-752.5	292	COM ₄₀	10126.5	1085.0
191	C ₂₊	7081.0	-1090.0	242	DMY ₁₄	10845.0	-709.5	293	COM ₃₉	10083.5	1085.0
192	C ₂₊	7154.0	-1090.0	243	DMY ₁₅	10845.0	-666.5	294	COM ₃₈	10040.5	1085.0
193	C ₂₋	7263.5	-1090.0	244	DMY ₁₆	10845.0	-623.5	295	COM ₃₇	9997.5	1085.0
194	C ₂₋	7336.5	-1090.0	245	DMY ₁₇	10845.0	-580.5	296	COM ₃₆	9954.5	1085.0
195	C ₂₋	7409.5	-1090.0	246	DMY ₁₈	10845.0	-537.5	297	COM ₃₅	9911.5	1085.0
196	C ₂₋	7482.5	-1090.0	247	DMY ₁₉	10845.0	-494.5	298	COM ₃₄	9868.5	1085.0
197	C ₂₋	7555.5	-1090.0	248	DMY ₂₀	10845.0	-451.5	299	COM ₃₃	9825.5	1085.0
198	C ₂₋	7628.5	-1090.0	249	DMY ₂₁	10845.0	-408.5	300	COM ₃₂	9782.5	1085.0
199	C ₃₊	7738.0	-1090.0	250	DMY ₂₂	10845.0	-365.5	301	COM ₃₁	9739.5	1085.0
200	C ₃₊	7811.0	-1090.0	251	DMY ₂₃	10845.0	-322.5	302	COM ₃₀	9696.5	1085.0
201	C ₃₊	7884.0	-1090.0	252	DMY ₂₄	10845.0	-279.5	303	COM ₂₉	9653.5	1085.0
202	C ₃₊	7957.0	-1090.0	253	DMY ₂₅	10845.0	-236.5	304	COM ₂₈	9610.5	1085.0
203	C ₃₊	8030.0	-1090.0	254	DMY ₂₆	10845.0	-193.5	305	COM ₂₇	9567.5	1085.0
204	C ₃₊	8103.0	-1090.0	255	DMY ₂₇	10845.0	-150.5	306	COM ₂₆	9524.5	1085.0

■ PAD COORDINATES 3

Chip Size : 22,070μm x 2,550μm (Center 0μm x 0μm)

No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)
307	COM ₂₅	9481.5	1085.0	358	SEGB ₇	7288.5	1085.0	409	SEGB ₂₄	5095.5	1085.0
308	COM ₂₄	9438.5	1085.0	359	SEGC ₇	7245.5	1085.0	410	SEGC ₂₄	5052.5	1085.0
309	COM ₂₃	9395.5	1085.0	360	SEGA ₈	7202.5	1085.0	411	SEGA ₂₅	5009.5	1085.0
310	COM ₂₂	9352.5	1085.0	361	SEGB ₈	7159.5	1085.0	412	SEGB ₂₅	4966.5	1085.0
311	COM ₂₁	9309.5	1085.0	362	SEGC ₈	7116.5	1085.0	413	SEGC ₂₅	4923.5	1085.0
312	COM ₂₀	9266.5	1085.0	363	SEGA ₉	7073.5	1085.0	414	SEGA ₂₆	4880.5	1085.0
313	COM ₁₉	9223.5	1085.0	364	SEGB ₉	7030.5	1085.0	415	SEGB ₂₆	4837.5	1085.0
314	COM ₁₈	9180.5	1085.0	365	SEGC ₉	6987.5	1085.0	416	SEGC ₂₆	4794.5	1085.0
315	COM ₁₇	9137.5	1085.0	366	SEGA ₁₀	6944.5	1085.0	417	SEGA ₂₇	4751.5	1085.0
316	COM ₁₆	9094.5	1085.0	367	SEGB ₁₀	6901.5	1085.0	418	SEGB ₂₇	4708.5	1085.0
317	COM ₁₅	9051.5	1085.0	368	SEGC ₁₀	6858.5	1085.0	419	SEGC ₂₇	4665.5	1085.0
318	COM ₁₄	9008.5	1085.0	369	SEGA ₁₁	6815.5	1085.0	420	SEGA ₂₈	4622.5	1085.0
319	COM ₁₃	8965.5	1085.0	370	SEGB ₁₁	6772.5	1085.0	421	SEGB ₂₈	4579.5	1085.0
320	COM ₁₂	8922.5	1085.0	371	SEGC ₁₁	6729.5	1085.0	422	SEGC ₂₈	4536.5	1085.0
321	COM ₁₁	8879.5	1085.0	372	SEGA ₁₂	6686.5	1085.0	423	SEGA ₂₉	4493.5	1085.0
322	COM ₁₀	8836.5	1085.0	373	SEGB ₁₂	6643.5	1085.0	424	SEGB ₂₉	4450.5	1085.0
323	COM ₉	8793.5	1085.0	374	SEGC ₁₂	6600.5	1085.0	425	SEGC ₂₉	4407.5	1085.0
324	COM ₈	8750.5	1085.0	375	SEGA ₁₃	6557.5	1085.0	426	SEGA ₃₀	4364.5	1085.0
325	COM ₇	8707.5	1085.0	376	SEGB ₁₃	6514.5	1085.0	427	SEGB ₃₀	4321.5	1085.0
326	COM ₆	8664.5	1085.0	377	SEGC ₁₃	6471.5	1085.0	428	SEGC ₃₀	4278.5	1085.0
327	COM ₅	8621.5	1085.0	378	SEGA ₁₄	6428.5	1085.0	429	SEGA ₃₁	4235.5	1085.0
328	COM ₄	8578.5	1085.0	379	SEGB ₁₄	6385.5	1085.0	430	SEGB ₃₁	4192.5	1085.0
329	COM ₃	8535.5	1085.0	380	SEGC ₁₄	6342.5	1085.0	431	SEGC ₃₁	4149.5	1085.0
330	COM ₂	8492.5	1085.0	381	SEGA ₁₅	6299.5	1085.0	432	SEGA ₃₂	4106.5	1085.0
331	COM ₁	8449.5	1085.0	382	SEGB ₁₅	6256.5	1085.0	433	SEGB ₃₂	4063.5	1085.0
332	COM ₀	8406.5	1085.0	383	SEGC ₁₅	6213.5	1085.0	434	SEGC ₃₂	4020.5	1085.0
333	SEGSA ₀	8363.5	1085.0	384	SEGA ₁₆	6170.5	1085.0	435	SEGA ₃₃	3977.5	1085.0
334	SEGSB ₀	8320.5	1085.0	385	SEGB ₁₆	6127.5	1085.0	436	SEGB ₃₃	3934.5	1085.0
335	SEGSC ₀	8277.5	1085.0	386	SEGC ₁₆	6084.5	1085.0	437	SEGC ₃₃	3891.5	1085.0
336	SEGA ₀	8234.5	1085.0	387	SEGA ₁₇	6041.5	1085.0	438	SEGA ₃₄	3848.5	1085.0
337	SEGB ₀	8191.5	1085.0	388	SEGB ₁₇	5998.5	1085.0	439	SEGB ₃₄	3805.5	1085.0
338	SEGC ₀	8148.5	1085.0	389	SEGC ₁₇	5955.5	1085.0	440	SEGC ₃₄	3762.5	1085.0
339	SEGA ₁	8105.5	1085.0	390	SEGA ₁₈	5912.5	1085.0	441	SEGA ₃₅	3719.5	1085.0
340	SEGB ₁	8062.5	1085.0	391	SEGB ₁₈	5869.5	1085.0	442	SEGB ₃₅	3676.5	1085.0
341	SEGC ₁	8019.5	1085.0	392	SEGC ₁₈	5826.5	1085.0	443	SEGC ₃₅	3633.5	1085.0
342	SEGA ₂	7976.5	1085.0	393	SEGA ₁₉	5783.5	1085.0	444	SEGA ₃₆	3590.5	1085.0
343	SEGB ₂	7933.5	1085.0	394	SEGB ₁₉	5740.5	1085.0	445	SEGB ₃₆	3547.5	1085.0
344	SEGC ₂	7890.5	1085.0	395	SEGC ₁₉	5697.5	1085.0	446	SEGC ₃₆	3504.5	1085.0
345	SEGA ₂	7847.5	1085.0	396	SEGA ₂₀	5654.5	1085.0	447	SEGA ₃₇	3461.5	1085.0
346	SEGB ₃	7804.5	1085.0	397	SEGB ₂₀	5611.5	1085.0	448	SEGB ₃₇	3418.5	1085.0
347	SEGC ₃	7761.5	1085.0	398	SEGC ₂₀	5568.5	1085.0	449	SEGC ₃₇	3375.5	1085.0
348	SEGA ₄	7718.5	1085.0	399	SEGA ₂₁	5525.5	1085.0	450	SEGA ₃₈	3332.5	1085.0
349	SEGB ₄	7675.5	1085.0	400	SEGB ₂₁	5482.5	1085.0	451	SEGB ₃₈	3289.5	1085.0
350	SEGC ₄	7632.5	1085.0	401	SEGC ₂₁	5439.5	1085.0	452	SEGC ₃₈	3246.5	1085.0
351	SEGA ₅	7589.5	1085.0	402	SEGA ₂₂	5396.5	1085.0	453	SEGA ₃₉	3203.5	1085.0
352	SEGB ₅	7546.5	1085.0	403	SEGB ₂₂	5353.5	1085.0	454	SEGB ₃₉	3160.5	1085.0
353	SEGC ₅	7503.5	1085.0	404	SEGC ₂₂	5310.5	1085.0	455	SEGC ₃₉	3117.5	1085.0
354	SEGA ₆	7460.5	1085.0	405	SEGA ₂₃	5267.5	1085.0	456	SEGA ₄₀	3074.5	1085.0
355	SEGB ₆	7417.5	1085.0	406	SEGB ₂₃	5224.5	1085.0	457	SEGB ₄₀	3031.5	1085.0
356	SEGC ₆	7374.5	1085.0	407	SEGC ₂₃	5181.5	1085.0	458	SEGC ₄₀	2988.5	1085.0
357	SEGA ₇	7331.5	1085.0	408	SEGA ₂₄	5138.5	1085.0	459	SEGA ₄₁	2945.5	1085.0

■ PAD COORDINATES 4

Chip Size : 22,070μm x 2,550μm (Center 0μm x 0μm)

No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)
460	SEGB ₄₁	2902.5	1085.0	511	SEGB ₅₈	709.5	1085.0	562	SEGB ₇₅	-1483.5	1085.0
461	SEGC ₄₁	2859.5	1085.0	512	SEGC ₅₈	666.5	1085.0	563	SEGC ₇₅	-1526.5	1085.0
462	SEGA ₄₂	2816.5	1085.0	513	SEGA ₅₉	623.5	1085.0	564	SEGA ₇₆	-1569.5	1085.0
463	SEGB ₄₂	2773.5	1085.0	514	SEGB ₅₉	580.5	1085.0	565	SEGB ₇₆	-1612.5	1085.0
464	SEGC ₄₂	2730.5	1085.0	515	SEGC ₅₉	537.5	1085.0	566	SEGC ₇₆	-1655.5	1085.0
465	SEGA ₄₃	2687.5	1085.0	516	SEGA ₆₀	494.5	1085.0	567	SEGA ₇₇	-1698.5	1085.0
466	SEGB ₄₃	2644.5	1085.0	517	SEGB ₆₀	451.5	1085.0	568	SEGB ₇₇	-1741.5	1085.0
467	SEGC ₄₃	2601.5	1085.0	518	SEGC ₆₀	408.5	1085.0	569	SEGC ₇₇	-1784.5	1085.0
468	SEGA ₄₄	2558.5	1085.0	519	SEGA ₆₁	365.5	1085.0	570	SEGA ₇₈	-1827.5	1085.0
469	SEGB ₄₄	2515.5	1085.0	520	SEGB ₆₁	322.5	1085.0	571	SEGB ₇₈	-1870.5	1085.0
470	SEGC ₄₄	2472.5	1085.0	521	SEGC ₆₁	279.5	1085.0	572	SEGC ₇₈	-1913.5	1085.0
471	SEGA ₄₅	2429.5	1085.0	522	SEGA ₆₂	236.5	1085.0	573	SEGA ₇₉	-1956.5	1085.0
472	SEGB ₄₅	2386.5	1085.0	523	SEGB ₆₂	193.5	1085.0	574	SEGB ₇₉	-1999.5	1085.0
473	SEGC ₄₅	2343.5	1085.0	524	SEGC ₆₂	150.5	1085.0	575	SEGC ₇₉	-2042.5	1085.0
474	SEGA ₄₆	2300.5	1085.0	525	SEGA ₆₃	107.5	1085.0	576	SEGA ₈₀	-2085.5	1085.0
475	SEGB ₄₆	2257.5	1085.0	526	SEGB ₆₃	64.5	1085.0	577	SEGB ₈₀	-2128.5	1085.0
476	SEGC ₄₆	2214.5	1085.0	527	SEGC ₆₃	21.5	1085.0	578	SEGC ₈₀	-2171.5	1085.0
477	SEGA ₄₇	2171.5	1085.0	528	SEGA ₆₄	-21.5	1085.0	579	SEGA ₈₁	-2214.5	1085.0
478	SEGB ₄₇	2128.5	1085.0	529	SEGB ₆₄	-64.5	1085.0	580	SEGB ₈₁	-2257.5	1085.0
479	SEGC ₄₇	2085.5	1085.0	530	SEGC ₆₄	-107.5	1085.0	581	SEGC ₈₁	-2300.5	1085.0
480	SEGA ₄₈	2042.5	1085.0	531	SEGA ₆₅	-150.5	1085.0	582	SEGA ₈₂	-2343.5	1085.0
481	SEGB ₄₈	1999.5	1085.0	532	SEGB ₆₅	-193.5	1085.0	583	SEGB ₈₂	-2386.5	1085.0
482	SEGC ₄₈	1956.5	1085.0	533	SEGC ₆₅	-236.5	1085.0	584	SEGC ₈₂	-2429.5	1085.0
483	SEGA ₄₉	1913.5	1085.0	534	SEGA ₆₆	-279.5	1085.0	585	SEGA ₈₃	-2472.5	1085.0
484	SEGB ₄₉	1870.5	1085.0	535	SEGB ₆₆	-322.5	1085.0	586	SEGB ₈₃	-2515.5	1085.0
485	SEGC ₄₉	1827.5	1085.0	536	SEGC ₆₆	-365.5	1085.0	587	SEGC ₈₃	-2558.5	1085.0
486	SEGA ₅₀	1784.5	1085.0	537	SEGA ₆₇	-408.5	1085.0	588	SEGA ₈₄	-2601.5	1085.0
487	SEGB ₅₀	1741.5	1085.0	538	SEGB ₆₇	-451.5	1085.0	589	SEGB ₈₄	-2644.5	1085.0
488	SEGC ₅₀	1698.5	1085.0	539	SEGC ₆₇	-494.5	1085.0	590	SEGC ₈₄	-2687.5	1085.0
489	SEGA ₅₁	1655.5	1085.0	540	SEGA ₆₈	-537.5	1085.0	591	SEGA ₈₅	-2730.5	1085.0
490	SEGB ₅₁	1612.5	1085.0	541	SEGB ₆₈	-580.5	1085.0	592	SEGB ₈₅	-2773.5	1085.0
491	SEGC ₅₁	1569.5	1085.0	542	SEGC ₆₈	-623.5	1085.0	593	SEGC ₈₅	-2816.5	1085.0
492	SEGA ₅₂	1526.5	1085.0	543	SEGA ₆₉	-666.5	1085.0	594	SEGA ₈₆	-2859.5	1085.0
493	SEGB ₅₂	1483.5	1085.0	544	SEGB ₆₉	-709.5	1085.0	595	SEGB ₈₆	-2902.5	1085.0
494	SEGC ₅₂	1440.5	1085.0	545	SEGC ₆₉	-752.5	1085.0	596	SEGC ₈₆	-2945.5	1085.0
495	SEGA ₅₃	1397.5	1085.0	546	SEGA ₇₀	-795.5	1085.0	597	SEGA ₈₇	-2988.5	1085.0
496	SEGB ₅₃	1354.5	1085.0	547	SEGB ₇₀	-838.5	1085.0	598	SEGB ₈₇	-3031.5	1085.0
497	SEGC ₅₃	1311.5	1085.0	548	SEGC ₇₀	-881.5	1085.0	599	SEGC ₈₇	-3074.5	1085.0
498	SEGA ₅₄	1268.5	1085.0	549	SEGA ₇₁	-924.5	1085.0	600	SEGA ₈₈	-3117.5	1085.0
499	SEGB ₅₄	1225.5	1085.0	550	SEGB ₇₁	-967.5	1085.0	601	SEGB ₈₈	-3160.5	1085.0
500	SEGC ₅₄	1182.5	1085.0	551	SEGC ₇₁	-1010.5	1085.0	602	SEGC ₈₈	-3203.5	1085.0
501	SEGA ₅₅	1139.5	1085.0	552	SEGA ₇₂	-1053.5	1085.0	603	SEGA ₈₉	-3246.5	1085.0
502	SEGB ₅₅	1096.5	1085.0	553	SEGB ₇₂	-1096.5	1085.0	604	SEGB ₈₉	-3289.5	1085.0
503	SEGC ₅₅	1053.5	1085.0	554	SEGC ₇₂	-1139.5	1085.0	605	SEGC ₈₉	-3332.5	1085.0
504	SEGA ₅₆	1010.5	1085.0	555	SEGA ₇₃	-1182.5	1085.0	606	SEGA ₉₀	-3375.5	1085.0
505	SEGB ₅₆	967.5	1085.0	556	SEGB ₇₃	-1225.5	1085.0	607	SEGB ₉₀	-3418.5	1085.0
506	SEGC ₅₆	924.5	1085.0	557	SEGC ₇₃	-1268.5	1085.0	608	SEGC ₉₀	-3461.5	1085.0
507	SEGA ₅₇	881.5	1085.0	558	SEGA ₇₄	-1311.5	1085.0	609	SEGA ₉₁	-3504.5	1085.0
508	SEGB ₅₇	838.5	1085.0	559	SEGB ₇₄	-1354.5	1085.0	610	SEGB ₉₁	-3547.5	1085.0
509	SEGC ₅₇	795.5	1085.0	560	SEGC ₇₄	-1397.5	1085.0	611	SEGC ₉₁	-3590.5	1085.0
510	SEGA ₅₈	752.5	1085.0	561	SEGA ₇₅	-1440.5	1085.0	612	SEGA ₉₂	-3633.5	1085.0

■ PAD COORDINATES 5

Chip Size : 22,070μm x 2,550μm (Center 0μm x 0μm)

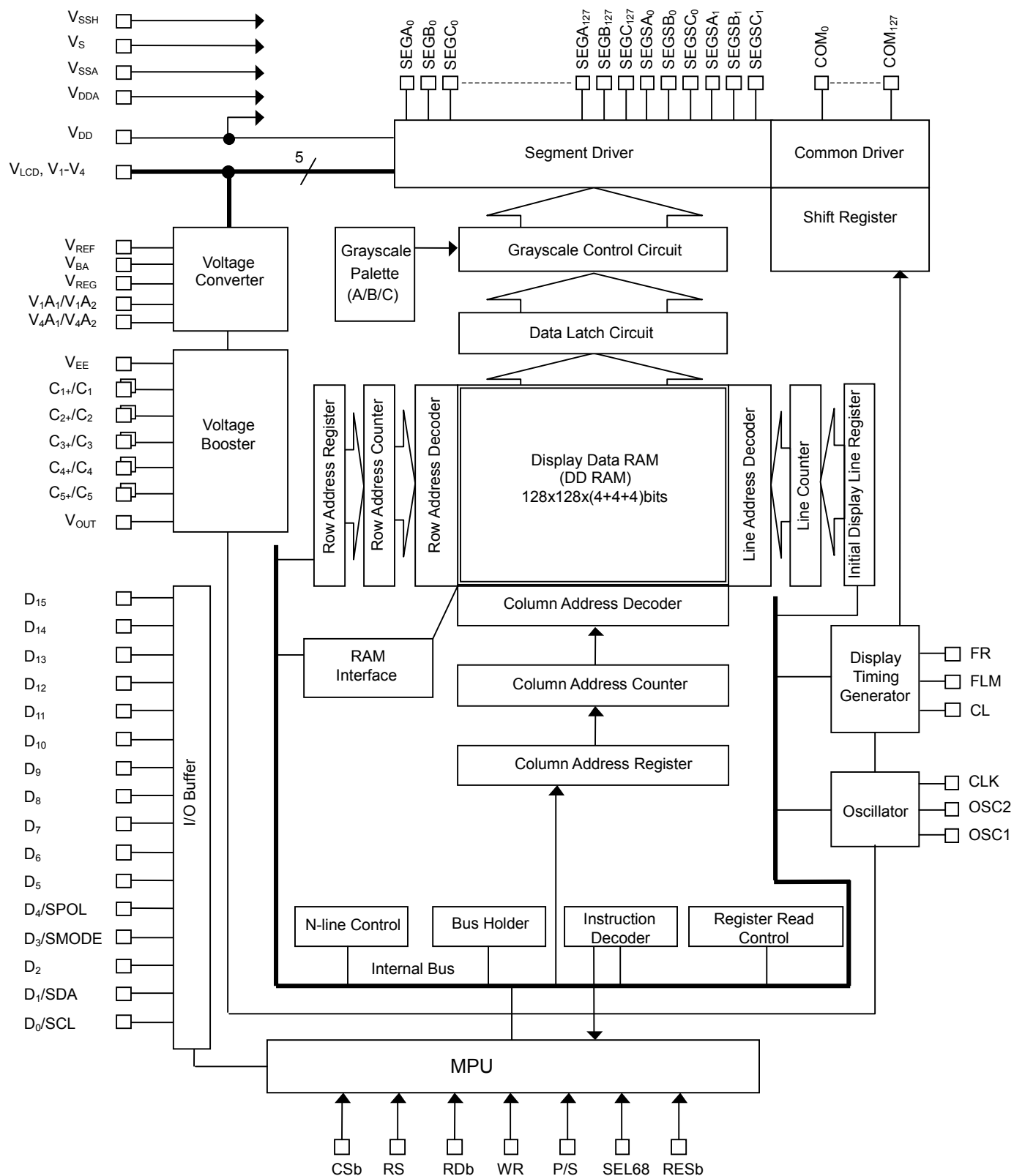
No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)	No.	PAD NAME	X(μm)	Y(μm)
613	SEGB ₉₂	-3676.5	1085.0	664	SEGB ₁₀₉	-5869.5	1085.0	715	SEGB ₁₂₆	-8062.5	1085.0
614	SEGC ₉₂	-3719.5	1085.0	665	SEGC ₁₀₉	-5912.5	1085.0	716	SEGC ₁₂₆	-8105.5	1085.0
615	SEGA ₉₃	-3762.5	1085.0	666	SEGA ₁₁₀	-5955.5	1085.0	717	SEGA ₁₂₇	-8148.5	1085.0
616	SEGB ₉₃	-3805.5	1085.0	667	SEGB ₁₁₀	-5998.5	1085.0	718	SEGB ₁₂₇	-8191.5	1085.0
617	SEGC ₉₃	-3848.5	1085.0	668	SEGC ₁₁₀	-6041.5	1085.0	719	SEGC ₁₂₇	-8234.5	1085.0
618	SEGA ₉₄	-3891.5	1085.0	669	SEGA ₁₁₁	-6084.5	1085.0	720	SEGA ₁₂₈	-8277.5	1085.0
619	SEGB ₉₄	-3934.5	1085.0	670	SEGB ₁₁₁	-6127.5	1085.0	721	SEGB ₁₂₈	-8320.5	1085.0
620	SEGC ₉₄	-3977.5	1085.0	671	SEGC ₁₁₁	-6170.5	1085.0	722	SEGC ₁₂₈	-8363.5	1085.0
621	SEGA ₉₅	-4020.5	1085.0	672	SEGA ₁₁₂	-6213.5	1085.0	723	COM ₆₄	-8406.5	1085.0
622	SEGB ₉₅	-4063.5	1085.0	673	SEGB ₁₁₂	-6256.5	1085.0	724	COM ₆₅	-8449.5	1085.0
623	SEGC ₉₅	-4106.5	1085.0	674	SEGC ₁₁₂	-6299.5	1085.0	725	COM ₆₆	-8492.5	1085.0
624	SEGA ₉₆	-4149.5	1085.0	675	SEGA ₁₁₃	-6342.5	1085.0	726	COM ₆₇	-8535.5	1085.0
625	SEGB ₉₆	-4192.5	1085.0	676	SEGB ₁₁₃	-6385.5	1085.0	727	COM ₆₈	-8578.5	1085.0
626	SEGC ₉₆	-4235.5	1085.0	677	SEGC ₁₁₃	-6428.5	1085.0	728	COM ₆₉	-8621.5	1085.0
627	SEGA ₉₇	-4278.5	1085.0	678	SEGA ₁₁₄	-6471.5	1085.0	729	COM ₇₀	-8664.5	1085.0
628	SEGB ₉₇	-4321.5	1085.0	679	SEGB ₁₁₄	-6514.5	1085.0	730	COM ₇₁	-8707.5	1085.0
629	SEGC ₉₇	-4364.5	1085.0	680	SEGC ₁₁₄	-6557.5	1085.0	731	COM ₇₂	-8750.5	1085.0
630	SEGA ₉₈	-4407.5	1085.0	681	SEGA ₁₁₅	-6600.5	1085.0	732	COM ₇₃	-8793.5	1085.0
631	SEGB ₉₈	-4450.5	1085.0	682	SEGB ₁₁₅	-6643.5	1085.0	733	COM ₇₄	-8836.5	1085.0
632	SEGC ₉₈	-4493.5	1085.0	683	SEGC ₁₁₅	-6686.5	1085.0	734	COM ₇₅	-8879.5	1085.0
633	SEGA ₉₉	-4536.5	1085.0	684	SEGA ₁₁₆	-6729.5	1085.0	735	COM ₇₆	-8922.5	1085.0
634	SEGB ₉₉	-4579.5	1085.0	685	SEGB ₁₁₆	-6772.5	1085.0	736	COM ₇₇	-8965.5	1085.0
635	SEGC ₉₉	-4622.5	1085.0	686	SEGC ₁₁₆	-6815.5	1085.0	737	COM ₇₈	-9008.5	1085.0
636	SEGA ₁₀₀	-4665.5	1085.0	687	SEGA ₁₁₇	-6858.5	1085.0	738	COM ₇₉	-9051.5	1085.0
637	SEGB ₁₀₀	-4708.5	1085.0	688	SEGB ₁₁₇	-6901.5	1085.0	739	COM ₈₀	-9094.5	1085.0
638	SEGC ₁₀₀	-4751.5	1085.0	689	SEGC ₁₁₇	-6944.5	1085.0	740	COM ₈₁	-9137.5	1085.0
639	SEGA ₁₀₁	-4794.5	1085.0	690	SEGA ₁₁₈	-6987.5	1085.0	741	COM ₈₂	-9180.5	1085.0
640	SEGB ₁₀₁	-4837.5	1085.0	691	SEGB ₁₁₈	-7030.5	1085.0	742	COM ₈₃	-9223.5	1085.0
641	SEGC ₁₀₁	-4880.5	1085.0	692	SEGC ₁₁₈	-7073.5	1085.0	743	COM ₈₄	-9266.5	1085.0
642	SEGA ₁₀₂	-4923.5	1085.0	693	SEGA ₁₁₉	-7116.5	1085.0	744	COM ₈₅	-9309.5	1085.0
643	SEGB ₁₀₂	-4966.5	1085.0	694	SEGB ₁₁₉	-7159.5	1085.0	745	COM ₈₆	-9352.5	1085.0
644	SEGC ₁₀₂	-5009.5	1085.0	695	SEGC ₁₁₉	-7202.5	1085.0	746	COM ₈₇	-9395.5	1085.0
645	SEGA ₁₀₃	-5052.5	1085.0	696	SEGA ₁₂₀	-7245.5	1085.0	747	COM ₈₈	-9438.5	1085.0
646	SEGB ₁₀₃	-5095.5	1085.0	697	SEGB ₁₂₀	-7288.5	1085.0	748	COM ₈₉	-9481.5	1085.0
647	SEGC ₁₀₃	-5138.5	1085.0	698	SEGC ₁₂₀	-7331.5	1085.0	749	COM ₉₀	-9524.5	1085.0
648	SEGA ₁₀₄	-5181.5	1085.0	699	SEGA ₁₂₁	-7374.5	1085.0	750	COM ₉₁	-9567.5	1085.0
649	SEGB ₁₀₄	-5224.5	1085.0	700	SEGB ₁₂₁	-7417.5	1085.0	751	COM ₉₂	-9610.5	1085.0
650	SEGC ₁₀₄	-5267.5	1085.0	701	SEGC ₁₂₁	-7460.5	1085.0	752	COM ₉₃	-9653.5	1085.0
651	SEGA ₁₀₅	-5310.5	1085.0	702	SEGA ₁₂₂	-7503.5	1085.0	753	COM ₉₄	-9696.5	1085.0
652	SEGB ₁₀₅	-5353.5	1085.0	703	SEGB ₁₂₂	-7546.5	1085.0	754	COM ₉₅	-9739.5	1085.0
653	SEGC ₁₀₅	-5396.5	1085.0	704	SEGC ₁₂₂	-7589.5	1085.0	755	COM ₉₆	-9782.5	1085.0
654	SEGA ₁₀₆	-5439.5	1085.0	705	SEGA ₁₂₃	-7632.5	1085.0	756	COM ₉₇	-9825.5	1085.0
655	SEGB ₁₀₆	-5482.5	1085.0	706	SEGB ₁₂₃	-7675.5	1085.0	757	COM ₉₈	-9868.5	1085.0
656	SEGC ₁₀₆	-5525.5	1085.0	707	SEGC ₁₂₃	-7718.5	1085.0	758	COM ₉₉	-9911.5	1085.0
657	SEGA ₁₀₇	-5568.5	1085.0	708	SEGA ₁₂₄	-7761.5	1085.0	759	COM ₁₀₀	-9954.5	1085.0
658	SEGB ₁₀₇	-5611.5	1085.0	709	SEGB ₁₂₄	-7804.5	1085.0	760	COM ₁₀₁	-9997.5	1085.0
659	SEGC ₁₀₇	-5654.5	1085.0	710	SEGC ₁₂₄	-7847.5	1085.0	761	COM ₁₀₂	-10040.5	1085.0
660	SEGA ₁₀₈	-5697.5	1085.0	711	SEGA ₁₂₅	-7890.5	1085.0	762	COM ₁₀₃	-10083.5	1085.0
661	SEGB ₁₀₈	-5740.5	1085.0	712	SEGB ₁₂₅	-7933.5	1085.0	763	COM ₁₀₄	-10126.5	1085.0
662	SEGC ₁₀₈	-5783.5	1085.0	713	SEGC ₁₂₅	-7976.5	1085.0	764	COM ₁₀₅	-10169.5	1085.0
663	SEGA ₁₀₉	-5826.5	1085.0	714	SEGA ₁₂₆	-8019.5	1085.0	765	COM ₁₀₆	-10212.5	1085.0

■ PAD COORDINATES 6

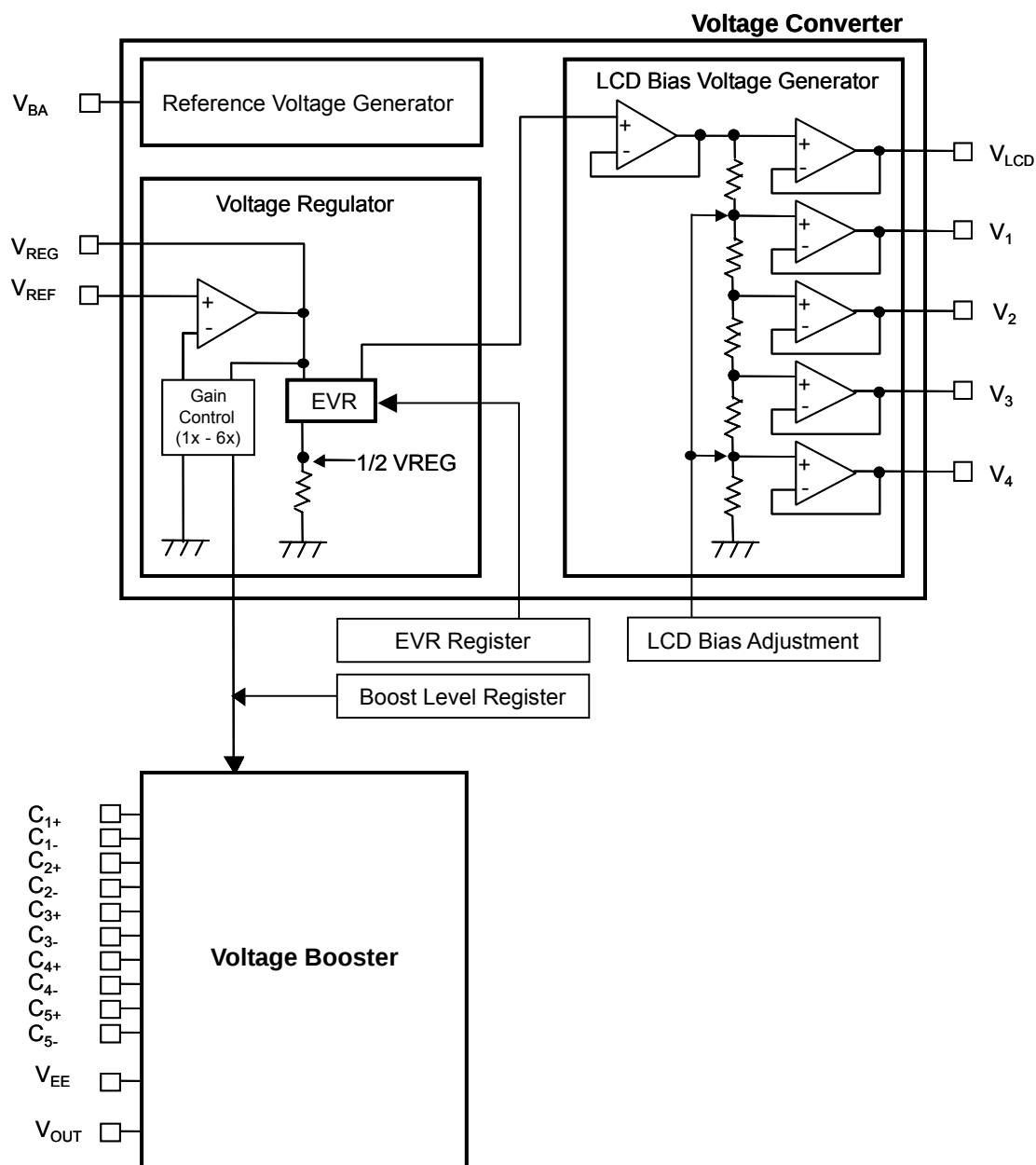
Chip Size : 22,070μm x 2,550μm (Center 0μm x 0μm)

No.	PAD NAME	X(um)	Y(um)	No.	PAD NAME	X(um)	Y(um)	No.	PAD NAME	X(um)	Y(um)
766	COM ₁₀₇	-10255.5	1085.0	817	DMY ₇₁	-10845.0	-881.5				
767	COM ₁₀₈	-10298.5	1085.0								
768	COM ₁₀₉	-10341.5	1085.0								
769	COM ₁₁₀	-10384.5	1085.0								
770	COM ₁₁₁	-10427.5	1085.0								
771	COM ₁₁₂	-10470.5	1085.0								
772	COM ₁₁₃	-10513.5	1085.0								
773	DMY ₄₁	-10556.5	1085.0								
774	DMY ₄₂	-10599.5	1085.0								
775	DMY ₄₃	-10642.5	1085.0								
776	DMY ₄₄	-10845.0	881.5								
777	DMY ₄₅	-10845.0	838.5								
778	DMY ₄₆	-10845.0	795.5								
779	COM ₁₁₄	-10845.0	752.5								
780	COM ₁₁₅	-10845.0	709.5								
781	COM ₁₁₆	-10845.0	666.5								
782	COM ₁₁₇	-10845.0	623.5								
783	COM ₁₁₈	-10845.0	580.5								
784	COM ₁₁₉	-10845.0	537.5								
785	COM ₁₂₀	-10845.0	494.5								
786	COM ₁₂₁	-10845.0	451.5								
787	COM ₁₂₂	-10845.0	408.5								
788	COM ₁₂₃	-10845.0	365.5								
789	COM ₁₂₄	-10845.0	322.5								
790	COM ₁₂₅	-10845.0	279.5								
791	COM ₁₂₆	-10845.0	236.5								
792	COM ₁₂₇	-10845.0	193.5								
793	DMY ₄₇	-10845.0	150.5								
794	DMY ₄₈	-10845.0	107.5								
795	DMY ₄₉	-10845.0	64.5								
796	DMY ₅₀	-10845.0	21.5								
797	DMY ₅₁	-10845.0	-21.5								
798	DMY ₅₂	-10845.0	-64.5								
799	DMY ₅₃	-10845.0	-107.5								
800	DMY ₅₄	-10845.0	-150.5								
801	DMY ₅₅	-10845.0	-193.5								
802	DMY ₅₆	-10845.0	-236.5								
803	DMY ₅₇	-10845.0	-279.5								
804	DMY ₅₈	-10845.0	-322.5								
805	DMY ₅₉	-10845.0	-365.5								
806	DMY ₆₀	-10845.0	-408.5								
807	DMY ₆₁	-10845.0	-451.5								
808	DMY ₆₂	-10845.0	-494.5								
809	DMY ₆₃	-10845.0	-537.5								
810	DMY ₆₄	-10845.0	-580.5								
811	DMY ₆₅	-10845.0	-623.5								
812	DMY ₆₆	-10845.0	-666.5								
813	DMY ₆₇	-10845.0	-709.5								
814	DMY ₆₈	-10845.0	-752.5								
815	DMY ₆₉	-10845.0	-795.5								
816	DMY ₇₀	-10845.0	-838.5								

■ BLOCK DIAGRAM



■ LCD POWER SUPPLY BLOCK DIAGRAM



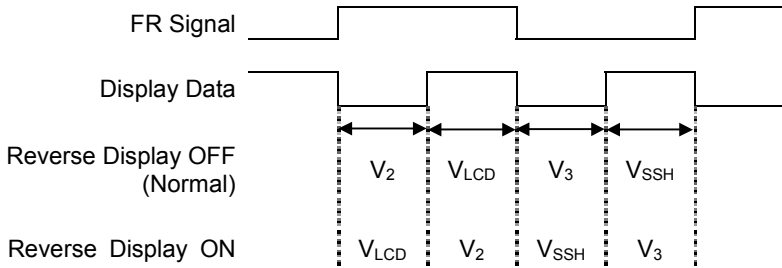
■ TERMINAL DESCRIPTION 1

No.	Terminal	I/O	Function		
64~70	V _{DD}	Power	Power Supply for Logic Circuits		
83~39	V _{SS}	Power	GND for Logic Circuits		
154~160	V _{SSH}	Power	GND for High Voltage Circuits		
8,9 28,29 92,93 100,101	V _{DDA}	Power	V _{DDA} is internally connected to V _{DD} to fix SEL68 or P/S to “H” if necessary, and cannot be used as main power supply. • V _{DDA} should be open if not used.		
4,5, 12,13 46,47 96,97 104,105	V _{SSA}	Power	V _{SSA} is internally connected to V _{SS} to fix SEL68 or P/S to “L” if necessary, and cannot be used as main GND. • V _{SSA} should be open if not used.		
106~111 112~117 118~123 124~129 130~135	V _{LCD} V ₁ V ₂ V ₃ V ₄	Power	LCD Bias Voltages • When the internal LCD power supply is used, internal LCD bias voltages (V _{LCD} and V ₁ -V ₄) are activated by the “Power Control” instruction. Stabilizing capacitors are required between each bias voltage and V _{SS} . • When the external LCD power supply is used, LCD bias voltages are externally supplied on V _{LCD} , V ₁ , V ₂ , V ₃ and V ₄ individually, with the following relation maintained: V _{SSH} <V ₄ <V ₃ <V ₂ <V ₁ <V _{LCD}		
175~180 181~186	C ₁₊ C ₁₋	Power	Capacitor Connection for Voltage Booster		
187~192 193~198	C ₂₊ C ₂₋	Power	Capacitor Connection for Voltage Booster		
199~204 205~210	C ₃₊ C ₃₋	Power	Capacitor Connection for Voltage Booster		
211~216 217~222	C ₄₊ C ₄₋	Power	Capacitor Connection for Voltage Booster		
223~228 229~234	C ₅₊ C ₅₋	Power	Capacitor Connection for Voltage Booster		
148~153	V _{BA}	Power	Reference-Voltage Generator Output		
142~147	V _{REF}	Power	Voltage Regulator Input		
168~174	V _{EE}	Power	Voltage Booster Input • V _{EE} is normally connected to V _{DD} .		
161~167	V _{OUT}	Power	Voltage Booster Output • Input if an external LCD power supply is used.		
136~141	V _{REG}	Power	Voltage Regulator Output		
90,91 94,95	V ₁ A ₁ V ₁ A ₂	I	V ₁ Bias Voltage Adjustment		
98,99 102,103	V ₄ A ₁ V ₄ A ₂	I	V ₄ Bias Voltage Adjustment		
14,15	RESb	I	Reset • Active “L”		
6,7	SEL68	I	MPU Mode Select		
			SEL86 MPU	H 68-series	L 80-series

■ TERMINAL DESCRIPTION 2

No.	Terminal	I/O	Function						
30,31	D ₀ /SCL	I/O	<u>Parallel Interface</u> D ₇ to D ₀ : 8-bit Bi-directional Bus • In the parallel interface mode (P/S="H"), D ₇ -D ₀ are connected to 8-bit bi-directional MPU bus. <u>Serial Interface</u> SDA : Serial Data SCL : Serial Clock SMODE : 3-/4-line Serial Mode Select SPOL : RS Polarity Select (3-line Serial Interface Mode) • In the 3 or 4-line serial interface mode (P/S="L"), D ₀ is assigned to SCL, and D ₁ to SDA. • In the 3-line serial interface mode, D ₄ is assigned to SPOL. • Serial data on SDA is latched at the rising edge of SCL signal in order of D ₇ , D ₆ ,... and D ₀ , and then converted into 8-bit parallel data at the timing of the internal signal produced from the 8 th SCL. • SCL should be set to "L" right after data transmission or during non-access.						
32,33	D ₁ /SDA	I/O							
36,37	D ₃ /SMODE	I/O							
38,39	D ₄ /SPOL	I/O							
34,35 40,41 42,43 44,45	D ₂ D ₅ D ₆ D ₇	I/O							
48,49 50,51 52,53 54,55 56,57 58,59 60,61 62,63	D ₈ D ₉ D ₁₀ D ₁₁ D ₁₂ D ₁₃ D ₁₄ D ₁₅	I/O	8-bit Bi-directional Bus • In the 16-bit bus length mode, D ₁₅ -D ₈ are assigned to upper 8-bit data bus. • In the serial interface mode or the 8-bit parallel interface mode, D ₁₅ -D ₈ should be fixed to "H" or "L".						
17,18	CSb	I	Chip Select • Active "L"						
20,21	RS	I	Register Select • This signal interprets transferred data as display data or instruction. <table><tr><td>RS</td><td>H</td><td>L</td></tr><tr><td>Data</td><td>Instruction</td><td>Display Data</td></tr></table>	RS	H	L	Data	Instruction	Display Data
RS	H	L							
Data	Instruction	Display Data							
26,27	RDb (E)	I	<u>80-series MPU Interface (P/S="H", SEL68="L")</u> Data Read (RDb) Signal • Active "L" <u>68-series MPU Interface (P/S="H", SEL68="H")</u> Enable Signal • Active "H"						
23,24	WRb (R/W)	I	<u>80-series MPU Interface (P/S="H", SEL68="L")</u> Data Write (WRb) Signal • Active "L" <u>68-series MPU Interface (P/S="H", SEL68="H")</u> Data Read or Write (R/W) Signal <table><tr><td>R/W</td><td>H</td><td>L</td></tr><tr><td>Status</td><td>Read</td><td>Write</td></tr></table>	R/W	H	L	Status	Read	Write
R/W	H	L							
Status	Read	Write							

■ TERMINAL DESCRIPTION 3

No.	Terminal	I/O	Function																		
10,11	P/S	I	Parallel/Serial Interface Mode Select <table><tr><th>P/S</th><th>Chip Select</th><th>Display / Instruction</th><th>Data</th><th>Read /Write</th><th>Serial Clock</th></tr><tr><td>H</td><td>CSb</td><td>RS</td><td>D₀ ~ D₇</td><td>RDb, WRb</td><td>-</td></tr><tr><td>L</td><td>CSb</td><td>RS</td><td>SDA (D₁)</td><td>Write Only</td><td>SCL (D₀)</td></tr></table> In the serial interface mode (P/S="L"), RDb, WRb, D₂ and D₅-D₁₅ should be fixed to "H" or "L",.	P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock	H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-	L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)
P/S	Chip Select	Display / Instruction	Data	Read /Write	Serial Clock																
H	CSb	RS	D ₀ ~ D ₇	RDb, WRb	-																
L	CSb	RS	SDA (D ₁)	Write Only	SCL (D ₀)																
71,72	CL	O	Line Clock CL is normally open.																		
73,74	FLM	O	First Line Maker FLM is normally open.																		
75,76	FR	O	Frame Rate FR is normally open.																		
77,78	CLK	O	Clock Output CLK is normally open.																		
79,80 81,82	OSC1 OSC2	I O	OSC - When the internal oscillator is used, fix OSC1 to "H" or "L" and leave OSC2 open. To attain more accurate frequency, connect OSC1 and OSC2 with an external resistor. - When the internal oscillator is not used, input external clock to OSC1 and leave OSC2 open.																		
336~719	SEGA ₀ ~SEGA ₁₂₇ SEGB ₀ ~SEGB ₁₂₇ SEGB ₀ ~SEGB ₁₂₇	O	Segment Drivers <table><tr><th>REV Register</th><th>OFF</th><th>ON</th></tr><tr><td>Normal</td><td>0</td><td>1</td></tr><tr><td>Reverse</td><td>1</td><td>0</td></tr></table> Segment drivers output the following voltage levels. <u>B/W Mode (Example)</u> 	REV Register	OFF	ON	Normal	0	1	Reverse	1	0									
REV Register	OFF	ON																			
Normal	0	1																			
Reverse	1	0																			
333 720 334 721 335 722	SEGSA ₀ SEGSA ₁ SEGSB ₀ SEGSB ₁ SEGSC ₀ SEGSC ₁	O	Icon Segment Drivers SEGSA₀~SEGSC₁ are used for icon display.																		
263~276 283~332 723~772 779~792	COM ₀ ~ COM ₁₂₇	O	Common Drivers Common drivers output the following voltage levels. <table><tr><th>Data</th><th>FR</th><th>Output Levels</th></tr><tr><td>H</td><td>H</td><td>V_{SSH}</td></tr><tr><td>L</td><td>H</td><td>V₁</td></tr><tr><td>H</td><td>L</td><td>V_{LCD}</td></tr><tr><td>L</td><td>L</td><td>V₄</td></tr></table>	Data	FR	Output Levels	H	H	V _{SSH}	L	H	V ₁	H	L	V _{LCD}	L	L	V ₄			
Data	FR	Output Levels																			
H	H	V _{SSH}																			
L	H	V ₁																			
H	L	V _{LCD}																			
L	L	V ₄																			

NOTE) DUMMY PADs: No. 1~3, 16, 19, 22, 25, 235~262, 277~282, 773~778, 793~817

■ FUNCTIONAL DESCRIPTION

(1) MPU INTERFACE

(1-1) Selection of Parallel/Serial Interface Mode

The P/S selects a parallel or a serial interface mode, as shown in Table 1. In the serial interface mode, neither display data in the DDRAM nor instruction data in the registers can be read out.

Table 1 Selection of Parallel/Serial Interface Mode

P/S	I/F Mode	CSb	RS	RDb	WRb	SEL68	SDA	SCL	Data
H	Parallel I/F	CSb	RS	RDb	WRb	SEL68			D ₇ -D ₀ (D ₁₅ -D ₀)
L	Serial I/F	CSb	RS	-	-	-	SDA	SCL	-

NOTE) “-” : Fix to “H” or “L”.

(1-2) Selection of MPU Mode

In the parallel interface mode, the SEL68 selects 68 or 80-series MPU mode, as shown in Table 2.

Table 2 Selection of MPU Mode

SEL68	MPU Mode	CSb	RS	RDb	WRb	Data
H	68-series MPU	CSb	RS	E	R/W	D ₇ -D ₀ (D ₁₅ -D ₀)
L	80-series MPU	CSb	RS	RDb	WRb	D ₇ -D ₀ (D ₁₅ -D ₀)

(1-3) Data Recognition

In the parallel interface mode, the data from MPU is interpreted as display data or instruction according to the combination of the RS, RDb and WRb (R/W) signals, as shown in Table 3.

Table 3 Data Recognition (Parallel Interface Mode)

RS	68-series	80-series		Function
	R/W	RDb	WRb	
H	H	L	H	Read Instruction
H	L	H	L	Write Instruction
L	H	L	H	Read Display Data
L	L	H	L	Write Display Data

(1-4) Selection of 3-/4-line Serial Interface Mode

In the serial interface mode, the SMODE selects 3- or 4-line serial interface mode, as shown in Table 4.

Table 4 Selection of 3-/4-line Serial Interface Mode

SMODE	Serial Interface Mode
H	3-line
L	4-line

(1-5) 4-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is inactive (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 8-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of D₇, D₆,..., and D₀, and converted into 8-bit parallel data at the timing of the internal signal produced from the 8th SCL signal. The data on the SDA is interpreted as display data or instruction according to the RS.

Table 5 Data Recognition (4-line Serial Interface)

RS	Data Recognition
H	Instruction
L	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 8-bit data transmission is completed. Fig 1 illustrates the interface timing of the 4-line serial interface mode.

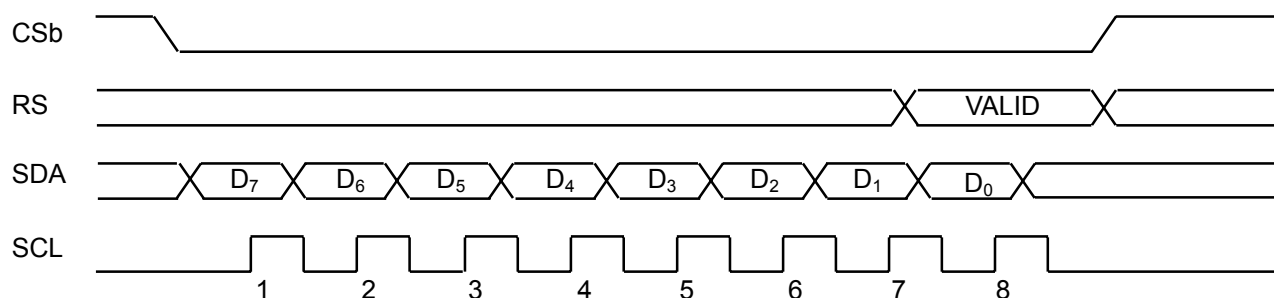


Fig 1 4-line Serial Interface Timing

(1-6) 3-line Serial Interface Mode

While the chip select is active (CSb=“L”), the SDA and SCL are enabled. While the chip select is not active (CSb=“H”), the SDA and SCL are disabled, and the internal shift register and the internal counter are being initialized. 9-bit serial data on the SDA is latched at the rising edge of the SCL signal in order of RS, D₇, D₆,..., and D₀, and then converted into 9-bit parallel data at the timing of the internal signal produced from the 9th SCL signal. The data on the SDA is interpreted as display data or instruction according to the combination of the RS bit and the SPOL status, as follows.

Table 6 Data Recognition (3-line Serial Interface)

SPOL=L		SPOL=H	
RS	Data Recognition	RS	Data Recognition
0	Display Data	0	Instruction
1	Instruction	1	Display Data

Note that the SCL should be set to “L” right after data transmission or during non-access because the serial interface is susceptible to external noises which may cause malfunctions. For added safety, inactivate the chip-select (CSb=“H”) temporary whenever 9-bit data transmission is completed. Fig 2 illustrates the interface timing of the 3-line serial interface mode.

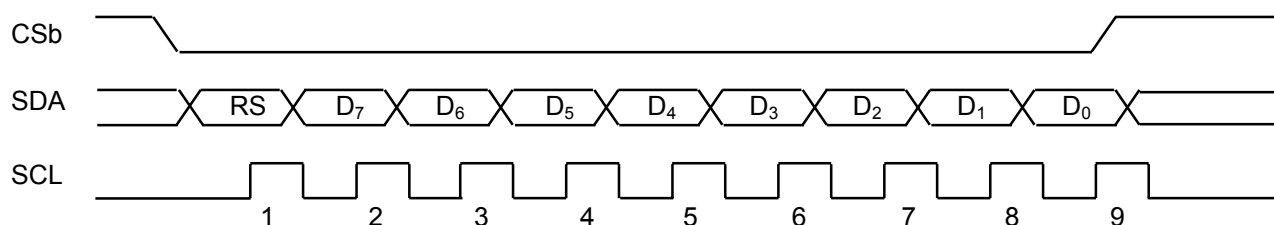


Fig 2 3-line Serial Interface Timing

(1-7) Accessing DDRAM

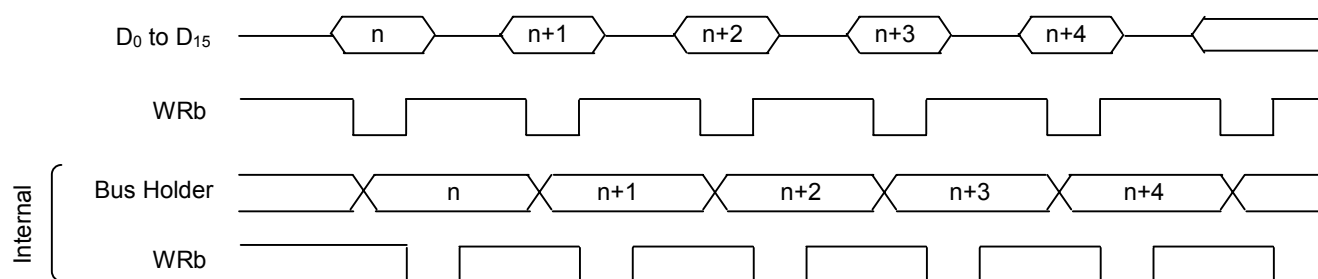
While the chip select is active (CSb="L"), the data from MPU can be written into the DDRAM or the instruction register. When the RS is "L", the data is interpreted as display data which is stored in the DDRAM. The display data is latched at the rising edge of the WRb signal in the 80-series MPU mode, or at the falling edge of the E signal in the 68-series MPU mode.

Table 7 Data Recognition

RS	Data Recognition
L	Display Data
H	Instruction

In the DDRAM read sequence, be sure to execute a dummy read right after setting an address or right after writing display data or instruction. The data from MPU is temporarily held in the internal bus-holder, then released on the internal data-bus, therefore a dummy data is read out by the 1st "Display Data Read" instruction. After that, the display data is read out from a specified address by the 2nd instruction. Note that the "Display Data Read" instruction cannot be used in the serial interface mode.

Display Data Write Operation



Display Data Read Operation

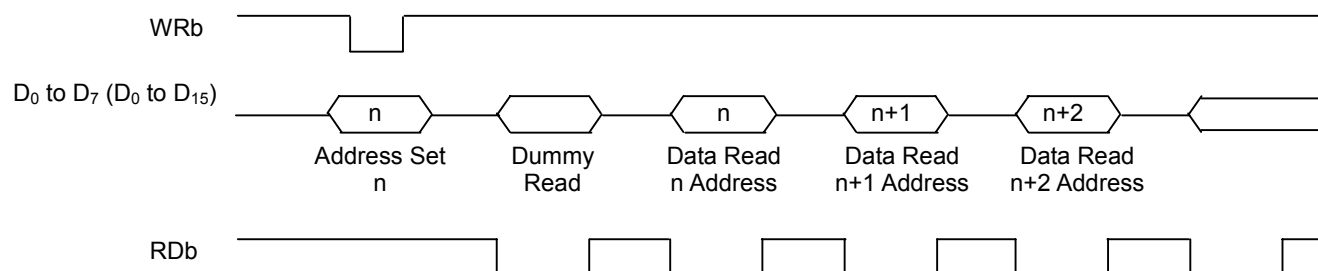


Fig 3 Internal-signal Timing of Display Data Read/Write Operations

NOTE) In 16-bit bus length mode, instruction is transmitted to/from instruction register in 16 bits, as well as display data.

(1-8) Accessing Instruction Register

Each instruction register has a specific address in between (0H) and (FH), and instruction data is read out from the register by the “Register Address” and “Register Read” instructions. For more information, refer to “(15-23) Register Address” and “(15-24) Register Read”.

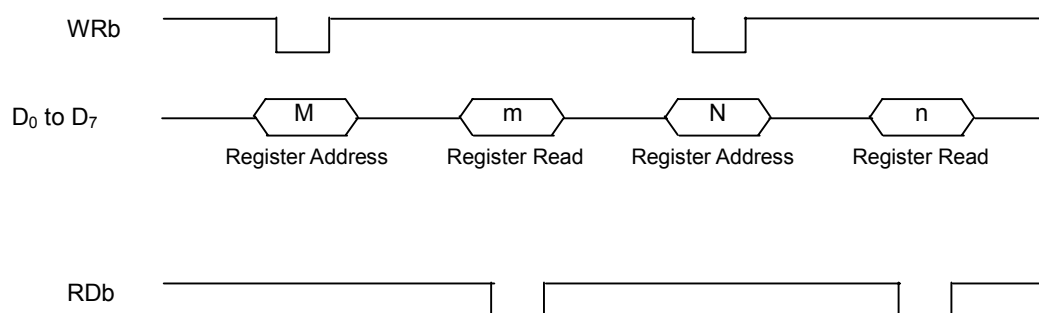


Fig 4 Access Timing of Instruction Register

(1-9) Selection of 8-/16-bit Bus Length (Parallel Interface Mode)

Either 8- or 16-bit bus length is selected by the D_0 (WLS) bit of the “Bus Length” instruction. In the 16-bit bus length mode, instruction as well as display data is transmitted to/from the instruction registers in 16 bits (D_{15} to D_0). However, only lower 8 bits (D_7 to D_0) are valid for instruction register access. And only 12 bits are actually stored in the DDRAM, even though entire 16 bits (D_{15} to D_0) are transmitted for DDRAM access. For more information, refer to “(4-4) Bit Assignment of Display Data”.

Table 8 Selection of 8-/16-bit Bus Length Mode

WLS	Bus Length Mode
L	8-bit Bus Length
H	16-bit Bus Length

(2) INITIAL DISPLAY LINE REGISTER

The address data in the initial display line register specifies the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. The initial COM is the start position of common scanning, which is specified by the “Initial COM” instruction.

The row address, which is established in the initial display line register, is preset into the line counter whenever the FLM becomes “H”. At the rising edge of the CL signal, the line counter is counted-up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit to decide a grayscale level, then the segment drivers A_i , B_i and C_i ($i=0$ to 127) generate LCD waveforms.

(3) COLUMN AND ROW ADDRESS COUNTERS

The column and row address counters designate a column address and a row address respectively for DDRAM access, but they are completely independent from the line counter. The line counter provides a line address which is synchronized with display control timings such as the FLM and the CL.

(4) DDRAM

(4-1) DDRAM Address Range

The DDRAM is capable of 128 bits for row address and 1,536 bits (12-bit x 128-segment) for column address. The range of the column address is from (00H) to (7FH), and the row address is from (00H) to (7FH). Setting outside these ranges is not allowed, otherwise it may cause malfunctions. For DDRAM access, two data transmissions are needed for 1 RGB-pixel in the 8-bit bus length mode, and one transmission in the 16-bit bus length mode.

8-bit Bus Length

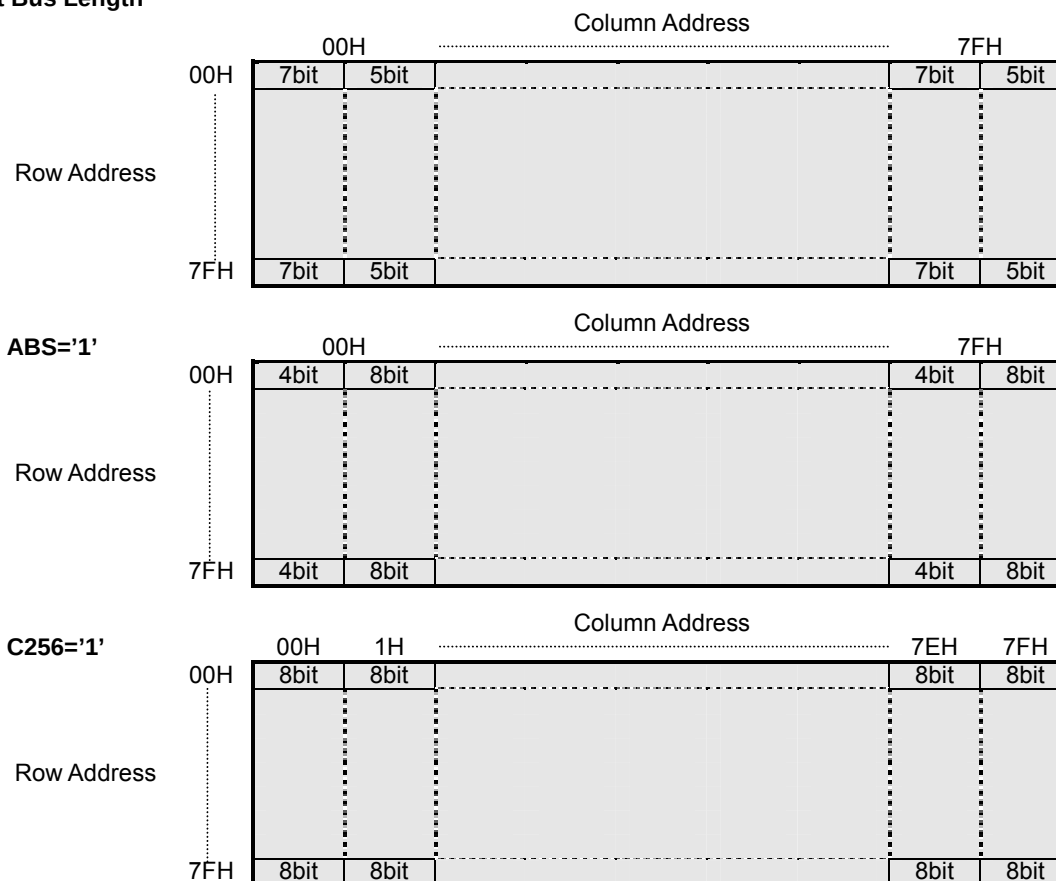


Fig 5 Range of Column Address in 8-bit Bus Length

16-bit Bus Length

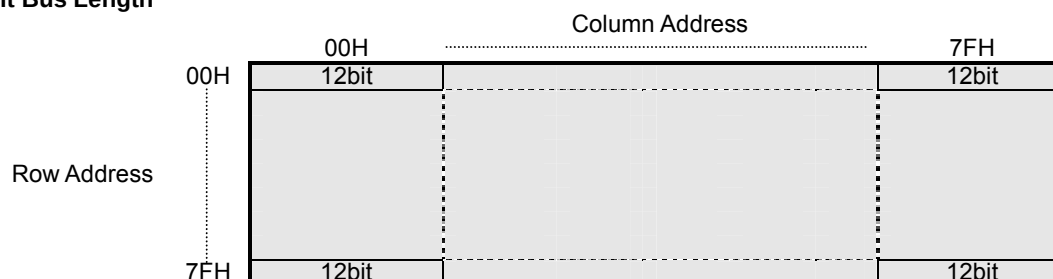


Fig 6 Range of Column Address in 16-bit Bus Length

(4-2) Window Area for DDRAM Access

Be sure to set up window area prior to DDRAM access. This area is set by the “Increment/Decrement Control” instruction and the designation of the start point and the end point.

By the “Increment/Decrement Control”, either auto-increment or -decrement is set for column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up or down, whenever the DDRAM is accessed. And, the start point is specified by the “Window Start Column Address” and “Window Start Row Address” instructions, and the end point by the “Window End Column Address” and “Window End Row Address” instructions. For more information, refer to “(15-9) Increment/Decrement Control”, “(15-25) Window End Column Address” and “(15-26) Window End Row Address”. The typical sequence of the window area setting is listed below.

1. Set D₂ (HV), D₁ (XD) and D₀ (YD) of “Increment/Decrement Control” instruction.
2. Set start point by “Window Start Column Address” and “Window Start Row Address” instructions.
3. Set end point by “Window End Column Address” and “Window End Row Address” instructions.
4. Window area is set up, and DDRAM can be accessed.

NOTE) The order of address setting is column address first, then row address.

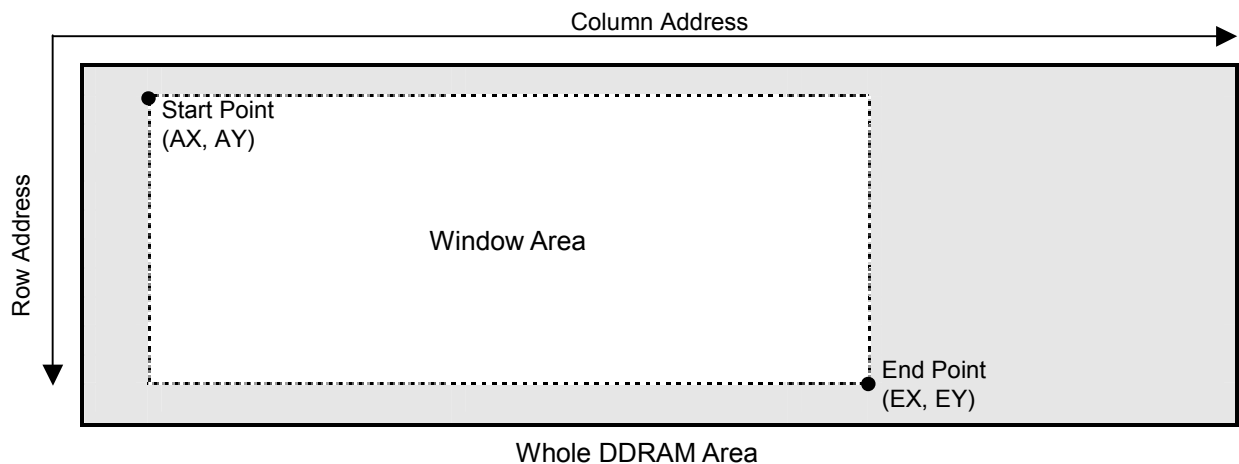


Fig 7 Window Area

NOTE1) The following relation should be maintained to avoid malfunctions.

- AX (Window Start Column Address) < EX (Window End Column Address) < Maximum Column Address
- AY (Window Start Row Address) < EY (Window End Row Address) < Maximum Row Address

NOTE2) The display-rotation function or the mirror-inversion function is enabled by this setting. Refer to “(4-3) DDRAM Access Direction”.

NOTE3) A read-modify-write operation is enabled by setting “1” at the D3 (AIM) of the “Increment/Decrement Control” instruction. Refer to the description about “AIM” bit in “(15-9) Increment/Decrement Control”.

(4-3) DDRAM Access Direction (Display-rotation and Mirror-inversion Functions)

The access direction of the DDRAM is selected out of eight options by setting the D_2 (HV), D_1 (XD) and D_0 (YD) bits of the “Increment/Decrement Control” instruction. This function allows the display data to be rotated 90, 180 or 270 degrees or mirror-inversed while being written onto the DDRAM. The following table shows the correspondences between instruction setting and on-screen image.

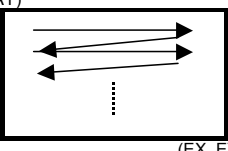
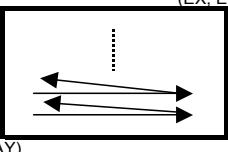
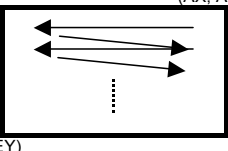
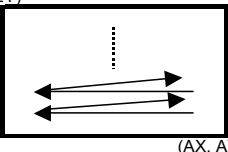
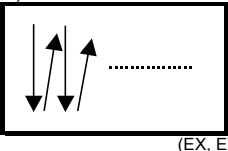
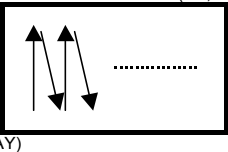
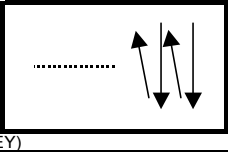
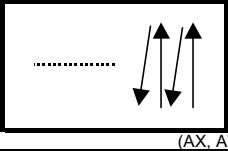
No.	HV	XD	YD	DDRAM Access Direction	On-screen Image	Valid Address
0	0	0	0			$AX < EX$ $AY < EY$
1	0	0	1			$AX < EX$ $AY > EY$
2	0	1	0			$AX > EX$ $AY < EY$
3	0	1	1			$AX > EX$ $AY > EY$
4	1	0	0			$AX < EX$ $AY < EY$
5	1	0	1			$AX < EX$ $AY > EY$
6	1	1	0			$AX > EX$ $AY < EY$
7	1	1	1			$AX > EX$ $AY > EY$

Fig 8 Display-rotation Function and Mirror-inverse Function

NOTE1) The same display data is used for each option's on-screen image. Only difference is “HV”, “XD” and “YD” bits setting.

NOTE2) The following relation must be maintained to avoid malfunctions.

AX (Window Start Column Address) $< EX$ (Window End Column Address) $<$ Maximum Column Address

AY (Window Start Row Address) $< EY$ (Window End Row Address) $<$ Maximum Row Address

(4-4) Bit Assignment of Display Data

(4-4-1) Bit Assignment Overview

These maps is used for grasping general outlines of the variations in the bit assignment of display data.

Table 9-1 DDRAM MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	C256	SEG ₀						SEG ₁						SEG ₁₂₆						SEG ₁₂₇					
				Palette A			Palette B			Palette C			Palette A			Palette B			Palette C			Palette A			Palette B		
				A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀
16bit	1	0	0	X=00H						X=01H						X=7EH						X=7FH					
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄
8bit	1	1	0	X=00H						X=01H						X=7EH						X=7FH					
				D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	0	0	0	X=00H (Upper)			X=00H (Lower)			X=01H (Upper)			X=01H (Lower)			X=7EH (Upper)			X=7EH (Lower)			X=7FH (Upper)			X=7FH (Lower)		
				D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄
	0	1	0	X=00H (Upper)			X=00H (Lower)			X=01H (Upper)			X=01H (Lower)			X=7EH (Upper)			X=7EH (Lower)			X=7FH (Upper)			X=7FH (Lower)		
				D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Table 9-2 DDRAM MAP 2 (Variable 8-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	WLS	ABS	C256	SEG ₀						SEG ₁						SEG ₁₂₆						SEG ₁₂₇					
				Palette A			Palette B			Palette C			Palette A			Palette B			Palette C			Palette A			Palette B		
				A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀
8bit				X=00H						X=01H						X=7EH						X=7FH					
				D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄
	0	X	1	-	-	-	-	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	-	-	-	-	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Table 10 SWAP

SWAP	Palette A				Palette B				Palette C			
	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀
0	SEGAX				SEGBX				SEGCX			
1	SEGCX				SEGBX				SEGAX			

NOTE1) On the RAM MAP 2, A₀, B₀, C₁ and C₀ bits are fixed to "1".
NOTE2) The functions of the variable 8-grayscale mode are different from those of the fixed 8-grayscale mode.
NOTE3) The contents of the DDRAM at "C256=0" are not compatible with the contents at "C256=1".
NOTE4) "C256=1" can be used in the 8-bit bus length mode, but not in the 16-bit bus length mode.
NOTE5) In the 8-bit bus length mode at "C256=0", odd accesses are prohibited because display data for 1 pixel is completed in successive two accesses.
NOTE6) In the 8-bit bus length mode at "C256=0", write upper bits first, then lower bits. This order is always adopted regardless of the "HV", "XD" and "YD" bits.

(4-4-2) Bit Assignment in Variable 16-grayscale Mode (DDRAM)

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H												↔	X=7FH											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H												↔	X=7FH											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H												↔	X=7FH											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H												↔	X=7FH											
Display Data in DDRAM Grayscale Palette Segment Driver		D ¹¹	D ¹⁰	D ⁹	D ⁸	D ⁷	D ⁶	D ⁵	D ⁴	D ³	D ²	D ¹	D ⁰	↕	D ¹¹	D ¹⁰	D ⁹	D ⁸	D ⁷	D ⁶	D ⁵	D ⁴	D ³	D ²	D ¹	D ⁰
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H(Upper)								X=00H(Lower)				↔	X=7FH(Upper)								X=7FH(Lower)			
Display Data in DDRAM Grayscale Palette Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H(Upper)								X=00H(Lower)				↔	X=7FH(Upper)								X=7FH(Lower)			
Display Data in DDRAM Grayscale Palette Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H (Upper)				X=00H(Lower)								↔	X=7FH (Upper)				X=7FH(Lower)							
Display Data in DDRAM Grayscale Palette Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H (Upper)				X=00H(Lower)								↔	X=7FH (Upper)				X=7FH(Lower)							
Display Data in DDRAM Grayscale Palette Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

(4-4-3) Bit Assignment in variable 8-grayscale Mode (DDRAM)

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																	
*	0	X=00H								↔	X=7FH								
Display Data in DDRAM Grayscale Palette Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		Palette A			Palette B			Palette C			↔	Palette A			Palette B			Palette C	
		SEGA ₀			SEGB ₀			SEGC ₀			↔	SEGA ₁₂₇			SEGB ₁₂₇			SEGC ₁₂₇	

ABS	SWAP	Column Address / Display Data / Segment Driver																	
*	1	X=00H								↔	X=7FH								
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		Palette A			Palette B			Palette C			↔	Palette A			Palette B			Palette C	
		SEGC ₀			SEGB ₀			SEGA ₀			↔	SEGC ₁₂₇			SEGB ₁₂₇			SEGA ₁₂₇	

(4-4-4) Bit Assignment in Fixed 8-grayscale Mode (DDRAM)

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H												↔	X=7FH											
Display Data in DDRAM		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H												↔	X=7FH											
Display Data in DDRAM		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) are invalid.

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H												↔	X=7FH											
Display Data in DDRAM		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H												↔	X=7FH											
Display Data in DDRAM	Grayscale Palette Segment Driver	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H(Upper)				X=00H(Lower)				↔	X=7FH Upper)				X=7FH(Lower)											
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↕	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
		Grayscale Palette Segment Driver				Palette A		Palette B		Palette C		↔	Palette A		Palette B		Palette C									
		SEGA ₀				SEGB ₀		SEGC ₀		↔	SEGA ₁₂₇		SEGB ₁₂₇		SEGC ₁₂₇											

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H(Upper)				X=00H(Lower)				↔	X=7FH(Upper)				X=7FH(Lower)											
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁
	Grayscale Palette Segment Driver	Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid.

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H (Upper)				X=00H(Lower)				↔	X=7FH (Upper)				X=7FH(Lower)											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H (Upper)				X=00H(Lower)				↔	X=7FH (Upper)				X=7FH(Lower)											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
*	0	X=00H								↔	X=7FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀								
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																
*	1	X=00H								↔	X=7FH							
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Grayscale Palette				Grayscale Palette				↔	Grayscale Palette				Grayscale Palette			
Segment Driver		SEGC ₀				SEGB ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇			
		SEGA ₀				SEGB ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇			

(4-4-5) Bit Assignment in B&W Mode (DDRAM)

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	0	X=00H								↔	X=7FH															
Display Data in DDRAM		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
0	1	X=00H								↔	X=7FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁	↔	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H								↔	X=7FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H								↔	X=7FH															
Display Data in DDRAM	Grayscale Palette Segment Driver	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↔	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

ABS	SWAP	Column Address / Display Data / Segment Driver							
0	0	X=00H(Upper)			X=00H(Lower)	←→	X=7FH(Upper)		
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette Segment Driver		Palette A	Palette B	Palette C	←→	←→	←→	←→	←→
		SEGA ₀	SEGB ₀	SEGC ₀	←→	←→	SEGA ₁₂₇	SEGB ₁₂₇	SEGC ₁₂₇

ABS	SWAP	Column Address / Display Data / Segment Driver							
0	1	X=00H(Upper)			X=00H(Lower)	←→	X=7FH(Upper)		
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette Segment Driver		Palette A	Palette B	Palette C	←→	←→	←→	←→	←→
		SEGC ₀	SEGB ₀	SEGA ₀	←→	←→	SEGC ₁₂₇	SEGB ₁₂₇	SEGA ₁₂₇

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	0	X=00H (Upper)				X=00H(Lower)				↔	X=7FH (Upper)				X=7FH(Lower)											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGA ₀				SEGB ₀				SEGC ₀				↔	SEGA ₁₂₇				SEGB ₁₂₇				SEGC ₁₂₇			

ABS	SWAP	Column Address / Display Data / Segment Driver																								
1	1	X=00H (Upper)				X=00H(Lower)				↔	X=7FH (Upper)				X=7FH(Lower)											
Display Data in DDRAM Grayscale Palette Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	↕	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				↔	Palette A				Palette B				Palette C			
		SEGC ₀				SEGB ₀				SEGA ₀				↔	SEGC ₁₂₇				SEGB ₁₂₇				SEGA ₁₂₇			

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

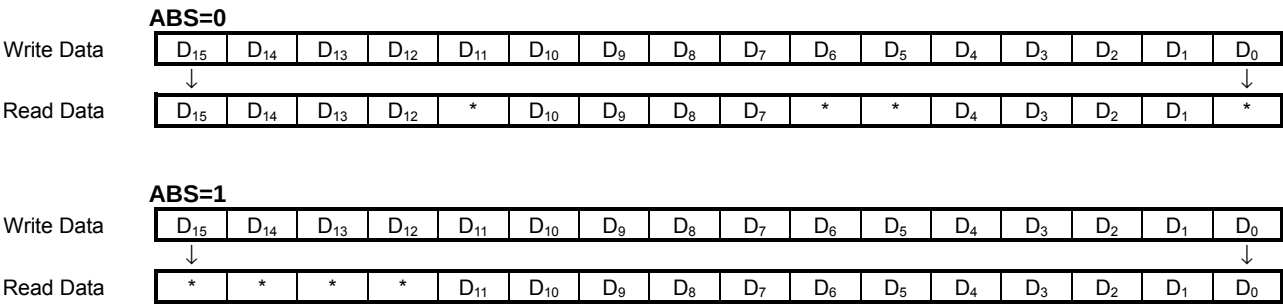
ABS	SWAP	Column Address / Display Data / Segment Driver							
*	0	X=00H				←→	X=7FH		
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette Segment Driver		Palette A	Palette B	Palette C	←→	←→	←→	←→	←→
		SEGA ₀	SEGB ₀	SEGC ₀	←→	←→	SEGA ₁₂₇	SEGB ₁₂₇	SEGC ₁₂₇

ABS	SWAP	Column Address / Display Data / Segment Driver							
*	1	X=00H				←→	X=7FH		
Display Data in DDRAM		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Grayscale Palette Segment Driver		Palette A	Palette B	Palette C	←→	←→	←→	←→	←→
		SEGC ₀	SEGB ₀	SEGA ₀	←→	←→	SEGC ₁₂₇	SEGB ₁₂₇	SEGA ₁₂₇

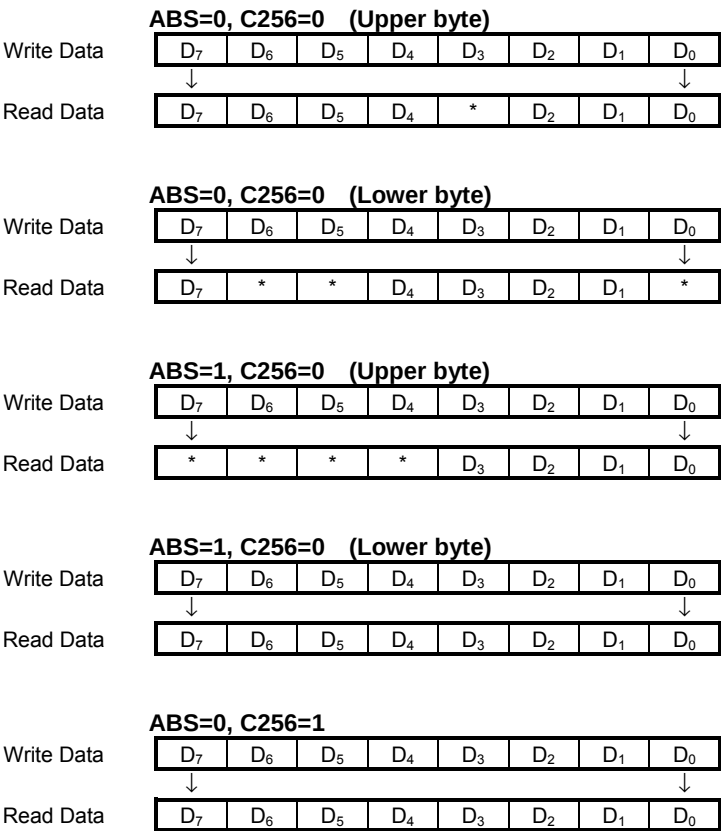
NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(4-4-6) Write Data and Read Data

16-bit Bus Length



8-bit Bus Length



NOTE) * : Invalid Data

(5) GRAYSCALE CONTROL CIRCUIT

(5-1) Display Mode Selection

A display mode is selected by the combination of the D₂ (MON) bit of the “Display Control (1)” instruction and the D₃ (PWM) and D₂ (C256) bits of the “Display Mode Control” instruction, as shown below.

Table 11 Display Mode Selection

MON	PWM	C256 (NOTE1)	Display Mode		Bus Length		Oscillation (NOTE2)
0	0	0	Variable 16-grayscale Mode	4096 Colors	8-/16-bit	(WLS=0/1)	f _{OSC1}
		1	Variable 8-grayscale Mode	256 Colors	8-bit	(WLS=0)	
	1	0	Fixed 8-grayscale Mode	256 Colors	8-/16-bit	(WLS=0/1)	f _{OSC2}
		1			8-bit	(WLS=0)	
1	*	0	B&W Mode	Black & White	8-/16-bit	(WLS=0/1)	f _{OSC3}
		1			8-bit	(WLS=0)	

NOTE1) In the variable grayscale mode, “C256” bit selects either 16-grayscale (4K colors) or 8-grayscale (256 colors). When C256=“0” (16-grayscale), all 12 bits are assigned to 1 RGB-pixel. When C256=“1” (8-grayscale), only 8 bits are assigned and the 8-bit bus length should be used. In the fixed 8-grayscale mode or the B&W mode, the “C256” bit is usually “1”. For more information how the display data is assigned, refer to “(4-4) Bit Assignment of Display Data”.

NOTE2) Oscillation frequency is decided according to the display mode, and is fine-tuned by the “Frequency Control” Instruction. Refer to “(11) OSCILLATOR” and “OSCILLATION FREQUENCY AND FRAME FREQUENCY”.

(5-1-1) Variable 16-grayscale Mode

In this mode, each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 16 from 32 grayscales (0/31-31/31) by setting palette data in the grayscale palette. Then, each of the segment drivers SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127) generates 16 grayscales to achieve 4,096 colors. Refer to Table 12-1 and Table 12-2.

(5-1-2) Variable 8-grayscale Mode

Each of the palettes A_j, B_j and C_j (j=0-15) is capable of selecting 8 from 32 grayscales (0/31-31/31). 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127)) generate 8 grayscales, and the other driver does 4 grayscales to achieve 256 colors. Refer to Table 13-1 through Table 13-4. The 8-bit bus length is usually used in this mode.

(5-1-3) Fixed 8-grayscale Mode

The palette setting is not necessary, because the palettes A_j, B_j and C_j (j=0-15) are always fixed at 4 or 8 grayscales between 0/7 and 7/7. 2 segment drivers of 1 RGB-group (SEG_{Ai}, SEG_{Bi} and SEG_{Ci} (i=0 to 127)) are fixed at 8 grayscales, and the other driver is 4 grayscales, then results in 256 colors. Refer to Table 14-1 and Table 14-2.

(5-1-4) B&W Mode

The palette setting is not necessary, where the only MSB bits of display data are valid. Refer to Table 15.

(6) GRAYSCALE PALETTE

(6-1) Grayscale Selection in Variable 16-grayscale Mode

Table 12-1 Grayscale selection

(Palette Aj, Bj, and Cj)

Display Data MSB----LSB	Palette Name
0 0 0 0	Palette A0/B0/C0
0 0 0 1	Palette A1/B1/C1
0 0 1 0	Palette A2/B2/C2
0 0 1 1	Palette A3/B3/C3
0 1 0 0	Palette A4/B4/C4
0 1 0 1	Palette A5/B5/C5
0 1 1 0	Palette A6/B6/C6
0 1 1 1	Palette A7/B7/C7
1 0 0 0	Palette A8/B8/C8
1 0 0 1	Palette A9/B9/C9
1 0 1 0	Palette A10/B10/C10
1 0 1 1	Palette A11/B11/C11
1 1 0 0	Palette A12/B12/C12
1 1 0 1	Palette A13/B13/C13
1 1 1 0	Palette A14/B14/C14
1 1 1 1	Palette A15/B15/C15

Table 12-2 Grayscale Palette

(Palette Aj, Bj, and Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0	Palette A0/B0/C0	1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	Palette A8/B8/C8
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31	Palette A2/B2/C2	1 0 1 0 1	21/31	Palette A10/B10/C10
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31	Palette A4/B4/C4	1 1 0 0 1	25/31	Palette A12/B12/C12
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31	Palette A6/B6/C6	1 1 1 0 1	29/31	Palette A14/B14/C14
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=0"

NOTE2) Applied to palette Aj, Bj and Cj (j=0 to 15)

(6-2) Grayscale Selection in Variable 8-grayscale Mode

Table 13-1 Grayscale selection

(Palette Aj and Bj)

Display Data MSB---LSB	Palette Name
0 0 0 *	Palette A1/B1/C1
0 0 1 *	Palette A3/B3/C3
0 1 0 *	Palette A5/B5/C5
0 1 1 *	Palette A7/B7/C7
1 0 0 *	Palette A9/B9/C9
1 0 1 *	Palette A11/B11/C11
1 1 0 *	Palette A13/B13/C13
1 1 1 *	Palette A15/B15/C15

Table 13-2 Grayscale Palette

(Palette Aj and Bj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31	Palette A1/B1/C1	1 0 0 1 1	19/31	Palette A9/B9/C9
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31	Palette A5/B5/C5	1 1 0 1 1	27/31	Palette A13/B13/C13
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1".

NOTE2) Applied to palette Aj and Bj (j=0 to 15)

NOTE3) Palette 0, 2, 4, 6, 8, 10, 12 and 14 are disabled.

Table 13-3 Grayscale selection

(Palette Cj)

Display Data MSB---LSB	Palette Name
0 0 **	Palette A3/B3/C3
0 1 **	Palette A7/B7/C7
1 0 **	Palette A11/B11/C11
1 1 **	Palette A15/B15/C15

Table 13-4 Grayscale Palette

(Palette Cj)

Palette Data MSB---LSB	Grayscale	Default Setting	Palette Data MSB---LSB	Grayscale	Default Setting
0 0 0 0 0	0		1 0 0 0 0	16/31	
0 0 0 0 1	1/31		1 0 0 0 1	17/31	
0 0 0 1 0	2/31		1 0 0 1 0	18/31	
0 0 0 1 1	3/31		1 0 0 1 1	19/31	
0 0 1 0 0	4/31		1 0 1 0 0	20/31	
0 0 1 0 1	5/31		1 0 1 0 1	21/31	
0 0 1 1 0	6/31		1 0 1 1 0	22/31	
0 0 1 1 1	7/31	Palette A3/B3/C3	1 0 1 1 1	23/31	Palette A11/B11/C11
0 1 0 0 0	8/31		1 1 0 0 0	24/31	
0 1 0 0 1	9/31		1 1 0 0 1	25/31	
0 1 0 1 0	10/31		1 1 0 1 0	26/31	
0 1 0 1 1	11/31		1 1 0 1 1	27/31	
0 1 1 0 0	12/31		1 1 1 0 0	28/31	
0 1 1 0 1	13/31		1 1 1 0 1	29/31	
0 1 1 1 0	14/31		1 1 1 1 0	30/31	
0 1 1 1 1	15/31	Palette A7/B7/C7	1 1 1 1 1	31/31	Palette A15/B15/C15

NOTE1) "MON=0", "PWM=0", "C256=1"

NOTE2) Applied to palette Cj (j=0 to 15)

NOTE3) Palette 0, 1, 2, 4, 5, 6, 8, 9, 10, 12, 13 and 14 are disabled.

(6-3) Grayscale Selection in Fixed 8-grayscale Mode

Table 14-1 Grayscale Selection

(Palette Aj and Bj)

Display Data MSB- - - -LSB	Grayscale
0 0 0 *	0/7
0 0 1 *	1/7
0 1 0 *	2/7
0 1 1 *	3/7
1 0 0 *	4/7
1 0 1 *	5/7
1 1 0 *	6/7
1 1 1 *	7/7

Table 14-2 Grayscale Palette

(Palette Cj)

Display Data MSB- - - -LSB	Grayscale
0 0 **	0/7
0 1 **	3/7
1 0 **	5/7
1 1 **	7/7

NOTE1) "MON=0", "PWM=1", "C256=0 or 1"

(6-4) Grayscale Selection in B&W Mode

Table 15 Grayscale Selection

Display Data MSB- - - -LSB	Grayscale
0 ***	0
1 ***	1

NOTE1) "MON=1", "PWM=0 or 1" and "C256=0 or 1"

(7) DISPLAY TIMING GENERATOR

The display timing generator generates timing clocks such as the CL (Line Clock), FR (Frame Rate) and FLM (First Line Maker) by dividing an oscillation frequency. These clocks are used inside the LSI, and are activated by setting “1” at the D₀ (SON) bit of the “Duty-1 /Display Clock ON/OFF” instruction.

The CL is used for the line counter and the data latch circuit. At the rising edge of the CL signal, the line counter is counted up, then 384-bit display data is latched into the data latch circuit. At the falling edge of the CL signal, the latch data is released to the grayscale control circuit, then segment drivers Ai, Bi and Ci (i=0 to 127) produce LCD driving waveforms. The internal data-transmission timing between the DDRAM and segment drivers is completely independent from external data-transmission timing, so that MPU makes access to the LSI without concern for the LSI's internal operation.

The FR and FLM are generated by the CL. The FR toggles once every frame in the default status, and is programmed to toggle once every N lines. And the FLM is used to specify an initial display line, which is preset whenever the FLM becomes “H”.

(8) DATA LATCH CIRCUIT

The data latch circuit is used to temporarily store display data which is released to the grayscale control circuit. The display data in this circuit is updated in synchronization with the CL. The “All Pixels ON/OFF”, “Display ON/OFF” and “Reverse Display ON/OFF” instructions control the data in this circuit, but does not change the data in the DDRAM.

(9) COMMON DRIVERS AND SEGMENT DRIVERS

The LSI includes 128-common drivers, 384-segment drivers and 6-icon segment drivers. The common drivers generate LCD driving waveforms formed on the V_{LCD}, V₁, V₄ and V_{SSH} levels. The segment drivers generate waveforms formed on the V_{LCD}, V₂, V₃ and V_{SSH} levels.

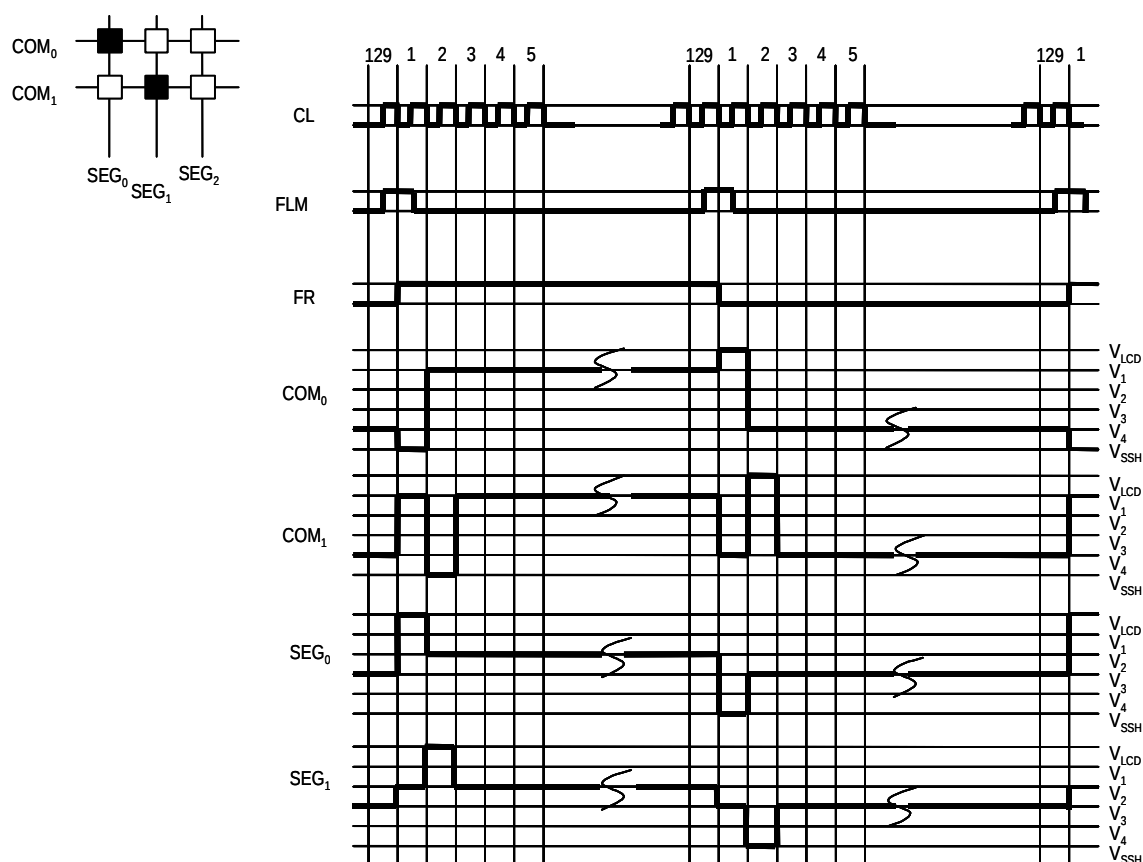


Fig 9 LCD Driving Waveforms (B&W Mode, Color Reverse OFF, 1/129 Duty)

(10) ICON SEGMENT

(10-1) Icon Segment Driver

The IC incorporates 6 icon segment drivers, such as the SEGSA₀, SEGSB₀, SEGSC₀, SEGSA₁, SEGSB₁ and SEGSC₁, and 2 icon segment registers. These drivers are used for the icon display in the periphery of an LCD screen. The palettes Aj, Bj and Cj (j=0-15) are applied to the SEGSA₀/SEGSA₁, SEGSB₀/SEGSB₁ and SEGSC₀/SEGSC₁ respectively, and each register has 12 bits to individually control the grayscale of 1 RGB-group (SEGSA₀, SEGSB₀, SEGSC₀ or SEGSA₁, SEGSB₁, SEGSC₁). This function is enabled by setting “1” at the D₁ (ICON) bit of the “Upper/Lower Palette Select and Icon Segment Access ON/OFF” instruction, and then either address (00H) or (01H) is specified by the “Window Start Column Address” instruction.

The D₁ (ALLON) bit of the “Display Control (1)” and the D₃ (REV) bit of the “Display Control (2)” instruction are effective in this function, and the D₀ (LREV) bit of the “Line Reverse ON/OFF” is ineffective.

Column Address (00H) : SEGSA₀, SEGSB₀, SEGSC₀

Column Address (01H) : SEGSA₁, SEGSB₁, SEGSC₁

Table 16 Selection of DDRAM Access or Icon Segment Register Access

RS	ICON	68-series	80-series		Function
		R/W	RDb	WRb	
L	0	H	L	H	Read Data (DDRAM)
L	0	L	H	L	Write Data (DDRAM)
L	1	H	L	H	Read Data (Icon Segment Register)
L	1	L	H	L	Write Data (Icon Segment Register)

NOTE1) Right after setting an address or right after writing data, a dummy read is necessary for accessing the icon segment registers as well as the DDRAM. The dummy data is read out by the 1st read instruction, and then correct data is read out from the specified address by the 2nd instruction.

NOTE2) The icon segment registers and the DDRAM use the same address counter. For this reason, whenever changing the “ICON” bit, the column address should be reset by the “Window Start Column Address” instruction.

NOTE3) The “HV” bit of the “Increment/Decrement Control” instruction should be “0” while accessing the icon segment register.

(10-2) Bit Assignment of Icon Segment Register Data

(10-2-1) Bit Assignment Overview

These maps is used for grasping general outlines of the variations in the bit assignment of the icon segment register data.

Table 17-1 ICON SEGMENT REGISTER MAP 1 (Variable 16-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	SEGS ₀				SEGS ₁																																				
	C256				Palette A				Palette B				Palette C				Palette A				Palette B				Palette C																
					A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀													
					X=00H																X=01H																				
WLS	1	0	0	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁								
				X=00H																X=01H																					
ABS	1	1	0	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁			
				X=00H (Upper)				X=00H (Lower)				X=01H (Upper)				X=01H (Lower)				X=01H (Upper)				X=01H (Lower)				X=01H (Upper)				X=01H (Lower)									
16bit	0	0	0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
				X=00H (Upper)				X=00H (Lower)				X=01H (Upper)				X=01H (Lower)				X=01H (Upper)				X=01H (Lower)				X=01H (Upper)				X=01H (Lower)									
8bit	0	1	0	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
				X=00H (Upper)				X=00H (Lower)				X=01H (Upper)				X=01H (Lower)				X=01H (Upper)				X=01H (Lower)				X=01H (Upper)				X=01H (Lower)									

Table 17-2 ICON SEGMENT REGISTER MAP 2 (Variable 8-grayscale Mode, Fixed 8-grayscale Mode or B&W Mode)

Mode	C256	ABS	WLS	SEGS ₀												SEGS ₁											
				Palette A						Palette B						Palette A						Palette B					
				A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀
8bit	0	X	1	X=00H						X=00H						X=01H						X=01H					
				-	-	-	-	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	-	-	-	-	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

Table 17-3 SWAP

SWAP	Palette A				Palette B				Palette C			
	A ₃	A ₂	A ₁	A ₀	B ₃	B ₂	B ₁	B ₀	C ₃	C ₂	C ₁	C ₀
0	SEGSax				SEGSbx				SEGSx			
1	SEGSx				SEGSbx				SEGSax			

NOTE1) On the register MAP 2, A₀, B₀, C₁ and C₀ bits are fixed to "1".
NOTE2) The functions of the variable 8-grayscale mode are different from those of the fixed 8-grayscale mode.
NOTE3) The contents of the icon segment register at "C256=0" are not compatible with the contents at "C256=1".
NOTE4) "C256=1" can be used in the 8-bit bus length mode, but not in the 16-bit bus length mode.
NOTE5) In the 8-bit bus length mode at "C256=0", odd accesses are prohibited because the data for 1 pixel is completed in successive two accesses.
NOTE6) In the 8-bit bus length mode at "C256=0", write upper bits first, then lower bits. This order is always adopted regardless of the "HV", "XD" and "YD" bits.

(10-2-2) Bit Assignment in Variable 16-grayscale Mode (Icon Segment Register)

16-bit Bus Length (MON=0, PWM=0, C256=0, WLS=1)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
0	0	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
0	1	X=00H													X=01H											
Register Data		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
Grayscale Palette		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
Icon Segment Driver		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	0	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	1	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

8-bit Bus Length (MON=0, PWM=0, C256=0, WLS=0)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																														
0	0	X=00H(Upper)					X=00H(Lower)						X=01H(Upper)					X=01H(Lower)														
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
		Palette A					Palette B					Palette C						Palette A					Palette B					Palette C				
		SEGSA ₀					SEGSB ₀					SEGSC ₀						SEGSA ₁					SEGSB ₁					SEGSC ₁				

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																															
0	1	X=00H(Upper)					X=00H(Lower)						X=01H(Upper)					X=01H(Lower)															
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁			D ₇	D ₆	D ₅	D ₄	D ₂	D ₁	D ₀	D ₇	D ₄	D ₃	D ₂	D ₁						
		Palette A					Palette B					Palette C							Palette A					Palette B					Palette C				
		SEGSA ₀					SEGSB ₀					SEGSC ₀							SEGSA ₁					SEGSB ₁					SEGSC ₁				

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	0	X=00H (Upper)				X=00H(Lower)									X=01H (Upper)				X=01H(Lower)							
Register Data Grayscale Palette Icon Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	1	X=00H (Upper)				X=00H(Lower)									X=01H (Upper)				X=01H(Lower)							
Register Data Grayscale Palette Icon Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

(10-2-3) Bit Assignment in variable 8-grayscale Mode (Icon Segment Register)

8-bit Bus Length (MON=0, PWM=0, C256=1, WLS=0)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																	
*	0	X=00H									X=01H								
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
		Palette A			Palette B			Palette C				Palette A			Palette B			Palette C	
		SEGSA ₀			SEGSB ₀			SEGSC ₀				SEGSA ₁			SEGSB ₁			SEGSC ₁	

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																	
*	1	X=00H									X=01H								
Register Data		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Grayscale Palette		Palette A			Palette B			Palette C				Palette A			Palette B			Palette C	
Icon Segment Driver		SEGSA ₀			SEGSB ₀			SEGSC ₀				SEGSA ₁			SEGSB ₁			SEGSC ₁	

(10-2-4) Bit Assignment in Fixed 8-grayscale Mode (Icon Segment Register)

16-bit Bus Length (MON=0, PWM=1, C256=0, WLS=1)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
0	0	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
0	1	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

NOTE) The data indicated with a slash mark (/) are invalid.

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	0	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	1	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=0, WLS=0)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver															
0	0	X=00H(Upper)								X=01H(Upper)							
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C							
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver															
0	1	X=00H(Upper)								X=01H(Upper)							
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C							
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			

NOTE) The data indicated with a slash mark (/) is invalid.

ABS	SWAP	Column Address / Register Data / Icon Segment Driver															
1	0	X=00H(Upper)				X=00H(Lower)								X=01H(Upper)			
Register Data Grayscale Palette Icon Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				Palette A			
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver															
1	1	X=00H(Upper)				X=00H(Lower)								X=01H(Upper)			
Register Data Grayscale Palette Icon Segment Driver		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				Palette A			
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			

NOTE) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length (MON=0, PWM=1, C256=1, WLS=0)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver															
*	0	X=00H								X=01H							
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				Palette A			
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver															
*	1	X=00H								X=01H							
Register Data Grayscale Palette Icon Segment Driver		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C				Palette A			
		SEGS _{A0}				SEGS _{B0}				SEGS _{C0}				SEGS _{A1}			

(10-2-5) Bit Assignment in B&W Mode (Icon Segment Register)

16-bit Bus Length (MON=1, PWM=*, C256=0, WLS=1)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
0	0	X=00H											X=01H													
Register Data Grayscale Palette Icon Segment Driver		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
0	1	X=00H											X=01H													
Register Data	Grayscale Palette Icon Segment Driver	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁		D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₀	D ₉	D ₈	D ₇	D ₄	D ₃	D ₂	D ₁
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	0	X=00H													X=01H											
Register Data		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
	Grayscale Palette	Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
	Icon Segment Driver	SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

ABS	SWAP	Column Address / Register Data / Icon Segment Driver																								
1	1	X=00H													X=01H											
Register Data Grayscale Palette Icon Segment Driver		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₁₁	D ₁₀	D ₉	D ₈	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
		Palette A				Palette B				Palette C					Palette A				Palette B				Palette C			
		SEGSA ₀				SEGSB ₀				SEGSC ₀					SEGSA ₁				SEGSB ₁				SEGSC ₁			

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=0, WLS=0)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver											
0	0	X=00H(Upper)				X=00H(Lower)				X=01H(Upper)			
Register Data		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₇	D ₆	D ₅
Grayscale Palette		Palette A				Palette B					Palette C		
Icon Segment Driver		SEGS _{A0}				SEGS _{B0}					SEGS _{C0}		

ABS	SWAP	Column Address / Register Data / Icon Segment Driver											
0	1	X=00H(Upper)				X=00H(Lower)				X=01H(Upper)			
Register Data		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₇	D ₆	D ₅
Grayscale Palette		Palette A				Palette B					Palette C		
Icon Segment Driver		SEGS _{A0}				SEGS _{B0}					SEGS _{C0}		

ABS	SWAP	Column Address / Register Data / Icon Segment Driver											
1	0	X=00H(Upper)				X=00H(Lower)				X=01H(Upper)			
Register Data		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄		D ₃	D ₂	D ₁
Grayscale Palette		Palette A				Palette B					Palette C		
Icon Segment Driver		SEGS _{A0}				SEGS _{B0}					SEGS _{C0}		

ABS	SWAP	Column Address / Register Data / Icon Segment Driver											
1	1	X=00H(Upper)				X=00H(Lower)				X=01H(Upper)			
Register Data		D ₃	D ₂	D ₁	D ₀	D ₇	D ₆	D ₅	D ₄		D ₃	D ₂	D ₁
Grayscale Palette		Palette A				Palette B					Palette C		
Icon Segment Driver		SEGS _{A0}				SEGS _{B0}					SEGS _{C0}		

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

8-bit Bus Length (MON=1, PWM=*, C256=1, WLS=0)

ABS	SWAP	Column Address / Register Data / Icon Segment Driver											
*	0	X=00H						X=01H					
Register Data		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₇	D ₆	D ₅
Grayscale Palette		Palette A				Palette B					Palette C		
Icon Segment Driver		SEGS _{A0}				SEGS _{B0}					SEGS _{C0}		

ABS	SWAP	Column Address / Register Data / Icon Segment Driver											
*	1	X=00H						X=01H					
Register Data		D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		D ₇	D ₆	D ₅
Grayscale Palette		Palette A				Palette B					Palette C		
Icon Segment Driver		SEGS _{A0}				SEGS _{B0}					SEGS _{C0}		

NOTE) The data indicated with a slash mark (/) is invalid, and only MSB bits are effective.

(11) OSCILLATOR

The oscillator is equipped with a resistor and a capacitor, and generates internal clocks used for the display timing generator and the voltage booster. The internal resistor is enabled by setting “0” at the D₁ (CKS) bit of the “Bus Length” instruction. For more accurate frequency, using an external resistor or external clock is recommended.

When using the internal resistor, the resistance is controlled to optimize frame frequency for different LCD panels, by setting the D₂-D₀ (RF2-RF0) bits of the “Frequency Control” instruction. For more safety, make sure what is the best frequency in the particular application.

(11-1) Using Internal Resistor (CKS=0)

In this case, the OSC1 should be fixed at “H” or “L” and the OSC2 is open. The oscillation frequency is varied according to the display mode, as follows.

Table 18 Oscillation Frequency vs. Display Mode

Symbol	MON	PWM	Display Mode
f _{OSC1}	0	0	Variable 8-/16-grayscale Mode
f _{OSC2}	0	1	Fixed 8-grayscale Mode
f _{OSC3}	1	*	B&W Mode

*: Don't care

(11-2) Using External Resistor (CKS=1)

Be sure to connect the OSC1 and OSC2 with an external resistor. The frequency of the oscillator should be adjusted to the same value generated by the internal resistor.

(11-3) Using External Clock (CKS=1)

Input external clock to the OSC1 and leave the OSC2 open. The external clock with 50% duty is recommended. The frequency of the external clock should be the same value generated by the internal resistor.

(12) LCD POWER SUPPLY

The internal LCD power supply is organized into the voltage converter and the voltage booster. The voltage converter consists of the reference voltage generator, the voltage regulator with EVR and the LCD bias voltage generator. The configuration of the LCD power supply is arranged by setting the D₃ (AMPON) and D₁ (DCON) bits of the “Power Control” instruction. For this configuration, the internal LCD power supply can be partially used in combination with an external supply voltage, as shown in Table 19.

Table 19 Configuration of LCD Power Supply

DCON	AMPON	Voltage Booster	Voltage Converter	External Supply Voltage	NOTE
0	0	Inactive	Inactive	V _{OUT} , V _{LCD} , V ₁ , V ₂ , V ₃ , V ₄	1, 3, 4
0	1	Inactive	Active	V _{OUT}	2, 3, 4
1	1	Active	Active	—	-

NOTE1) No internal LCD power supply is used. The LCD bias voltages are externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋, V_{REF}, V_{REG} and V_{EE} are open.

NOTE2) Only the voltage converter is used. The V_{OUT} is externally supplied, and the C₁₊, C₁₋, C₂₊, C₂₋, C₃₊, C₃₋, C₄₊, C₄₋, C₅₊, C₅₋ and V_{EE} are open. The reference voltage is supplied on the V_{REF}.

NOTE3) The following relation among each LCD bias voltages must be maintained.

$$V_{OUT} \geq V_{LCD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_{SSH}$$

NOTE4) If the internal LCD power supply doesn't have enough capability to drive the particular LCD panel, use the external LCD power supply. Otherwise, it may affect display quality.

(12-1) Voltage Booster

The internal voltage booster generates up to $6 \times V_{EE}$ voltage. The boost level is selected from 2x, 3x, 4x, 5x or 6x by setting the D_2 - D_0 ($VU2$ - $VU0$) bits of the “Boost Level” instruction. The boost voltage V_{OUT} must not exceed 18.0V, otherwise the voltage stress may cause a permanent damage to the LSI.

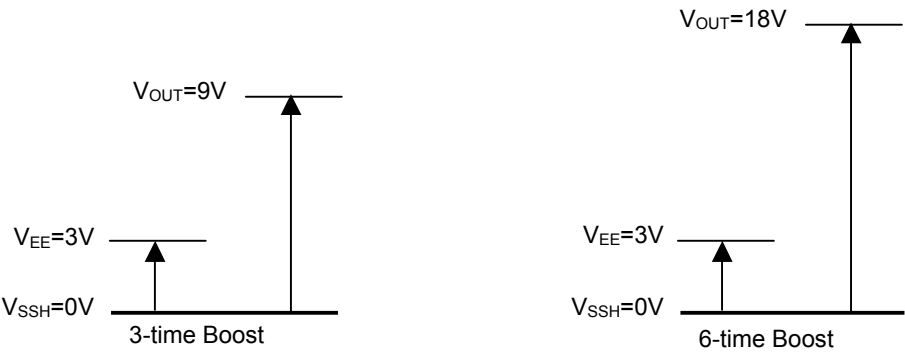


Fig 10 Boost Voltage

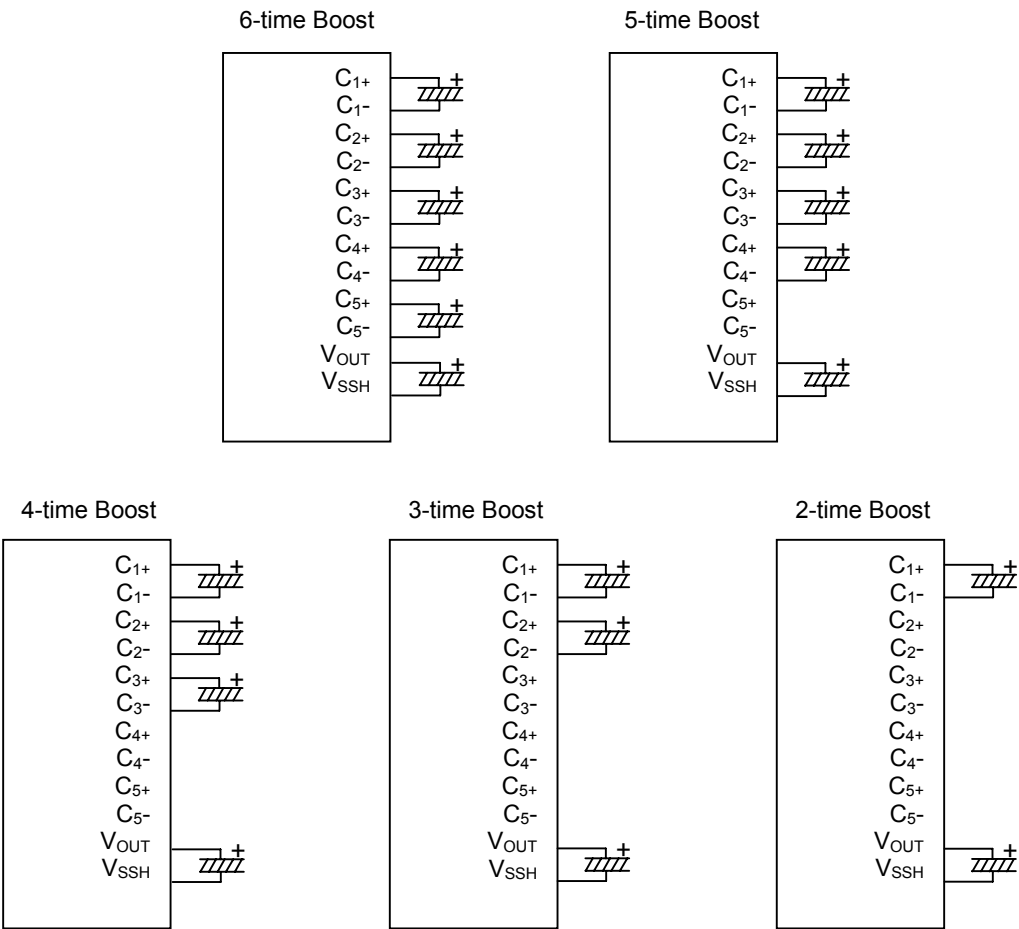


Fig 11 External Capacitor Connection of Voltage Booster

(12-2) Voltage Converter

(12-2-1) Reference Voltage Generator

The reference voltage generator produces the reference voltage ($V_{BA}=0.9 \times V_{EE}$). When using the internal LCD power supply, connect the V_{BA} and the V_{REF} , or supply $0.9 \times V_{EE}$ or lower voltage on the V_{REF} . When using an external LCD power supply, the V_{BA} should be open. Refer to Fig 12, 14 and 15.

(12-2-2) Voltage Regulator

The voltage regulator consists of an operational amplifier with gain control and EVR. The V_{REF} voltage is multiplied to obtain the V_{REG} voltage, and its multiple (boost level) is set by the D_2 - D_0 (VU2-VU0) bits of the “Boost Level” instruction. The formula is shown below.

$$V_{REG} = V_{REF} \times N \quad (N: \text{Boost Level})$$

(12-2-3) Electrical Variable Resistor (EVR)

The EVR is used to fine-tune the V_{LCD} voltage to optimize display contrast. The EVR value is controlled in 128 steps by setting the D_3 - D_0 (DV₆-DV₀) bits of the “EVR Control” instruction. The formula is shown below.

$$V_{LCD} = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127 \quad (M: \text{EVR Value})$$

(12-2-4) LCD Bias Voltage Generator

The LCD bias voltage generator consists of buffer amplifiers and bleeder resistors to generate the LCD bias voltages such as the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and its bias ratio is selected from 1/5, 1/6, 1/7, 1/8, 1/9, 1/10, 1/11 and 1/12.

As shown in Fig 12, when using only the internal LCD power supply, the capacitors CA2 are connected to the V_{LCD} , V_1 , V_2 , V_3 and V_4 respectively.

As shown in Fig 13, when using no internal LCD power supply, the LCD bias voltages are externally supplied on the V_{LCD} , V_1 , V_2 , V_3 and V_4 , and the internal LCD power supply should be turned off by setting “0” at the “DCON” and “AMPON” bits. And the C_{1+} , C_{1-} , C_{2+} , C_{2-} , C_{3+} , C_{3-} , C_{4+} , C_{4-} , C_{5+} , C_{5-} , V_{EE} , V_{REF} and V_{REG} are open.

Fig 14 and 15 show typical peripheral circuits when partially using the LCD power supply without the reference voltage generator.

Fig 16 shows the circuit when partially using the LCD power supply without the voltage booster.

(12-3) External Components for LCD Power Supply

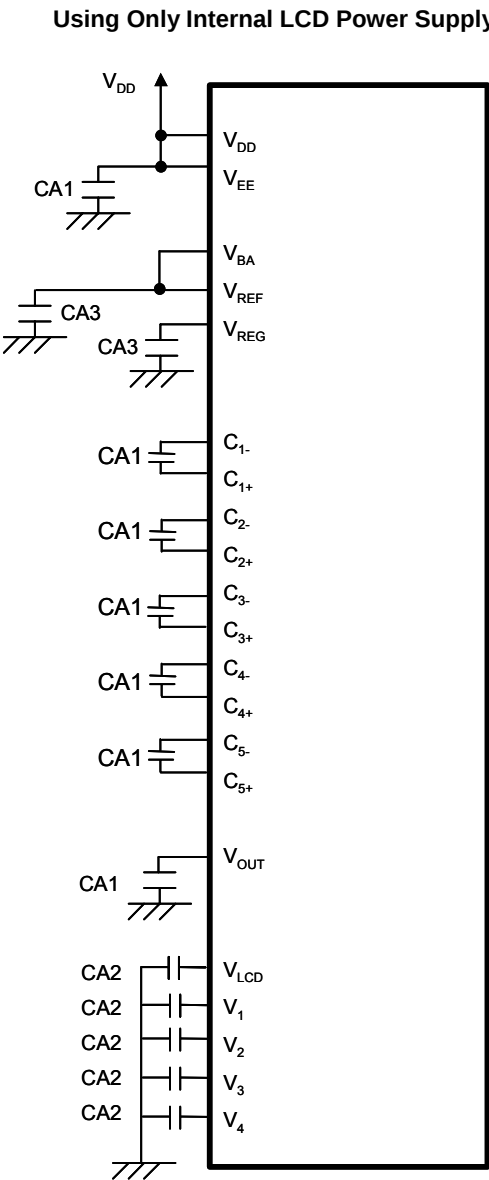


Fig 12

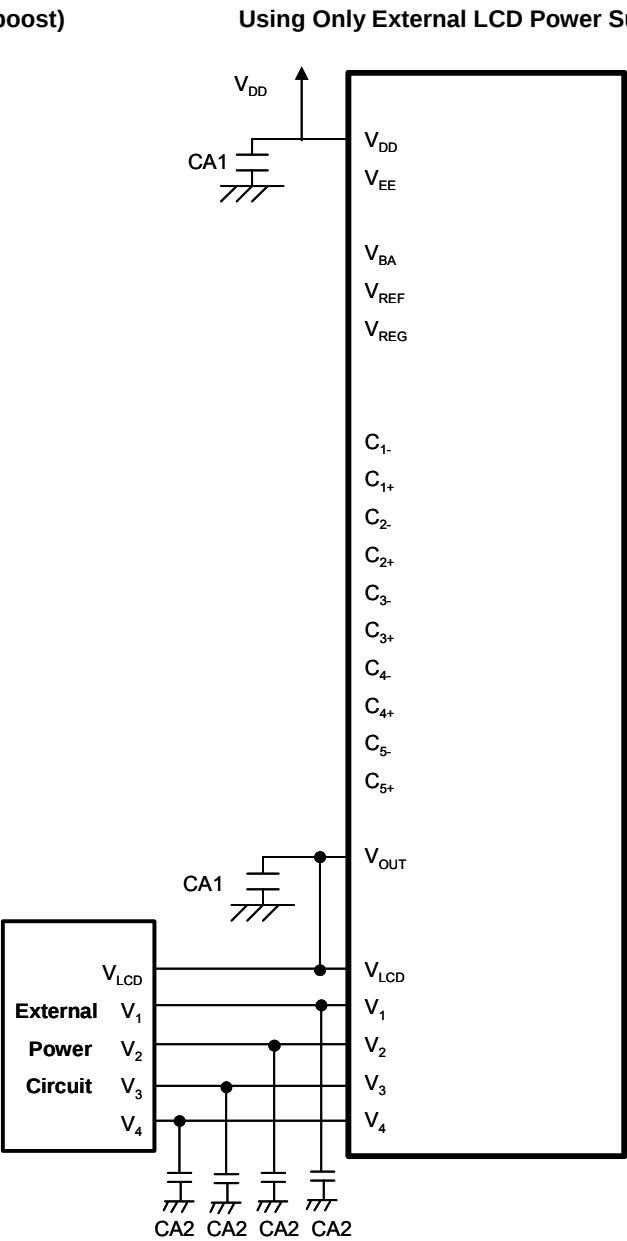


Fig 13

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply
Without Reference Voltage generator (1)
(6x boost)

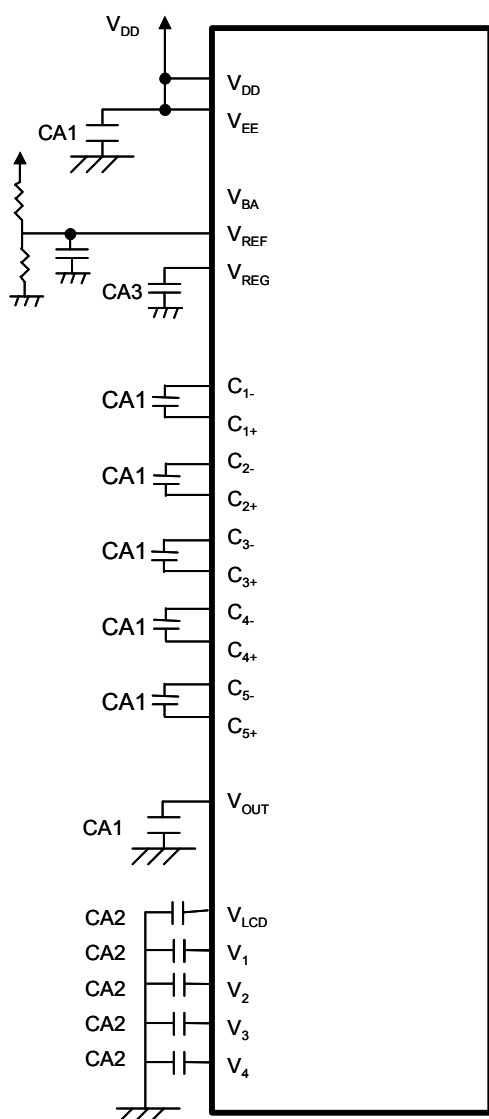


Fig 14

Using Internal LCD Power Supply
Without Reference Voltage generator (2)
(6x boost)

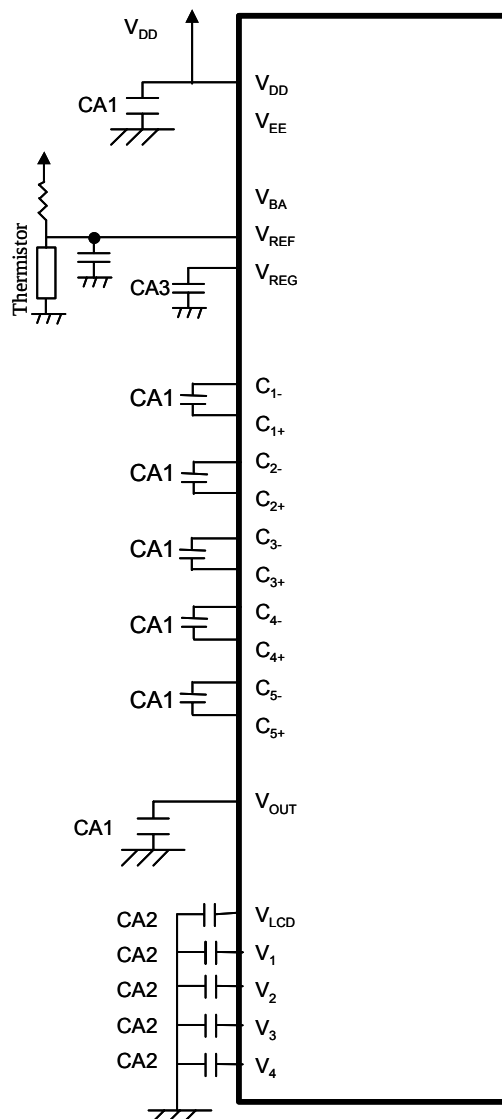


Fig 15

Reference Values

CA1	1.0 to 4.7 μ F
CA2	1.0 to 2.2 μ F
CA3	0.1 μ F

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (V_{DD} , V_{SS} , V_{EE} , V_{SSH} , V_{OUT} , V_{LCD} , V_1 , V_2 , V_3 and V_4) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

Using Internal LCD Power Supply
Without Voltage Booster

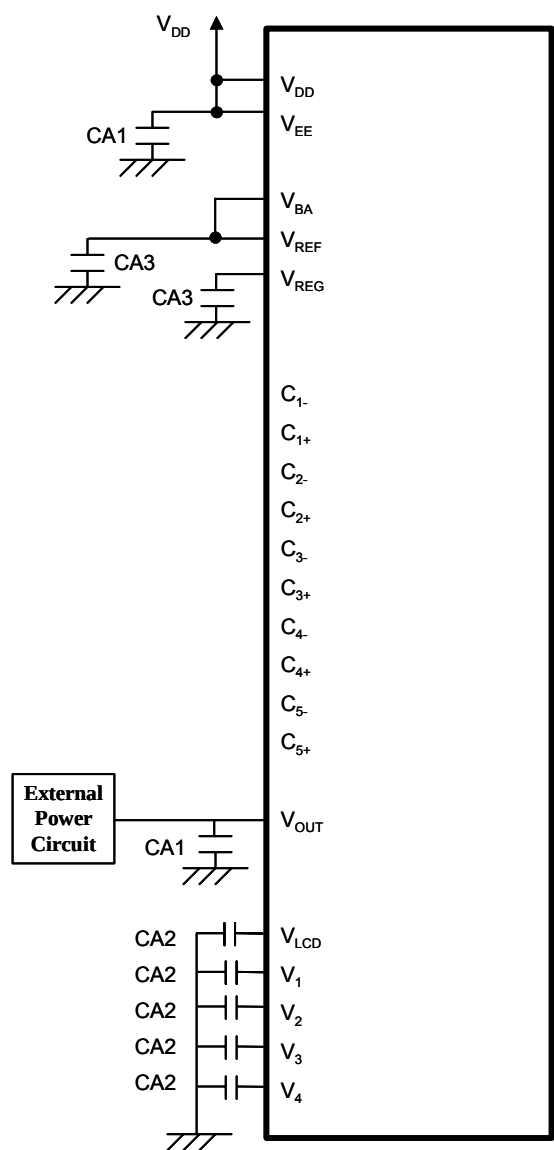


Fig 16

Reference Values

CA1	1.0 to 4.7μF
CA2	1.0 to 2.2μF
CA3	0.1μF

NOTE1) B grade capacitor is recommended for CA1-CA3. Make sure what is the best capacitor value in the particular application.

NOTE2) Parasitic resistance on the power supply lines (**V_{DD}**, **V_{SS}**, **V_{EE}**, **V_{SSH}**, **V_{OUT}**, **V_{LCD}**, **V₁**, **V₂**, **V₃** and **V₄**) reduces step-up efficiency of the voltage booster, and may have an impact on the LSI's operation and display quality. To minimize this impact, be sure to lay out the shortest wires and place capacitors as close to the LSI as possible.

(12-4) Discharge Circuit

The LSI incorporates two discharge circuits which are independently controlled for the V_{LCD} and V_1 - V_4 and for the V_{OUT} . The V_{LCD} and V_1 - V_4 are discharged by setting "1" at the D_0 (DIS) bit of the "Discharge ON/OFF" instruction or the reset by the RESb. And the V_{OUT} (100K Ω internal resistor between V_{OUT} and V_{EE}) is discharged by setting "1" at the D_1 (DIS2) bit of this instruction. Be sure to turned off the internal or external LCD power supply when this instruction is executed, otherwise it may function as a current load and affect an operating current. Refer to "(15-22) Discharge ON/OFF".

(12-5) Power ON/OFF

To protect the LSI from overcurrent, the following sequences must be maintained to turn on and off the power supply. In addition to the following discussions, refer to "(19) TYPICAL INSTRUCTION SEQUENCES".

(12-5-1) Power ON/OFF in Using Internal LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "Internal LCD power supply ON". Be sure to execute the "Display ON" instruction later than the completion of this power ON sequence. Otherwise, unexpected pixels may be turned on instantly.

Power OFF

First "Reset by RESb or "HALT" instruction", next " V_{DD} and V_{EE} OFF". If using different power sources for the V_{DD} and the V_{EE} individually, the V_{EE} must be turned off after the reset or the "HALT". After that, the V_{DD} can be turned off, waiting until the LCD bias voltages (V_{LCD} , V_1 , V_2 , V_3 and V_4) drop below the threshold level of LCD pixels.

(12-5-2) Power ON/OFF in Using External LCD Power Supply

Power ON

First " V_{DD} and V_{EE} ON", next "Reset by RESb", then "External LCD power supply ON". When using only external V_{OUT} , first " V_{DD} ON", next "Reset by RESb", then "External V_{OUT} ON", as well.

Power OFF

First "Reset by RESb or "HALT" instruction" to isolate external LCD bias voltages, next " V_{DD} OFF". For more safety, placing a resistor in series on the V_{LCD} line (or the V_{OUT} line in using only the external V_{OUT}) is recommended. That resistance is usually between 50 Ω and 100 Ω .

(12-6) LCD Bias Adjustment Circuit

The LCD bias voltages V_1 and V_4 can be fine-tuned for different LCD panels by setting the V_1A_1 & V_1A_2 and V_4A_1 & V_4A_2 terminals, as follows.

Table 20-1 LCD Bias Adjustment (V_1A_1 , V_1A_2)

V_1A_1	V_1A_2	Voltage Variation [mV] (NOTE1)
L	L	0
L	H	+5
H	L	-5
H	H	+10

Table 20-2 LCD Bias Adjustment (V_4A_1 , V_4A_2)

V_4A_1	V_4A_2	Voltage Variation [mV] (NOTE1)
L	L	0
L	H	+5
H	L	-5
H	H	+10

NOTE1) The variation is defined as the voltage shifted from 0mV at (V_1A_1 , V_1A_2)=(0,0) and (V_4A_1 , V_4A_2)=(0,0). And "+" means shifting toward the V_{LCD} , and "-" means shifting toward the V_{SS} .

NOTE2) The voltage variations as mentioned above are theoretical values, and therefore may have a certain amount of error.

NOTE3) The voltage variations as mentioned above are the theoretical values at V_{LCD} =13.5V.

(13) RESET FUNCTION

The reset function initializes the LSI to the following default status by setting the RESb to “L”. Connecting the RESb with MPU’s reset is recommended so that the LSI and MPU is initialized at a time.

Default Status

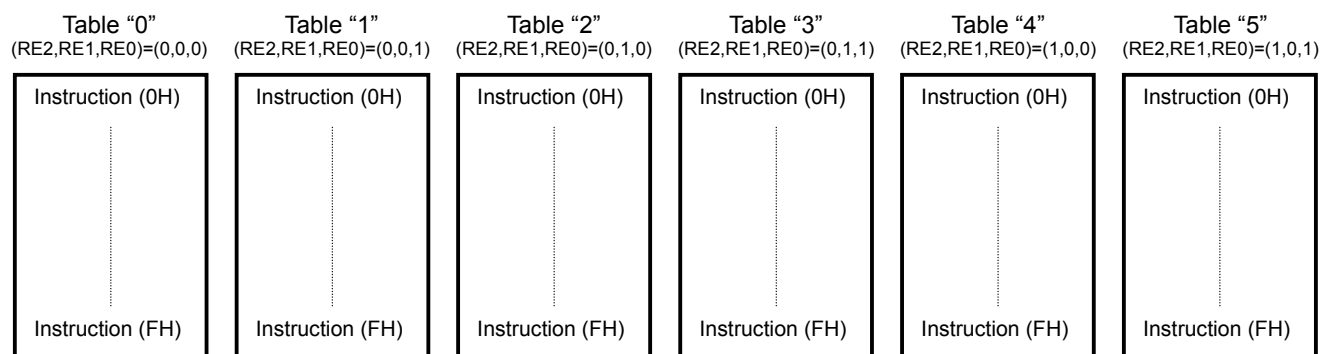
1. Display Data in DDRAM	:Undefined
2. Window Start Column Address	:(00)H
3. Window Start Row Address	:(00)H
4. Initial Display Line	:(0)H (1st line)
5. Display ON/OFF	:OFF
6. Reverse Display ON/OFF	:OFF (Normal)
7. Duty Cycle Ratio	:1/129 Duty (DSE=0)
8. N-line Inversion ON/OFF	:OFF
9. COM Scan Direction	:COM ₀ → COM ₁₂₇
10. Increment/Decrement Control	:(HV, XD, YD)=(0, 0, 0)
11. Read-modify-write	:OFF (AIM=0)
12. Swap	:OFF (Normal)
13. EVR Value	:(0, 0, 0, 0, 0, 0, 0)
14. Internal LCD Power Supply	:OFF
15. Display Mode	:Grayscale Mode
16. LCD Bias Ratio	:1/9 Bias
17. Palette 0	:(0, 0, 0, 0, 0)
18. Palette 1	:(0, 0, 0, 1, 1)
19. Palette 2	:(0, 0, 1, 0, 1)
20. Palette 3	:(0, 0, 1, 1, 1)
21. Palette 4	:(0, 1, 0, 0, 1)
22. Palette 5	:(0, 1, 0, 1, 1)
23. Palette 6	:(0, 1, 1, 0, 1)
24. Palette 7	:(0, 1, 1, 1, 1)
25. Palette 8	:(1, 0, 0, 0, 1)
26. Palette 9	:(1, 0, 0, 1, 1)
27. Palette 10	:(1, 0, 1, 0, 1)
28. Palette 11	:(1, 0, 1, 1, 1)
29. Palette 12	:(1, 1, 0, 0, 1)
30. Palette 13	:(1, 1, 0, 1, 1)
31. Palette 14	:(1, 1, 1, 0, 1)
32. Palette 15	:(1, 1, 1, 1, 1)
33. Display Mode Control	:Variable 16-grayscale Mode (4,096 Colors)
34. Bus Length	:8-bit Bus Length
35. Discharge ON/OFF	:OFF (DIS,DIS2)=(0,0)

(14) INSTRUCTION TABLES

(14-1) Instruction Table and Register Address

The LSI incorporates 6 instruction tables as shown in Fig 17, and each instruction table has a specific address in between “0” and “5”. And each instruction register has a specific address in between (0H) and (FH), and instruction is read out from the register by the “Register Address” and “Register Read” instructions.

Fig 18 shows part of the instruction sequence, where the instruction table should be specified prior to other instructions. However, when some instructions of the same table are sequentially executed, the table selection may be omitted. In addition, the “Display Data Write”, “Display Data Read” and “Register Read” instructions can be performed in any table.



NOTE) Address (FH) is assigned to “Instruction Table Select” in any table.

Fig 17 Instruction Table Overview

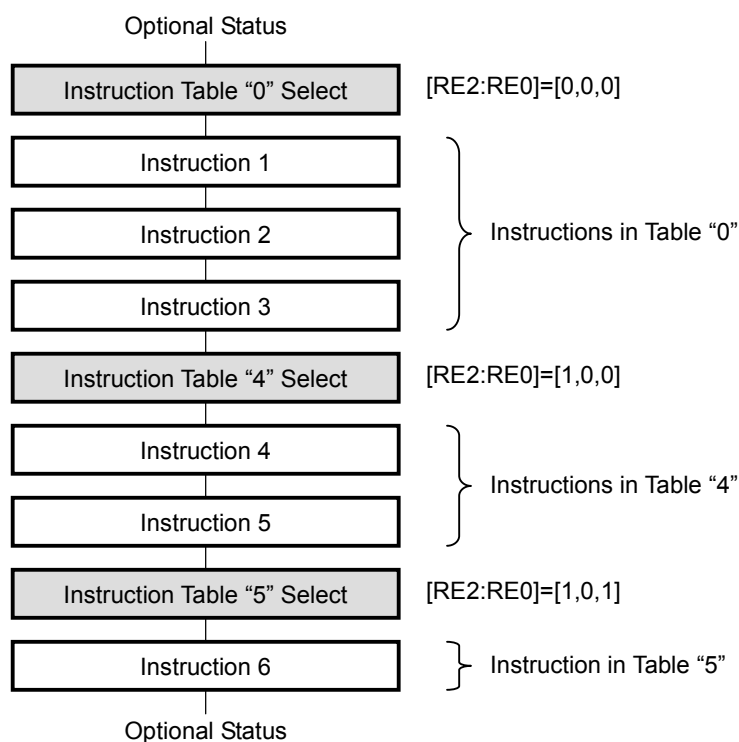


Fig 18 Outline of Instruction Sequence

(14-2) Instruction Table 0 (RE2, RE1, RE0)=(0, 0, 0)

Instructions/ Register Address [NH]		Code (80 Series MPU I/F)							Code								Functions	
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
1	Display Data Write	0	0	1	0	0/1	0/1	0/1	Write Data								Writing Display Data	
2	Display Data Read	0	0	0	1	0/1	0/1	0/1	Read Data								Reading Display Data	
3	Window Start Column Address (Lower) [0H]	0	1	1	0	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Setting Column Address for start point	
	Window Start Column Address (Upper) [1H]	0	1	1	0	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	Setting Column Address for start point	
4	Window Start Row Address (Lower) [2H]	0	1	1	0	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Setting Row Address for start point	
	Window Start Row Address (Upper) [3H]	0	1	1	0	0	0	0	0	0	1	1	*	AY6	AY5	AY4	Setting Row Address for start point	
5	Initial Display Line (Lower) [4H]	0	1	1	0	0	0	0	0	1	0	0	LA3	LA2	LA1	LA0	Setting Row Address for Initial COM	
	Initial Display Line (Upper) [5H]	0	1	1	0	0	0	0	0	1	0	1	*	LA6	LA5	LA4	Setting Row Address for Initial COM	
6	N-line Inversion (Lower) [6H]	0	1	1	0	0	0	0	0	1	1	0	N3	N2	N1	N0	Setting the Number of N-line Inversion	
	N-line Inversion (Upper) [7H]	0	1	1	0	0	0	0	0	1	1	1	*	N6	N5	N4	Setting the Number of N-line Inversion	
7	Display Control (1) [8H]	0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON/OFF	SHIFT : Common Scan Direction MON : Grayscale/B/W Mode ALLON : All Pixels ON/OFF ON/OFF : Display ON/OFF	
8	Display Control (2) [9H]	0	1	1	0	0	0	0	1	0	0	1	REV	NLIN	SWAP	*	REV : Reverse Display ON/OFF NLIN : N-line Inversion ON/OFF SWAP : SWAP ON/OFF	
9	Increment/Decrement Control [AH]	0	1	1	0	0	0	0	1	0	1	0	AIM	HV	XD	YD	AIM : Read-Modify-Write ON/OFF HV :Horizontal/ Vertical Direction XD : X Increment / Decrement YD : Y Increment / Decrement	
10	Power Control [BH]	0	1	1	0	0	0	0	1	0	1	1	AMP ON	HALT	DC ON	ACL	AMPON : Voltage Converter ON/OFF HALT : Power Save ON/OFF DCON : Voltage Booster ON/OFF ACL : Reset	
11	Duty Cycle Ratio [CH]	0	1	1	0	0	0	0	1	1	0	0	DS3	DS2	DS1	DS0	Setting LCD Duty Cycle Ratio	
12	Boost Level [DH]	0	1	1	0	0	0	0	1	1	0	1	*	VU2	VU1	VU0	Setting Boost Level	
13	LCD Bias Ratio [EH]	0	1	1	0	0	0	0	1	1	1	0	*	B2	B1	B0	Setting LCD Bias Ratio	
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table	

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14-3) Instruction Table 1 (RE2, RE1, RE0)=(0, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
15	Palette A0/A8 (Lower) [0H]	0	1	1	0	0	0	1	0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A0/A8 (Upper) [1H]	0	1	1	0	0	0	1	0	0	0	1	*	*	*	PA04/ PA84	Setting Palette Data : A0(PS=0) /A8(PS=1)
	Palette A1/A9 (Lower) [2H]	0	1	1	0	0	0	1	0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A1/A9 (Upper) [3H]	0	1	1	0	0	0	1	0	0	1	1	*	*	*	PA14/ PA94	Setting Palette Data : A1(PS=0) /A9(PS=1)
	Palette A2/A10 (Lower) [4H]	0	1	1	0	0	0	1	0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A2/A10 (Upper) [5H]	0	1	1	0	0	0	1	0	1	0	1	*	*	*	PA24/ PA104	Setting Palette Data : A2(PS=0) /A10(PS=1)
	Palette A3/A11 (Lower) [6H]	0	1	1	0	0	0	1	0	1	1	0	PA33/ PA113	PA32/P A112	PA31/ PA111	PA30/ PA110	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A3/A11 (Upper) [7H]	0	1	1	0	0	0	1	0	1	1	1	*	*	*	PA34/ PA114	Setting Palette Data : A3(PS=0) /A11(PS=1)
	Palette A4/A12 (Lower) [8H]	0	1	1	0	0	0	1	1	0	0	0	PA43/ PA123	PA42/P A122	PA41/ PA121	PA40/ PA120	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A4/A12 (Upper) [9H]	0	1	1	0	0	0	1	1	0	0	1	*	*	*	PA44/ PA124	Setting Palette Data : A4(PS=0) /A12(PS=1)
	Palette A5/A13 (Lower) [AH]	0	1	1	0	0	0	1	1	0	1	0	PA53/ PA133	PA52/P A132	PA51/ PA131	PA50/ PA130	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A5/A13 (Upper) [BH]	0	1	1	0	0	0	1	1	0	1	1	*	*	*	PA54/ PA134	Setting Palette Data : A5(PS=0) /A13(PS=1)
	Palette A6/A14 (Lower) [CH]	0	1	1	0	0	0	1	1	1	0	0	PA63/ PA143	PA62/P A142	PA61/ PA141	PA60/ PA140	Setting Palette Data : A6(PS=0) /A14(PS=1)
	Palette A6/A14 (Upper) [DH]	0	1	1	0	0	0	1	1	1	0	1	*	*	*	PA64/ PA144	Setting Palette Data : A6(PS=0) /A14(PS=1)
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14-4) Instruction Table 2 (RE2, RE1, RE0)=(0, 1, 0)

Instructions/ Register Address [NH]	Code (80 series MPU I/F)							Code								Functions
	CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
Palette A7/A15 (Lower) [0H]	0	1	1	0	0	1	0	0	0	0	0	PA73/ PA153	PA72/P A152	PA71/ PA151	PA70/ PA150	Setting Palette Data : A7(PS=0) /A15(PS=1)
Palette A7/A15 (Upper) [1H]	0	1	1	0	0	1	0	0	0	0	1	*	*	*	PA74/ PA154	Setting Palette Data : A7(PS=0) /A15(PS=1)
Palette B0/B8 (Lower) [2H]	0	1	1	0	0	1	0	0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80	Setting Palette Data : B0(PS=0) /B8(PS=1)
Palette B0/B8 (Upper) [3H]	0	1	1	0	0	1	0	0	0	1	1	*	*	*	PB04/ PB84	Setting Palette Data : B0(PS=0) /B8(PS=1)
Palette B1/B9 (Lower) [4H]	0	1	1	0	0	1	0	0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90	Setting Palette Data : B1(PS=0) /B9(PS=1)
Palette B1/B9 (Upper) [5H]	0	1	1	0	0	1	0	0	1	0	1	*	*	*	PB14/ PB94	Setting Palette Data : B1(PS=0) /B9(PS=1)
Palette B2/B10 (Lower) [6H]	0	1	1	0	0	1	0	0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100	Setting Palette Data : B2(PS=0) /B10(PS=1)
Palette B2/B10 (Upper) [7H]	0	1	1	0	0	1	0	0	1	1	1	*	*	*	PB24/ PB104	Setting Palette Data : B2(PS=0) /B10(PS=1)
Palette B3/B11 (Lower) [8H]	0	1	1	0	0	1	0	1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110	Setting Palette Data : B3(PS=0) /B11(PS=1)
Palette B3/B11 (Upper) [9H]	0	1	1	0	0	1	0	1	0	0	1	*	*	*	PB34/ PB114	Setting Palette Data : B3(PS=0) /B11(PS=1)
Palette B4/B12 (Lower) [AH]	0	1	1	0	0	1	0	1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120	Setting Palette Data : B4(PS=0) /B12(PS=1)
Palette B4/B12 (Upper) [BH]	0	1	1	0	0	1	0	1	0	1	1	*	*	*	PB44/ PB124	Setting Palette Data : B4(PS=0) /B12(PS=1)
Palette B5/B13 (Lower) [CH]	0	1	1	0	0	1	0	1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130	Setting Palette Data : B5(PS=0) /B13(PS=1)
Palette B5/B13 (Upper) [DH]	0	1	1	0	0	1	0	1	1	0	1	*	*	*	PB54/ PB134	Setting Palette Data : B5(PS=0) /B13(PS=1)
14 Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Tablet

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14-5) Instruction Table 3 (RE2, RE1, RE0)=(0, 1, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
15	Palette B6/B14 (Lower) [0H]	0	1	1	0	0	1	1	0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B6/B14 (Upper) [1H]	0	1	1	0	0	1	1	0	0	0	1	*	*	*	PB64/ PB144	Setting Palette Data : B6(PS=0) /B14(PS=1)
	Palette B7/B15 (Lower) [2H]	0	1	1	0	0	1	1	0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette B7/B15 (Upper) [3H]	0	1	1	0	0	1	1	0	0	1	1	*	*	*	PB74/ PB154	Setting Palette Data : B7(PS=0) /B15(PS=1)
	Palette C0/C8 (Lower) [4H]	0	1	1	0	0	1	1	0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C0/C8 (Upper) [5H]	0	1	1	0	0	1	1	0	1	0	1	*	*	*	PC04/ PC84	Setting Palette Data : C0(PS=0) /C8(PS=1)
	Palette C1/C9 (Lower) [6H]	0	1	1	0	0	1	1	0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C1/C9 (Upper) [7H]	0	1	1	0	0	1	1	0	1	1	1	*	*	*	PC14/ PC94	Setting Palette Data : C1(PS=0) /C9(PS=1)
	Palette C2/C10 (Lower) [8H]	0	1	1	0	0	1	1	1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C2/C10 (Upper) [9H]	0	1	1	0	0	1	1	1	0	0	1	*	*	*	PC24/ PC104	Setting Palette Data : C2(PS=0) /C10(PS=1)
	Palette C3/C11 (Lower) [AH]	0	1	1	0	0	1	1	1	0	1	0	PC33P C113	PC32/ PC112	PC31/ PC111	PC30/ PC110	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C3/C11 (Upper) [BH]	0	1	1	0	0	1	1	1	0	1	1	*	*	*	PC34/ PC114	Setting Palette Data : C3(PS=0) /C11(PS=1)
	Palette C4/C12 (Lower) [CH]	0	1	1	0	0	1	1	1	1	1	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120	Setting Palette Data : C4(PS=0) /C12(PS=1)
	Palette C4/C12 (Upper) [DH]	0	1	1	0	0	1	1	1	1	1	0	1	*	*	*	PC44/ PC124
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14-6) Instruction Table 4 (RE2, RE1, RE0)=(1, 0, 0)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
15	Palette C5/C13 (Lower) [0H]	0	1	1	0	1	0	0	0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C5/C13 (Upper) [1H]	0	1	1	0	1	0	0	0	0	0	1	*	*	*	PC54/ PC134	Setting Palette Data : C5(PS=0) /C13(PS=1)
	Palette C6/C14 (Lower) [2H]	0	1	1	0	1	0	0	0	0	1	0	PC63/P C143	PC62/ PC142	PC61/ PC141	PC60/ PC140	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C6/C14 (Upper) [3H]	0	1	1	0	1	0	0	0	0	1	1	*	*	*	PC64/ PC144	Setting Palette Data : C6(PS=0) /C14(PS=1)
	Palette C7/C15 (Lower) [4H]	0	1	1	0	1	0	0	0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150	Setting Palette Data : C7(PS=0) /C15(PS=1)
	Palette C7/C15 (Upper) [5H]	0	1	1	0	1	0	0	0	1	0	1	*	*	*	PC74/ PC154	Setting Palette Data : C7(PS=0) /C15(PS=1)
16	Initial COM [6H]	0	1	1	0	1	0	0	0	1	1	0	SC3	SC2	SC1	SC0	Setting start COM for scanning
17	Duty-1 /Display Clock ON/OFF [7H]	0	1	1	0	1	0	0	0	1	1	1	*	*	DSE	SON	SON : Display Clock ON/OFF DSE : Duty-1 ON/OFF
18	Display Mode Control /Boost Clock Control [8H]	0	1	1	0	1	0	0	1	0	0	0	PWM	C256	FDC1	FDC2	PWM : Variable/Fixed Grayscale C256 : 256-color Mode ON/OFF FDC1,2 : Boost Clock Control
19	Bus Length [9H]	0	1	1	0	1	0	0	1	0	0	1	*	ABS	CKS	WLS	ABS : Bit Assignment CKS : Oscillator Set WLS : 8-/16-bit Bus Length
20	EVR Control (Lower) [AH]	0	1	1	0	1	0	0	1	0	1	0	DV3	DV2	DV1	DV0	Setting EVR Value (Lower Bit)
	EVR Control (Upper) [BH]	0	1	1	0	1	0	0	1	0	1	1	*	DV6	DV5	DV4	Setting EVR Value (Upper Bit)
21	Frequency Control [DH]	0	1	1	0	1	0	0	1	1	0	1	*	RF2	RF1	RF0	Adjusting Oscillation Frequency
22	Discharge ON/OFF [EH]	0	1	1	0	1	0	0	1	1	1	0	*	*	DIS2	DIS	Discharge ON/OFF
23	Register Address [CH]	0	1	1	0	1	0	0	1	1	0	0	Register Address				Setting Register Address
24	Register Read	0	1	0	1	0/1	0/1	0/1	*	*	*	*	Read Data				Reading Instruction
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table Select

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(14-7) Instruction Table 5 (RE2, RE1, RE0)=(1, 0, 1)

Instructions/ Register Address [NH]		Code (80 series MPU I/F)							Code								Functions
		CSb	RS	RDb	WRb	RE2	RE1	RE0	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀	
25	Window End Column Address (Lower) [0H]	0	1	1	0	1	0	1	0	0	0	0	EX3	EX2	EX1	EX0	Setting Column Address for end point
	Window End Column Address (Upper) [1H]	0	1	1	0	1	0	1	0	0	0	1	EX7	EX6	EX5	EX4	Setting Column Address for end point
26	Window End Row Address (Lower) [2H]	0	1	1	0	1	0	1	0	0	1	0	EY3	EY2	EY1	EY0	Setting Row Address for end point
	Window End Row Address (Upper) [3H]	0	1	1	0	1	0	1	0	0	1	1	*	EY6	EY5	EY4	Setting Row Address for end point
27	Initial Line-reverse Address (Lower) [4H]	0	1	1	0	1	0	1	0	1	0	0	LS3	LS2	LS1	LS0	Setting Start Line for Line-reverse Display
	Initial Line-reverse Address (Upper) [5H]	0	1	1	0	1	0	1	0	1	0	1	*	LS6	LS5	LS4	Setting Start Line for Line-reverse Display
28	Last Line-reverse Address (Lower) [6H]	0	1	1	0	1	0	1	0	1	1	0	LE3	LE2	LE1	LE0	Setting End Line for Line-reverse Display
	Last Line-reverse Address (Upper) [7H]	0	1	1	0	1	0	1	0	1	1	1	*	LE6	LE5	LE4	Setting End Line for Line-reverse Display
29	Line Reverse ON/OFF [8H]	0	1	1	0	1	0	1	1	0	0	0	*	*	BT	LREV	BT : Blink Set LREV : Line-reverse ON/OFF
30	Upper/Lower Palette Select /Icon Segment Access ON/OFF [9H]	0	1	1	0	1	0	1	1	0	0	1	*	*	ICON	PS	PS : Upper/Lower Palette ICON : Icon Segment ON/OFF
31	PWM Control [AH]	0	1	1	0	1	0	1	1	0	1	0	PWMS	PWMA	PWMB	PWMC	Setting PWM Mode
14	Instruction Table Select [FH]	0	1	1	0	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	Setting Instruction Table

NOTE1) * : Don't care.

NOTE2) [NH] (N=0-F) : Register Address

NOTE3) Any nonexistent instruction code is prohibited.

NOTE4) Dual instructions except for "EVR Control" are already effective when either upper byte or lower byte is set.

NOTE5) "EVR Control" instruction is finally effective when both upper and lower bytes are set. Send upper byte first, next lower byte.

(15) INSTRUCTION DESCRIPTIONS

This chapter provides detailed descriptions about each instruction. These descriptions are written with the assumption that 80-series MPU is used. When using 68-series MPU, the polarities of the E and R/W signals differ from those of the RDb and WRb signals.

(15-1) Display Data Write

The “Display Data Write” instruction writes display data on a specified DDRAM address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(15-2) Display Data Read

The “Display Data Read” instruction reads out display data from a specified DDRAM address. One dummy read is necessary right after DDRAM address setting.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	0	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Display Data							

(15-3) Window Start Column Address

The “Window Start Column Address” instruction specifies the column address of the start point. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	AX3	AX2	AX1	AX0

(Default: AX3-AX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	AX7	AX6	AX5	AX4

(Default: AX7-AX4=0H / Register Address: 1H)

(15-4) Window Start Row Address

The “Window Start Row Address” instruction specifies the row address of the start point. Available setting range is from (00H) to (7FH), and outside this range is not allowed. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	AY3	AY2	AY1	AY0

(Default: AY3-AY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	AY6	AY5	AY4

(Default: AY6-AY4=0H / Register Address: 3H)

(15-5) Initial Display Line

This instruction sets the row address, which corresponds to an initial COM and is normally positioned on top of a screen in full display. For more information, refer to “(15-16) Initial COM”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LA3	LA2	LA1	LA0

(Default: LA3-LA0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LA6	LA5	LA4

(Default: LA6-LA4=0H / Register Address: 5H)

Table 21 Initial Display Line Address

LA6	LA5	LA4	LA3	LA2	LA1	LA0	Row Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
⋮							⋮
1	1	1	1	1	1	1	127

(15-6) N-line Inversion

The number of N line is selected in between “2” and “128”. When the N-line inversion is enabled by setting “1” at the D₂ (NLIN) bit of the “Display Control (2)” instruction, the FR toggles once every N lines. When the N-line inversion is disabled by setting “0” at this bit, the FR toggles by the frame.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	N3	N2	N1	N0

(Default: N3-N0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	N6	N5	N4

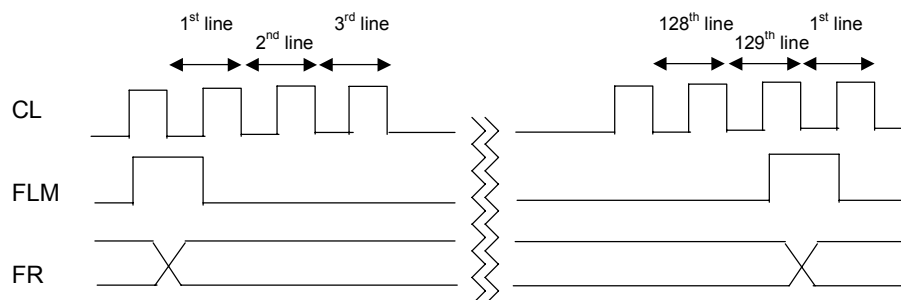
(Default: N6-N4=0H / Register Address: 7H)

Table 22 N-line Inversion

N6	N5	N4	N3	N2	N1	N0	N Line
0	0	0	0	0	0	0	Inhibited
0	0	0	0	0	0	1	2
⋮							⋮
1	1	1	1	1	1	1	128

NOTE1) N Line=(N Value)+1

N-line inversion OFF



N-line inversion ON

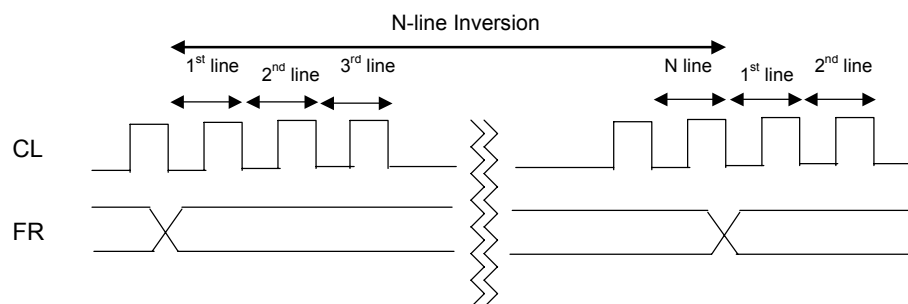


Fig 19 N-line Inversion Timing (1/129 Duty)

(15-7) Display Control (1)

The “Display Control (1)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	0	1	0	0	0	SHIFT	MON	ALL ON	ON /OFF

(Default: [SHIFT,MON,ALLON,ON/OFF]=0H / Register Address: 8H)

D₀ (ON/OFF)

ON/OFF=0 : Display OFF (All COM/SEG fixed at V_{SSH} level)

ON/OFF=1 : Display ON

D₁ (ALLON)

This bit forcibly turns on all pixels regardless of display data. This bit has a priority over the “REV” bit of the “Display Control (2)” instruction.

ALLON=0 : Normal

ALLON=1 : All pixels ON

D₂ (MON)

MON=0 : Grayscale Mode (Variable 16-grayscale, Variable 8-grayscale or Fixed 8-grayscale Mode)

MON=1 : B&W Mode

D₃ (SHIFT)

SHIFT=0 : COM₀ → COM₁₂₇

SHIFT=1 : COM₀ ← COM₁₂₇

(15-8) Display Control (2)

The “Display Control (2)” instruction controls display conditions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	REV	NLIN	SWAP	*

(Default: [REV,NLIN,SWAP]=0H / Register Address: 9H)

D₁ (SWAP)

This bit swaps palettes A_j and palettes C_j (j=0-15). This function reduces the restrictions on the IC position of an LCD module. For more information, refer to “(17) SWAP FUNCTION”.

SWAP=0 : SWAP OFF
SWAP=1 : SWAP ON

D₂ (NLIN)

This bit enables the N-line inversion.

NLIN=0 : N-line Inversion OFF (FR toggles by the frame.)
NLIN=1 : N-line Inversion ON (FR toggles once every N lines.)

D₃ (REV)

This bit enables the reverse display function that reverses the polarities of all display data without changing the DDRAM.

REV=0 : Reverse Display OFF (Normal)
REV=1 : Reverse Display ON

Table 23 Reverse Display ON/OFF

REV	Display	DDRAM Data → Display Data	
0	Normal	0	0
		1	1
1	Reverse	0	1
		1	0

(15-9) Increment/Decrement Control

The “HV”, “XD” and “YD” bits set either auto-increment or auto-decrement mode to the column address and row address individually. Once this mode is set up, the column address, row address or both are automatically counted up or down, whenever the DDRAM is accessed. This instruction is used for the window area setting as well as the “Window Start Column/Row Address” and “Window End Column/Row Address” instructions. The display-rotation function or the mirror-inversion function is also enabled by this setting. For more information, refer to “(4-3) DDRAM Access Direction”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	AIM	HV	XD	YD

(Default: [AIM,HV,XD,YD]=0H / Register Address: AH)

D₀ (YD), D₁ (XD), D₂ (HV)

Table 24 Horizontal/Vertical & Increment/Decrement

HV	XD	YD	X	Y	Direction
0	0	0	Increment	Increment	Horizontal
0	0	1	Increment	Decrement	
0	1	0	Decrement	Increment	
0	1	1	Decrement	Decrement	
1	0	0	Increment	Increment	Vertical
1	0	1	Increment	Decrement	
1	1	0	Decrement	Increment	
1	1	1	Decrement	Decrement	

D₃ (AIM)

Table 25 Read-modify-write ON/OFF

AIM	Increment Mode	NOTE
0	Read-modify-write OFF	1
1	Read-modify-write ON	2

NOTE1) Increment or decrement in writing and reading display data

NOTE2) Increment or decrement in writing display data only

(15-10) Power Control

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	AMPON	HALT	DCON	ACL

(Default: [AMPON,HALT,DCON,ACL]=0H / Register Address: BH)

D₀ (ACL)

This bit initializes the internal LCD power supply.

ACL=0 : Initialization OFF (Normal)
 ACL=1 : Initialization ON

NOTE) During the initialization, "1" is read out as the status of the "ACL" bit by the "Register Read" instruction. After the initialization, it is "0". As the CLK triggers the initialization, the "wait time" at least equivalent to 2 cycles of the CLK is required for the next instruction.

D₁ (DCON)

The "DCON" bit activates the voltage booster.

DCON=0 : Voltage Booster OFF
 DCON=1 : Voltage Booster ON

D₂ (HALT)

The "HALT" bit enables the power save mode. During the power save, operating current is down to the stand-by level. The internal state of the LSI in the power save mode is listed below.

HALT=0 : Power Save OFF (Normal)
 HALT=1 : Power Save ON

Internal State in Power Save Mode (HALT="1")

- Internal oscillator and internal LCD power supply are halted.
- All segment and common drivers are fixed at V_{SSH} level.
- External clock to the OSC1 cannot be accepted.
- Display data in the DDRAM is being maintained.
- Data in the instruction registers are being maintained.
- V_{LCD}, V₁, V₂, V₃ and V₄ are in high impedance.

NOTE) In the power save ON sequence, execute the "Display OFF" prior to the "Power Save ON". In the power save OFF sequence, execute the "Power save OFF" prior to the "Display ON". If the "Power Save ON/OFF" instruction is executed during the "Display ON", unexpected pixels may be turned on instantly.

D₃ (AMPON)

The "AMPON" bit activates the voltage converter which includes the reference voltage generator, the voltage regulator and the LCD bias generator.

AMPON=0 : Voltage Converter OFF
 AMPON=1 : Voltage Converter ON

(15-11) Duty Cycle Ratio

The “Duty Cycle Ratio” instruction selects LCD duty cycle ratio, and is used to carry out the partial display in combination with other instructions such as the “Boost Level”, the “LCD Bias Ratio” and the “EVR Control”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	DS3	DS2	DS1	DS0

(Default: DS3-DS0=0H / Register Address: CH)

Table 26 Duty Cycle Ratio

DS3	DS2	DS1	DS0	Duty Cycle Ratio		# of Commons
				DSE=0	DES=1	
0	0	0	0	1/129	1/128	128 commons
0	0	0	1	1/121	1/120	120 commons
0	0	1	0	1/113	1/112	112 commons
0	0	1	1	1/105	1/104	104 commons
0	1	0	0	1/97	1/96	96 commons
0	1	0	1	1/89	1/88	88 commons
0	1	1	0	1/81	1/80	80 commons
0	1	1	1	1/73	1/72	72 commons
1	0	0	0	1/65	1/64	64 commons
1	0	0	1	1/57	1/56	56 commons
1	0	1	0	1/49	1/48	48 commons
1	0	1	1	1/41	1/40	40 commons
1	1	0	0	1/33	1/32	32 commons
1	1	0	1	1/25	1/24	24 commons
1	1	1	0	1/17	1/16	16 commons
1	1	1	1	Inhibited		

NOTE) Duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the D₁ (DSE) bit of the “Duty-1 ON/OFF” instruction. Refer to “(15-17) Duty-1 /Display Clock ON/OFF”.

(15-12) Boost Level

The “Boost level” selects the multiple of the voltage booster.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	VU2	VU1	VU0

(Default: VU2-VU0=0H / Register Address: DH)

Table 27 Boost Level

VU2	VU1	VU0	Boost Level
0	0	0	1 time (No boost)
0	0	1	2 times
0	1	0	3 times
0	1	1	4 times
1	0	0	5 times
1	0	1	6 times
1	1	0	Inhibited
1	1	1	Inhibited

(15-13) LCD Bias Ratio

The "LCD bias ratio" selects LCD bias ratio.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	0	*	B2	B1	B0

(Default: B2-B0=0H / Register Address: EH)

Table 28 LCD Bias Ratio

B2	B1	B0	LCD Bias Ratio
0	0	0	1/9
0	0	1	1/8
0	1	0	1/7
0	1	1	1/6
1	0	0	1/5
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

(15-14) Instruction Table Select

This instruction specifies an instruction table, and should be executed prior to other instructions.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	1	1	TST0	RE2	RE1	RE0

(Default: TST0, RE2-RE0=0H / Register Address: FH)

Table 29 Instruction Table Select

RE2	RE1	RE0	Instructions
0	0	0	Instruction Table (0)
0	0	1	Instruction Table (1)
0	1	0	Instruction Table (2)
0	1	1	Instruction Table (3)
1	0	0	Instruction Table (4)
1	0	1	Instruction Table (5)

NOTE) "TST0" bit must be "0". This is used for maker tests only.

(15-15) Palette A / B / C

Palette A0 (PS=0) / Palette A8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA03/ PA83	PA02/ PA82	PA01/ PA81	PA00/ PA80

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA04/ PA84

(Register Address: 1H)

Palette A1 (PS=0) / Palette A9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PA13/ PA93	PA12/ PA92	PA11/ PA91	PA10/ PA90

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PA14/ PA94

(Register Address: 3H)

Palette A2 (PS=0) / Palette A10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PA23/ PA103	PA22/ PA102	PA21/ PA101	PA20/ PA100

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PA24/ PA104

(Register Address: 5H)

Palette A3 (PS=0) / Palette A11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PA33/ PA113	PA32/ PA112	PA31/ PA111	PA30/ PA110

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PA34/ PA114

(Register Address: 7H)

Palette A4 (PS=0) / Palette A12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PA43/ PA123	PA42/ PA122	PA41/ PA121	PA40/ PA120

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PA44/ PA124

(Register Address: 9H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette A5 (PS=0) / Palette A13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PA53/ PA133	PA52/ PA132	PA51/ PA131	PA50/ PA130

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PA54/ PA134

(Register Address: BH)

Palette A6 (PS=0) / Palette A14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PA63/ PA143	PA62/ PA142	PA61/ PA141	PA60/ PA140

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PA64/ PA144

(Register Address: DH)

Palette A7 (PS=0) / Palette A15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PA73/ PA153	PA72/ PA152	PA71/ PA151	PA70/ PA150

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PA74/ PA154

(Register Address: 1H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B0 (PS=0) / Palette B8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB03/ PB83	PB02/ PB82	PB01/ PB81	PB00/ PB80

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB04/ PB84

(Register Address: 3H)

Palette B1 (PS=0) / Palette B9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PB13/ PB93	PB12/ PB92	PB11/ PB91	PB10/ PB90

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PB14/ PB94

(Register Address: 5H)

Palette B2 (PS=0) / Palette B10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PB23/ PB103	PB22/ PB102	PB21/ PB101	PB20/ PB100

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PB24/ PB104

(Register Address: 7H)

Palette B3 (PS=0) / Palette B11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PB33/ PB113	PB32/ PB112	PB31/ PB111	PB30/ PB110

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PB34/ PB114

(Register Address: 9H)

Palette B4 (PS=0) / Palette B12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PB43/ PB123	PB42/ PB122	PB41/ PB121	PB40/ PB120

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PB44/ PB124

(Register Address: BH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette B5 (PS=0) / Palette B13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PB53/ PB133	PB52/ PB132	PB51/ PB131	PB50/ PB130

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PB54/ PB134

(Register Address: DH)

Palette B6 (PS=0) / Palette B14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PB63/ PB143	PB62/ PB142	PB61/ PB141	PB60/ PB140

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PB64/ PB144

(Register Address: 1H)

Palette B7 (PS=0) / Palette B15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PB73/ PB153	PB72/ PB152	PB71/ PB151	PB70/ PB150

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PB74/ PB154

(Register Address: 3H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C0 (PS=0) / Palette C8 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC03/ PC83	PC02/ PC82	PC01/ PC81	PC00/ PC80

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC04/ PC84

(Register Address: 5H)

Palette C1 (PS=0) / Palette C9 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	PC13/ PC93	PC12/ PC92	PC11/ PC91	PC10/ PC90

(Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	*	PC14/ PC94

(Register Address: 7H)

Palette C2 (PS=0) / Palette C10 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PC23/ PC103	PC22/ PC102	PC21/ PC101	PC20/ PC100

(Register Address: 8H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	*	PC24/ PC104

(Register Address: 9H)

Palette C3 (PS=0) / Palette C11 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PC33/ PC113	PC32/ PC112	PC31/ PC111	PC30/ PC110

(Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	*	*	PC34/ PC114

(Register Address: BH)

Palette C4 (PS=0) / Palette C12 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	PC43/ PC123	PC42/ PC122	PC41/ PC121	PC40/ PC120

(Register Address: CH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	0	1	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	1	*	*	*	PC44/ PC124

(Register Address: DH)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

Palette C5 (PS=0) / Palette C13 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	PC53/ PC133	PC52/ PC132	PC51/ PC131	PC50/ PC130

(Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	*	*	*	PC54/ PC134

(Register Address: 1H)

Palette C6 (PS=0) / Palette C14 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	PC63/ PC143	PC62/ PC142	PC61/ PB141	PC60/ PB140

(Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	*	*	PC64/ PC144

(Register Address: 3H)

Palette C7 (PS=0) / Palette C15 (PS=1)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	PC73/ PC153	PC72/ PC152	PC71/ PC151	PC70/ PC150

(Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	*	*	PC74/ PC154

(Register Address: 5H)

NOTE) Refer to the tables in “(6) GRAYSCALE PALETTE” for default setting.

(15-16) Initial COM

The “Initial COM” instruction specifies the common driver for a scan start common.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	SC3	SC2	SC1	SC0

(Default: SC3-SC0=0H / Register Address: 6H)

Table 30 Initial COM

SC3	SC2	SC1	SC0	Initial COM (SHIFT=0)	Initial COM (SHIFT=1)
0	0	0	0	COM ₀	COM ₁₂₇
0	0	0	1	COM ₄	COM ₁₂₃
0	0	1	0	COM ₈	COM ₁₁₉
0	0	1	1	COM ₁₆	COM ₁₁₁
0	1	0	0	COM ₂₄	COM ₁₀₃
0	1	0	1	COM ₃₂	COM ₉₅
0	1	1	0	COM ₄₀	COM ₈₇
0	1	1	1	COM ₄₈	COM ₇₉
1	0	0	0	COM ₅₆	COM ₇₁
1	0	0	1	COM ₆₄	COM ₆₃
1	0	1	0	COM ₇₂	COM ₅₅
1	0	1	1	COM ₈₀	COM ₄₇
1	1	0	0	COM ₈₈	COM ₃₉
1	1	0	1	COM ₉₆	COM ₃₁
1	1	1	0	COM ₁₀₄	COM ₂₃
1	1	1	1	COM ₁₁₂	COM ₁₅

(15-17) Duty-1 /Display Clock ON/OFF

This instruction controls ON (Duty-1) /OFF (Duty-0) and Display Clock ON/OFF.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	*	DSE	SON

(Default: SON,DSE=0H / Register Address: 7H)

D₀ (SON)

SON=0 : CL, FLM, FR, and CLK are fixed at “L” level.
SON=1 : CL, FLM, FR, and CLK are enabled.

D₁ (DSE)

The duty cycle ratio is subtracted by 1 (Duty-1) from the original duty cycle ratio by setting “1” at the “DSE” bit.

DSE=0 : OFF (Duty-0)
DSE=1 : ON (Duty-1)

NOTE) For the last common timing at “DSE=0”, all common drivers generate non-selective waveforms, and segment drivers generate the same waveforms as for the previous common timing. For instance, in 1/129 duty cycle, the segment waveforms for 129th common timing are the same as for 128th common timing (last line).

(15-18) Display Mode Control /Boost Clock Control

The “Display Mode Control” instruction sets up display modes such as the variable or fixed grayscale mode and the variable 8- or 16-grayscale mode. The D₂ (MON) bit of the “Display Control (1)” is used in combination. Refer to “(5) GRAY SCALE CONTROL CIRCUIT” and “(15-7) Display Control (1).” The D₁ and D₀ (FDC1 and FDC2) bits set the boost clock.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	PWM	C256	FDC1	FDC2

(Default: PWM,C256=0H / Register Address: 8H)

D₃ (PWM)

PWM=0 : Variable grayscale Mode (Variable 8-/16-grayscale Mode)
 PWM=1 : Fixed 8-grayscale Mode

D₂ (C256)

C256=0 : Variable 16-grayscale Mode at “PWM=0” (4096 colors)
 C256=1 : Variable 8-grayscale Mode at “PWM=0” (256 colors)

D₁ , D₀ (FDC1, FDC2)

Table 31 FDC1, FDC2

FDC1	FDC2	Boost Clock
0	0	1x
0	1	2x
1	0	4x
1	1	1/2x

(15-19) Bus Length

This instruction selects 8- or 16-bit bus length, and sets oscillator configuration as well.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	ABS	CKS	WLS

(Default: ABS,CKS,WLS=0H / Register Address: 9H)

D₀ (WLS)

WLS=0: 8-bit Bus Length
 WLS=1: 16-bit Bus Length

D₁ (CKS)

CKS =0: Internal Oscillator using an internal resistor
 CKS =1: External Clock, or Internal Oscillator using an external resistor

NOTE) Refer to “(11) OSCILLATOR”.

D₂ (ABS)

ABS=0: ABS Mode OFF (Normal)
 ABS=1: ABS Mode ON

(15-20) EVR Control

The “EVR Control” instruction adjusts V_{LCD} to optimize display contrast. This instruction is finally effective when both upper and lower bytes are transmitted in order to prevent high V_{LCD} . The setting order is upper byte first, then lower byte. Refer to “(12-2-3) Electrical Variable Resistor (EVR)”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	DV ₃	DV ₂	DV ₁	DV ₀

(Default: DV₃-DV₀=0H / Register Address: AH)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	1	*	DV ₆	DV ₅	DV ₄

(Default: DV₆-DV₄=0H / Register Address: BH)

Table 32 EVR Control

DV ₆	DV ₅	DV ₄	DV ₃	DV ₂	DV ₁	DV ₀	V_{LCD}
0	0	0	0	0	0	0	Low
0	0	0	0	0	0	1	:
			:				:
			:				:
1	1	1	1	1	1	1	High

Formula of VLCD

$$V_{LCD} [V] = 0.5 \times V_{REG} + M (V_{REG} - 0.5 \times V_{REG}) / 127$$

$$V_{BA} = V_{EE} \times 0.9$$

$$V_{REG} = V_{REF} \times N$$

V_{BA} : Output of the reference voltage generator
 V_{REF} : Input of the voltage regulator
 V_{REG} : Output of the voltage regulator
 N : Boost level
 M : EVR Value

(15-21) Frequency Control

The “Frequency Control” instruction adjusts the frame frequency.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	Rf2	Rf1	Rf0

(Default: DV₃-DV₀=0H / Register Address: DH)

Table 33 Frequency Control

Rf 2	Rf 1	Rf 0	Feedback Resistor Value
0	0	0	Reference Value
0	0	1	0.8 x Reference Value
0	1	0	0.9 x Reference Value
0	1	1	1.1 x Reference Value
1	0	0	1.2 x Reference Value
1	0	1	0.7 x Reference Value
1	1	0	1.3 x Reference Value
1	1	1	Inhibited

(15-22) Discharge ON/OFF

Discharge circuit is used to discharge out of the stabilizing capacitors placed on the V_{LCD}, V₁, V₂, V₃, V₄ and V_{OUT}. Refer to “(12-4) Discharge Circuit”.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	*	DIS2	DIS

(Default: DIS2,DIS1=0H / Register Address: EH)

D₀ (DIS)

DIS=0 : Discharge OFF
 DIS=1 : Discharge ON (Discharge from V_{LCD}, V₁, V₂, V₃ and V₄)

D₁ (DIS2)

DIS2=0 : Discharge OFF
 DIS2=1 : Discharge ON (Discharge from V_{OUT} through the internal resistor between V_{OUT} and V_{EE})

NOTE) Resistance is 100KΩ typical.

(15-23) Register Address

The “Register Address” instruction specifies a register address.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	1	0	0	RA3	RA2	RA1	RA0

(Default: RA3-RA0=BH / Register Address: CH)

(15-24) Register Read

The “Register Read” instruction reads out instruction data from the register which address is specified by the “Register Address” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	0	1	0/1	0/1	0/1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
*	*	*	*	Internal register data read			

(15-25) Window End Column Address

The “Window End Column Address” instruction specifies the column address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	0	EX3	EX2	EX1	EX0

(Default: EX3-EX0=0H / Register Address: 0H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	EX7	EX6	EX5	EX4

(Default: EX7-EX4=0H / Register Address: 1H)

(15-26) Window End Row Address

The “Window End Row Address” instruction specifies the row address of the end point. Refer to “(4-2) Window Area for DDRAM Access”. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	0	EY3	EY2	EY1	EY0

(Default: EY3-EY0=0H / Register Address: 2H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	1	1	*	EY6	EY5	EY4

(Default: EY6-EY4=0H / Register Address: 3H)

(15-27) Initial Line-reverse Address

The “Initial Line-reverse Address” instruction specifies the start line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	0	LS3	LS2	LS1	LS0

(Default: LS3-LS0=0H / Register Address: 4H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	0	1	*	LS6	LS5	LS4

(Default: LS6-LS4=0H / Register Address: 5H)

(15-28) Last Line-reverse Address

The “Last Line-reverse Address” instruction specifies the end line of the line-reverse display area. The setting order is lower byte first, then upper byte.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	0	LE3	LE2	LE1	LE0

(Default: LE3-LE0=0H / Register Address: 6H)

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	1	1	1	*	LE6	LE5	LE4

(Default: LE6-LE4=0H / Register Address: 7H)

(15-29) Line Reverse ON/OFF

The “Line Reverse ON/OFF” instruction enables the line-reverse display, and blink function as well. Note that the line reverse display cannot be used for entire display area. In this case, use the reverse display function by the D₃ (REV) bit of the “Display Control (2)” instruction.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	*	*	BT	LREV

(Default: BT,LREV=0H / Register Address: 8H)

D₀ (LREV)

- LREV =0 : Line Reverse OFF (Normal)
- LREV =1 : Line Reverse ON

D₁ (BT)

- BT =0 : No Blink
- BT =1 : Blink once every 32 frames

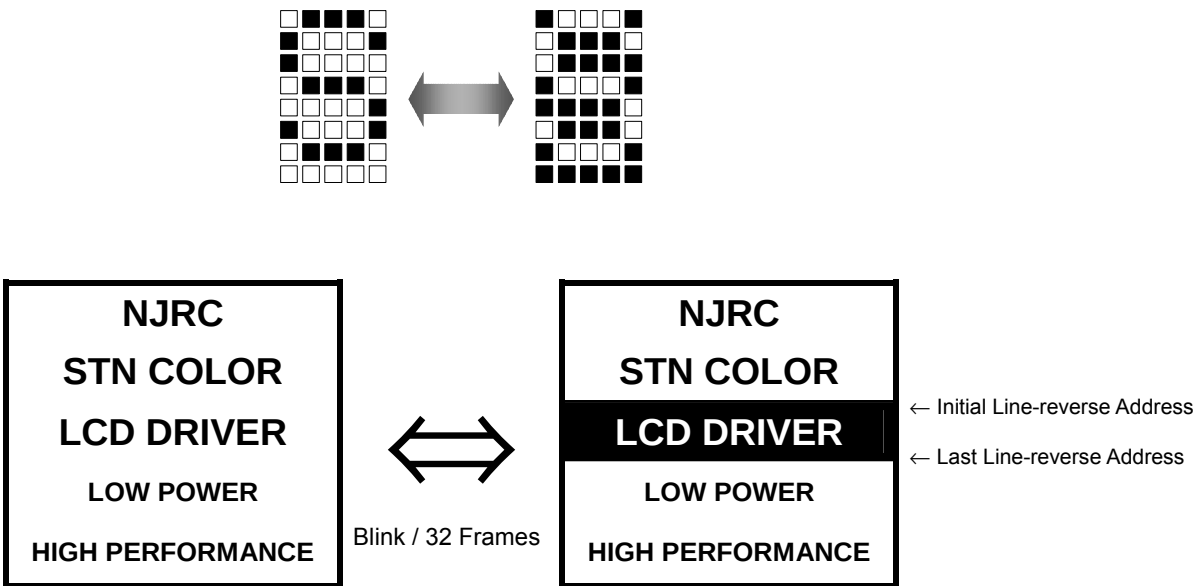


Fig 20 On-screen Image in Using Line-reverse Display and Blink Function

(15-30) Upper/Lower Palette Select /Icon Segment Access ON/OFF

The “Upper/Lower Palette Select” instruction selects either upper or lower palette register.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	1	*	*	ICON	PS

(Default: PS=0 / Register Address: 9H)

D₀ (PS)

PS=0 : Lower Palettes (PA00, PA01, PA02, PA03, ..., PC74)
 PS=1 : Upper Palettes (PA80, PA81, PA82, PA83, ..., PC154)

D₁ (ICON)

ICON=0 : Icon Segment Access OFF (DDRAM Access)
 ICON=1 : Icon Segment Access ON

NOTE) The Icon segment access is enabled by setting “1” at the D₁ (ICON) bit of this instruction, then the address (00H) or (01H) should be specified by the “Window Start Column Address” instruction.

(15-31) PWM Control

The “PWM control” instruction selects PWM type, as shown in Fig 21.

CSb	RS	RDb	WRb	RE2	RE1	RE0
0	1	1	0	1	0	1

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	1	0	PWMS	PWMA	PWMB	PWMC

(Default: PWMS,PWMA,PWMB,PWMC=0H / Register Address: AH)

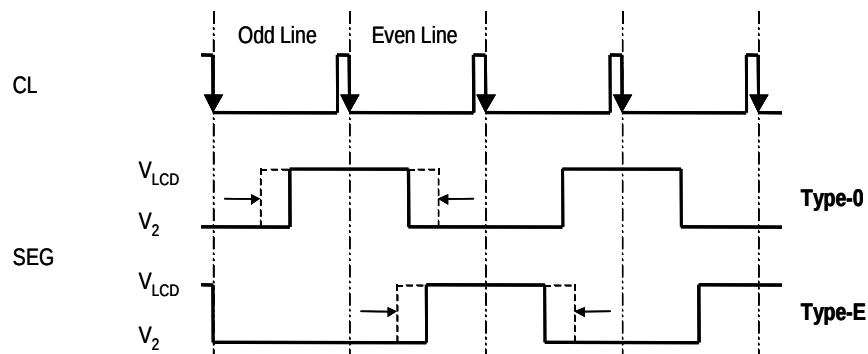
D₃ (PWMS)

PWMS=0 : Type 1
 PWMS=1 : Type 2

D₂ (PWMA), D₁ (PWMB), D₀ (PWMC)

PWMZ=0 (Z=A, B and C): Type 1-O
 PWMZ=1 (Z=A, B and C): Type 1-E

PWM Type 1 (PWMS=0)



PWM Type 2 (PWMS=1)

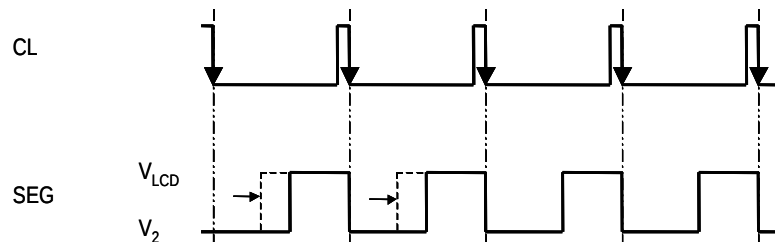


Fig 21 PWM Control

(16) PARTIAL DISPLAY FUNCTION

The partial display function activates specified area on an LCD screen, or equivalently, common drivers are simply scanning this specified area. This function allows LCD modules to work in a minimum duty cycle ratio to minimize power consumption. The partial display function is carried out by the combination of the “Duty Cycle Ratio”, “LCD Bias Ratio”, “Boost Level” and “EVR Control” instructions. For more information, refer to “(15-11) Duty Cycle Ratio”, “(15-12) Boost Level”, “(15-13) LCD Bias Ratio” and “(15-20) EVR Control”. Typical setting sequence is shown in “(19-4) Partial Display Sequence”.

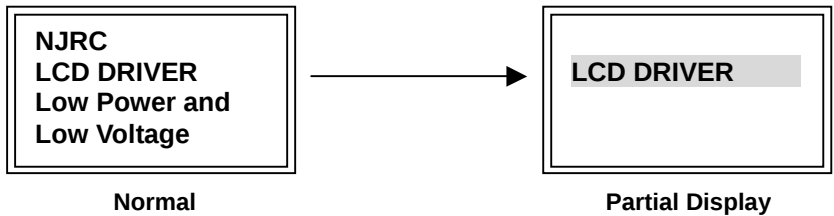


Fig 22 On-screen Image in Using Partial Display Function

(17) SWAP FUNCTION

The swap function switches the palettes Aj and the palettes Cj (j=0-15), and is controlled by the D₁ (SWAP) bit of the “Display Control (2)” instruction. This function reduces the restrictions on the IC position of an LCD module. Fig 23 “Overview of Swap Function” illustrates general outlines of internal operations, and (17-1-1) through (17-1-4) show each configuration on a mode-by-mode basis.

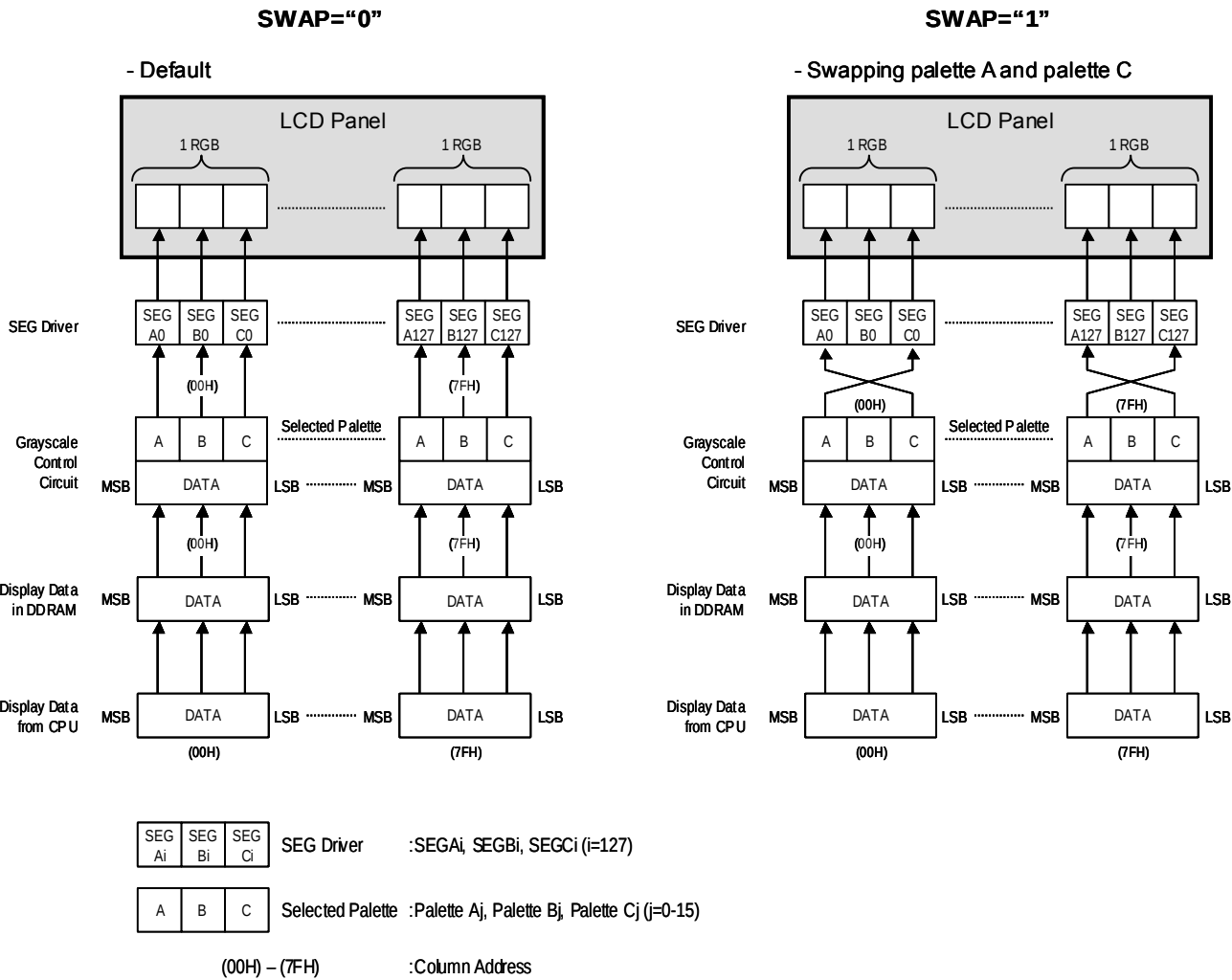
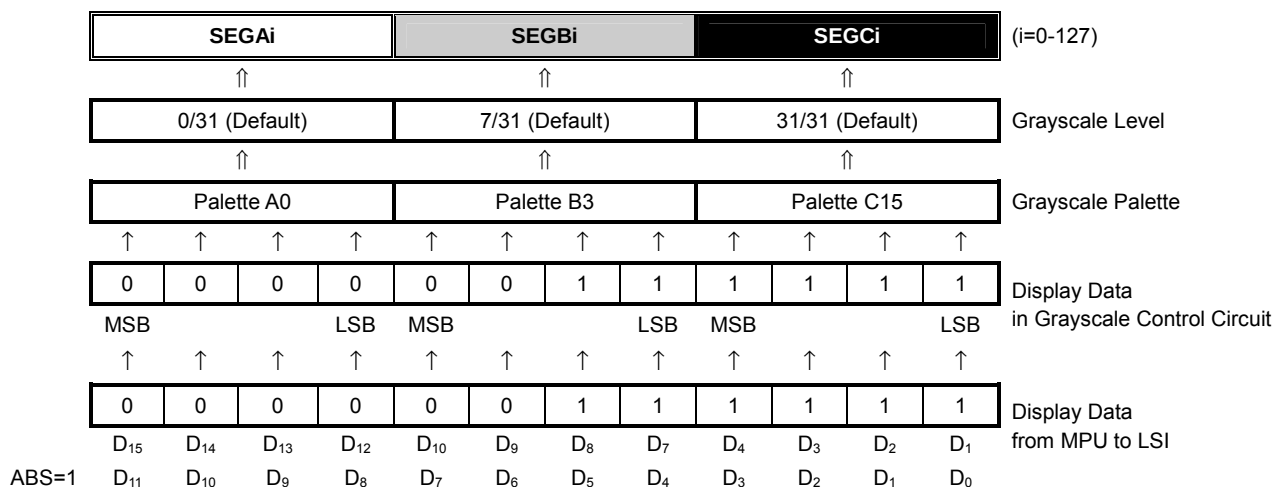


Fig 23 Overview of SWAP Function

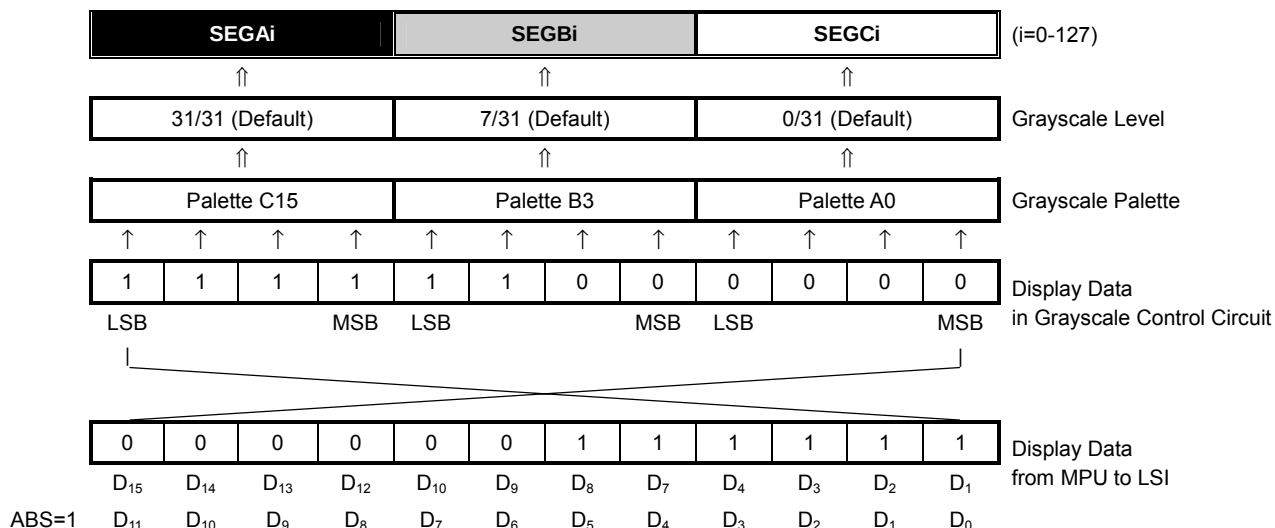
(17-1) Swap Function in Variable 16-grayscale Mode

16-bit Bus Length

SWAP=0



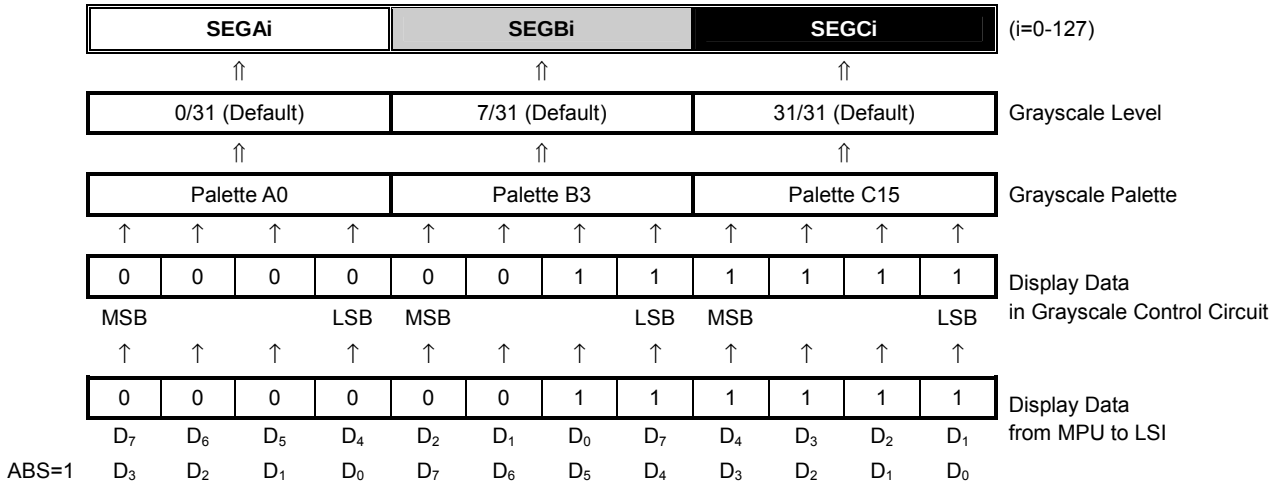
SWAP=1



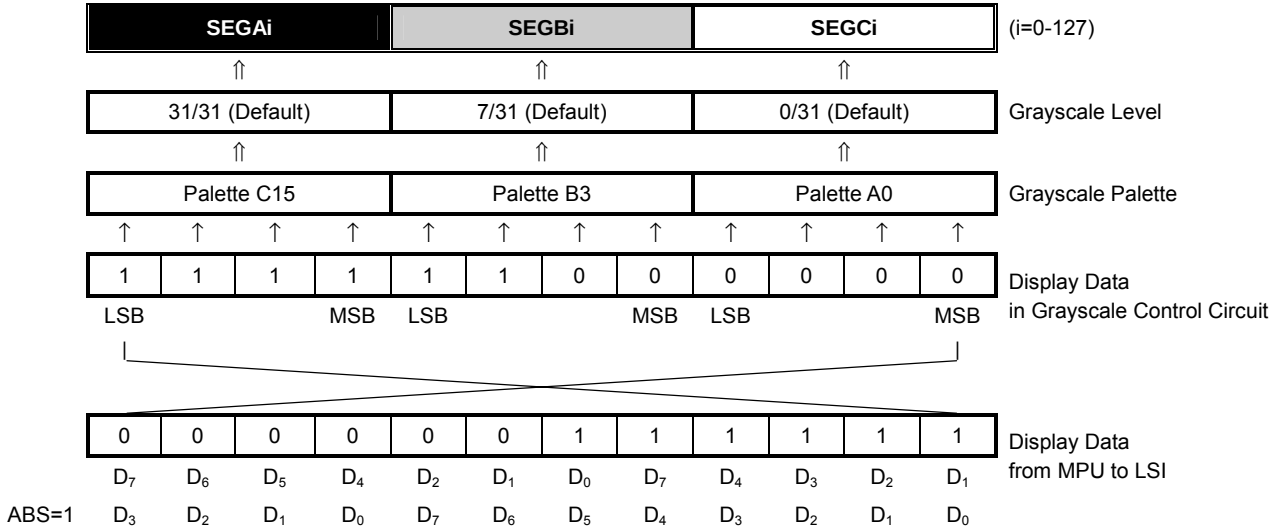
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

8-bit Bus Length

SWAP=0



SWAP=1

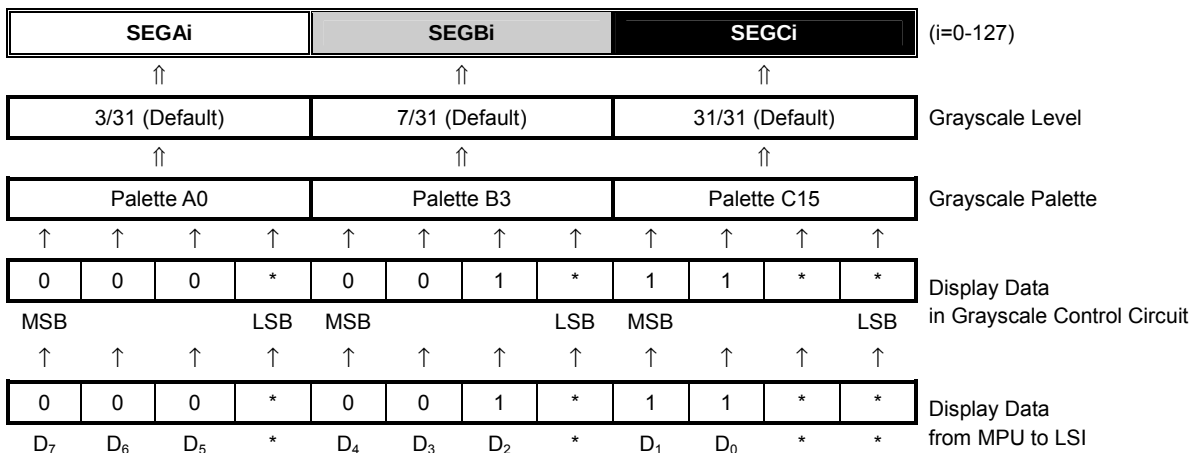


NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

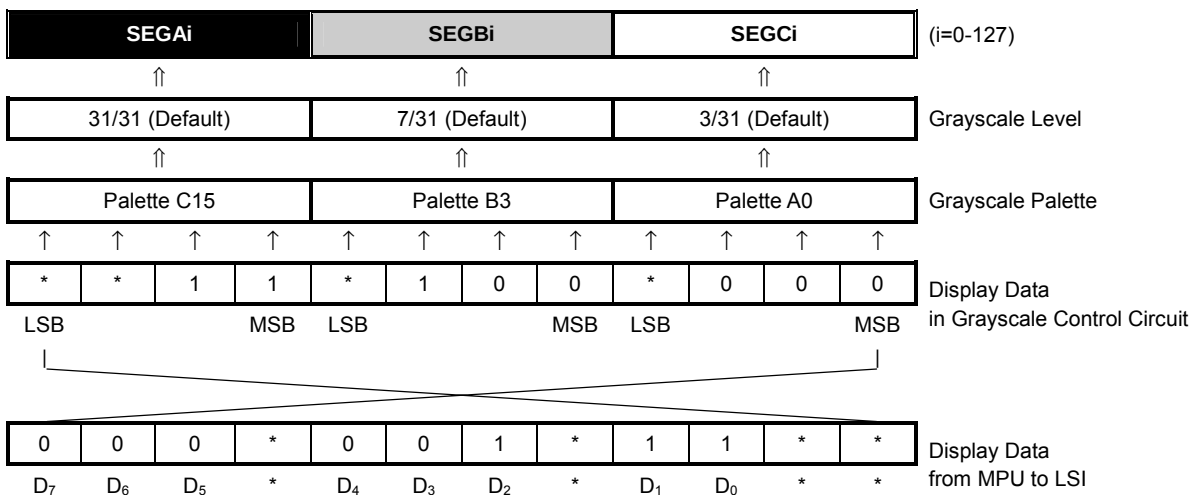
(17-2) Swap Function in Variable 8-Grayscale Mode

8-bit Bus Length

SWAP=0



SWAP=1

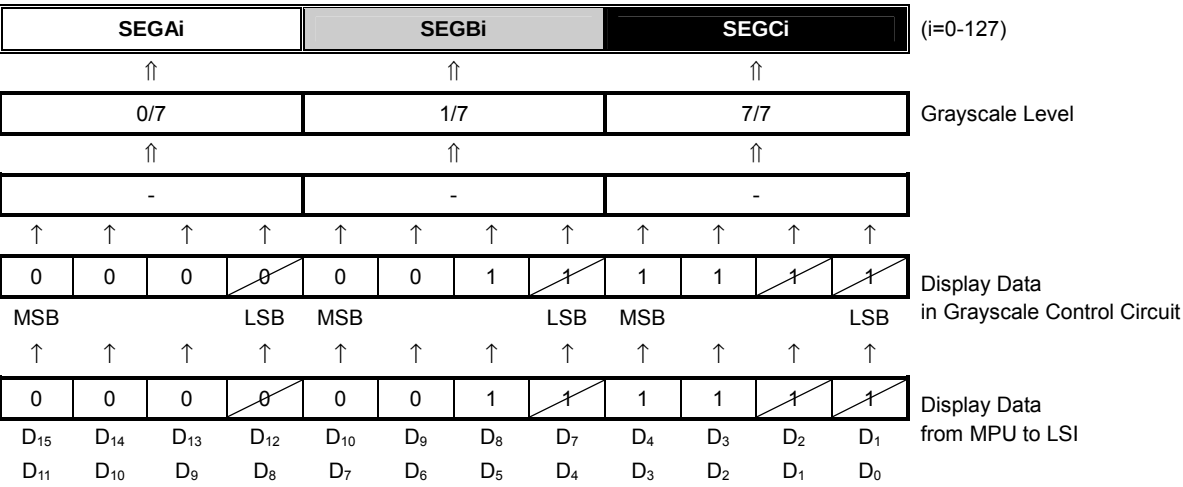


NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

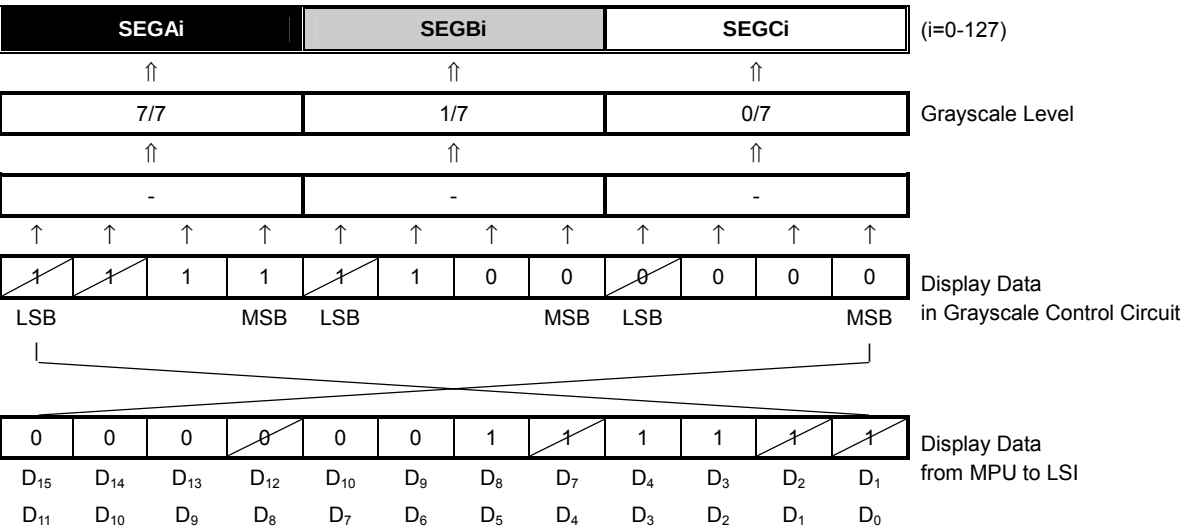
(17-3) Swap Function in Fixed 8-grayscale Mode

16-bit Bus Length

SWAP=0



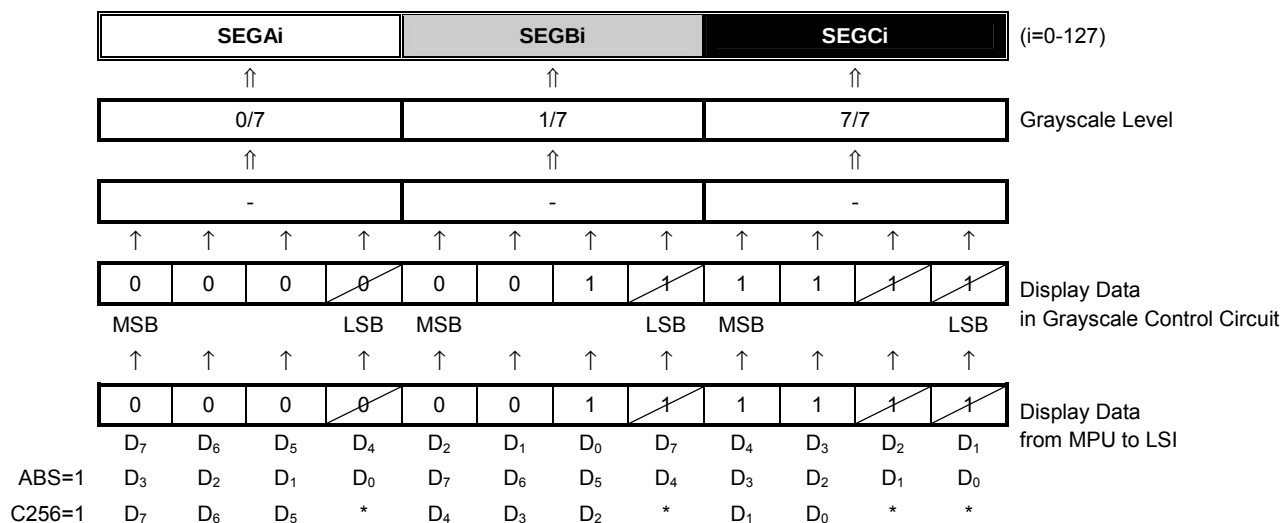
SWAP=1



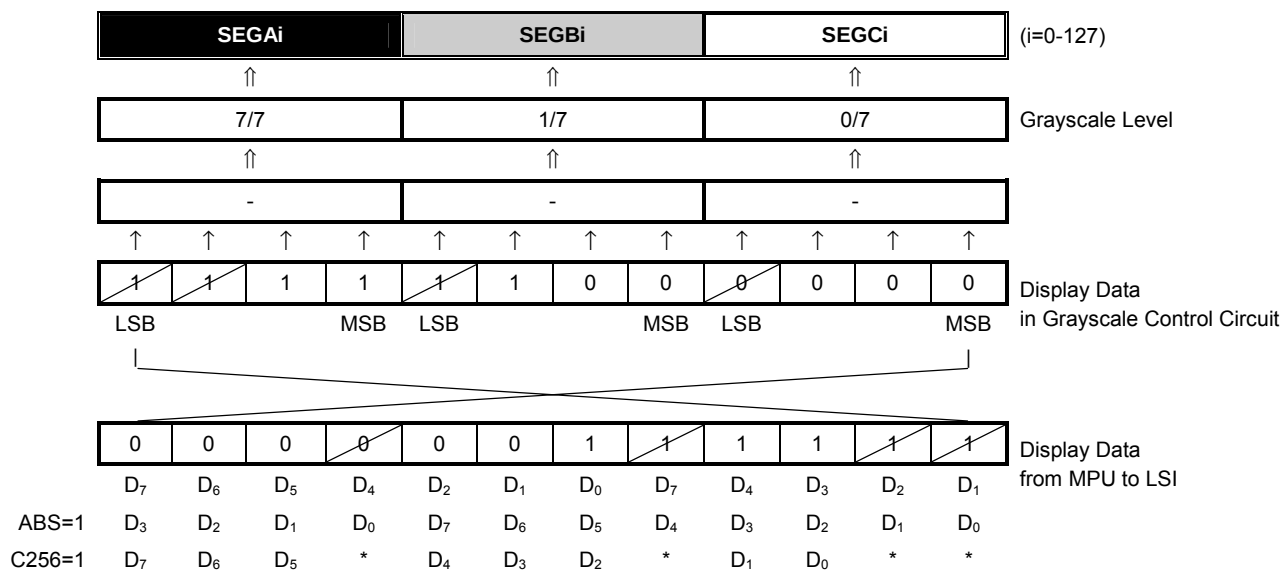
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



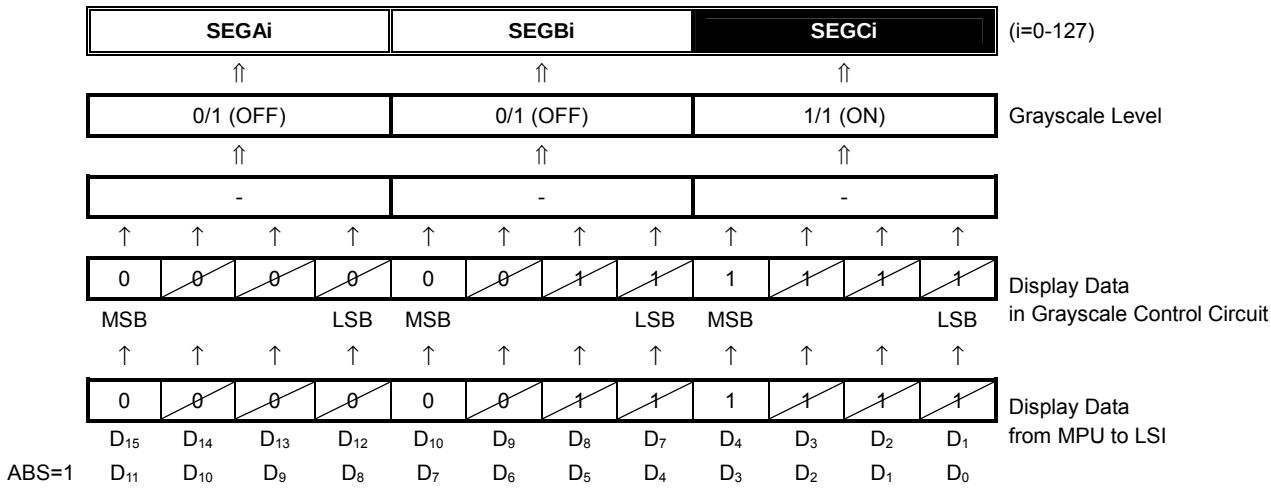
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".

NOTE2) The data indicated with a slash mark (/) is invalid.

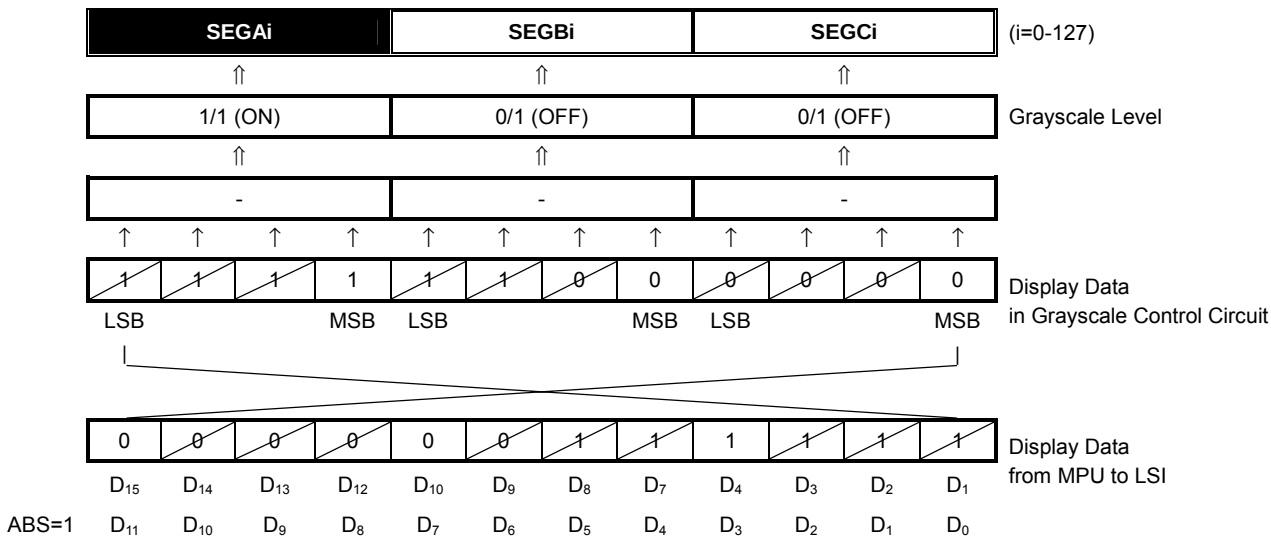
(17-4) Swap Function in B&W Mode

16-bit Bus Length

SWAP=0



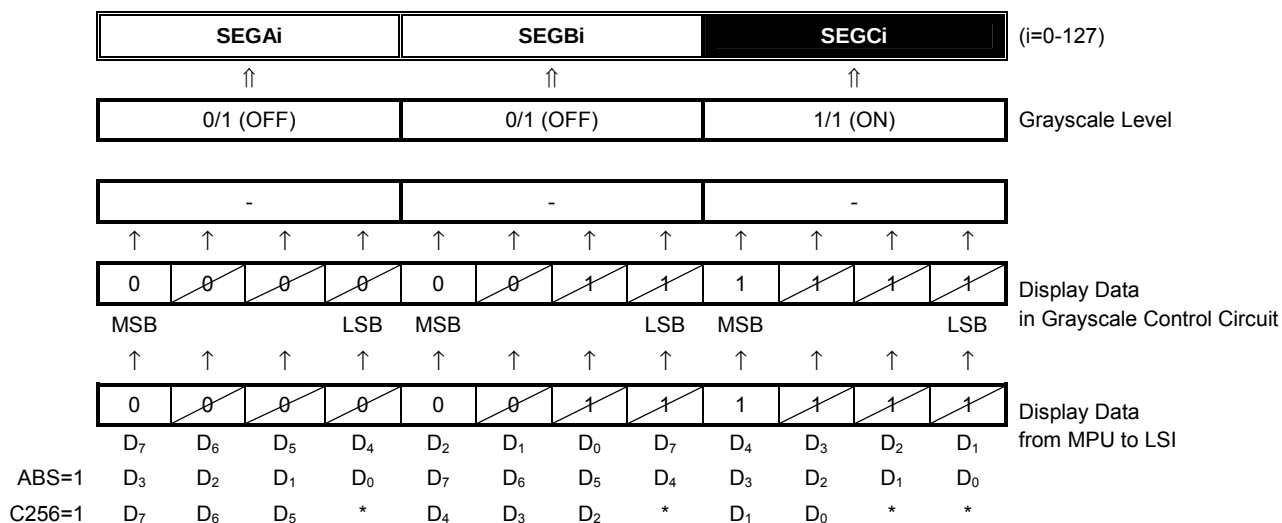
SWAP=1



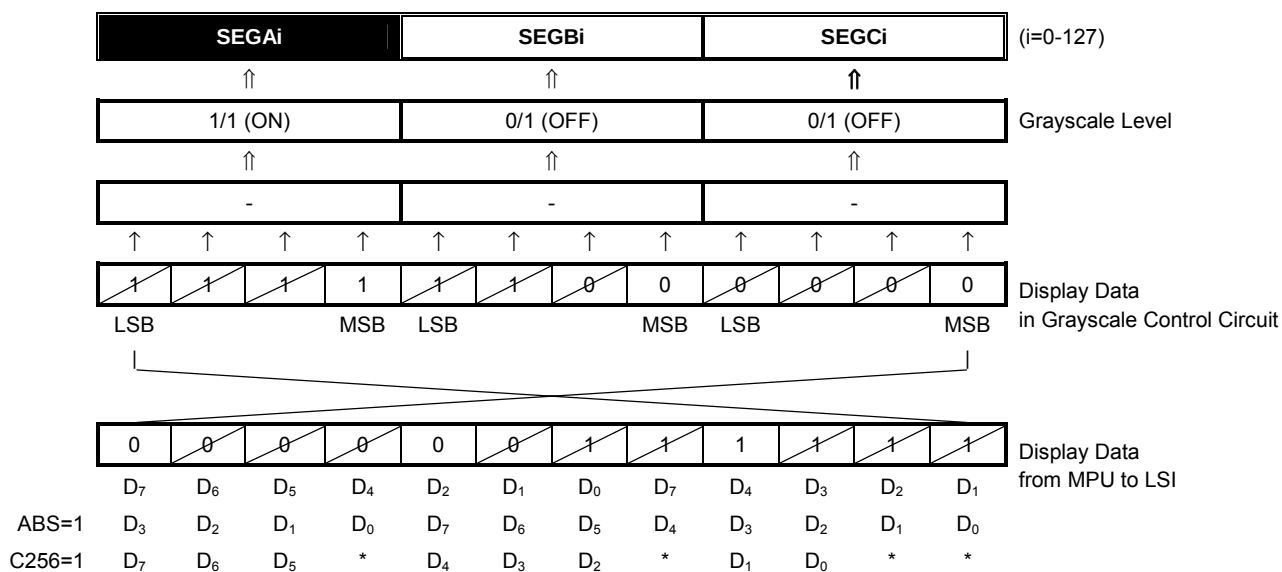
NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as "0".
NOTE2) The data indicated with a slash mark (/) is invalid.

8-bit Bus Length

SWAP=0



SWAP=1



NOTE1) Without a special note on the left, the ABS and C256 bits are regarded as “0”.

NOTE2) The data indicated with a slash mark (/) is invalid.

(18) RELATION BETWEEN ROW ADDRESS AND COMMON DRIVER

The relation between row address and common driver is changed by the D₃ (SHIFT) bit of the “Display Control (1)” and the “Duty Cycle Ratio”, “Initial Display Line” and “Initial COM” instructions.

When the “Initial Display Line” is set to (LA6:LA0=00H: Address “0”), the row address corresponding to an initial COM is “0”. However, if the “Initial Display Line” is other than “0”, the row address is shifted from “0” by just that address. For instance, when the initial display line address is (LA6:LA0=05H: Address “5”) and the initial COM is (SC3:SC0=1H), the row address on the initial COM is “5” and the initial COM is “COM₄”.

(18-1) through (18-5) illustrate the examples of the relation between row address and common driver.

(18-1) SHIFT=0, Initial Display Line “0”, Duty Cycle Ratio “1/129”

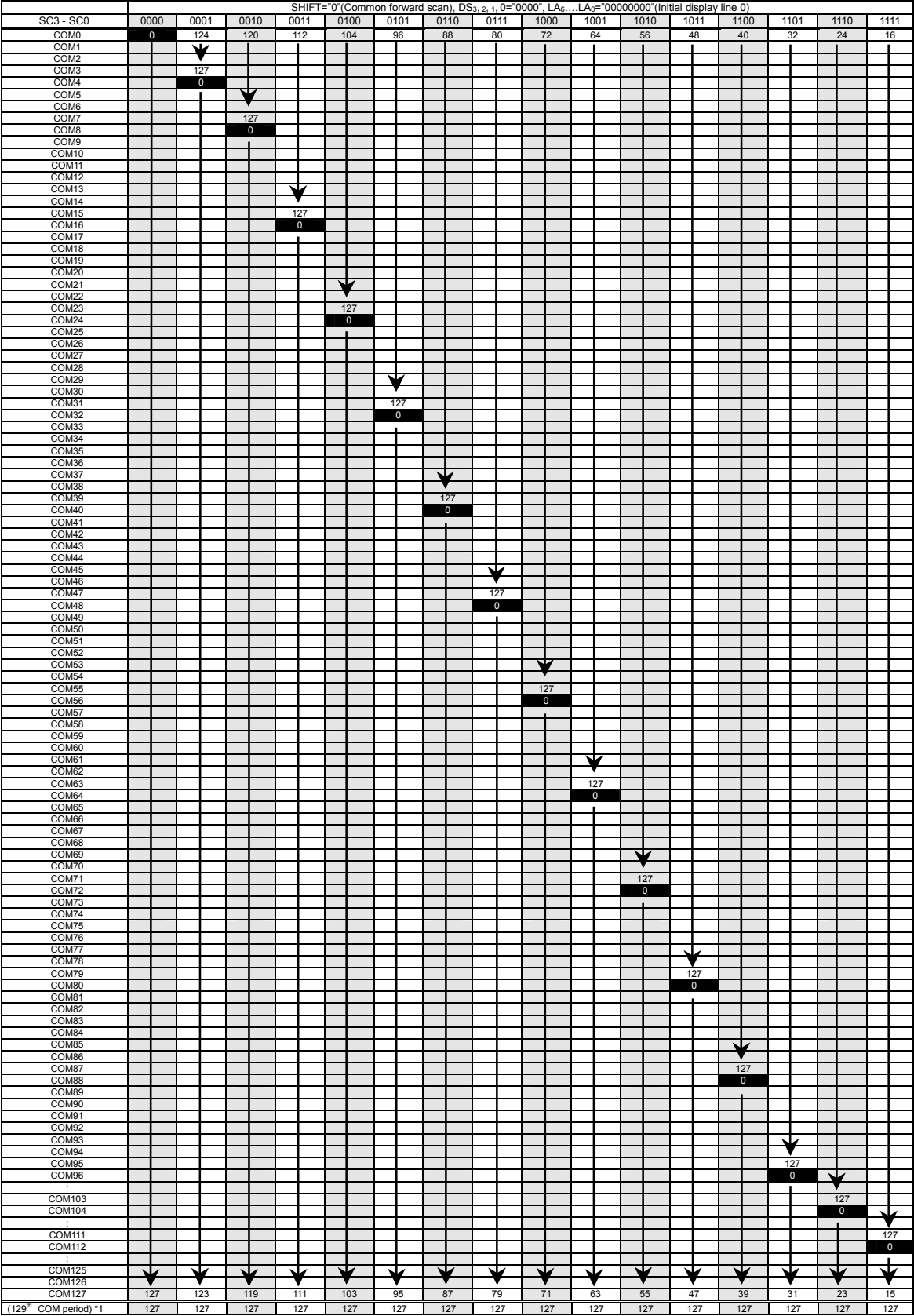


Fig 24 Relation between Row address and Common Driver (1)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 129th COM timing are the same as for 128th COM timing (Row address “127”).

(18-2) SHIFT=0, Initial Display Line "0", Duty Cycle Ratio "1/17"

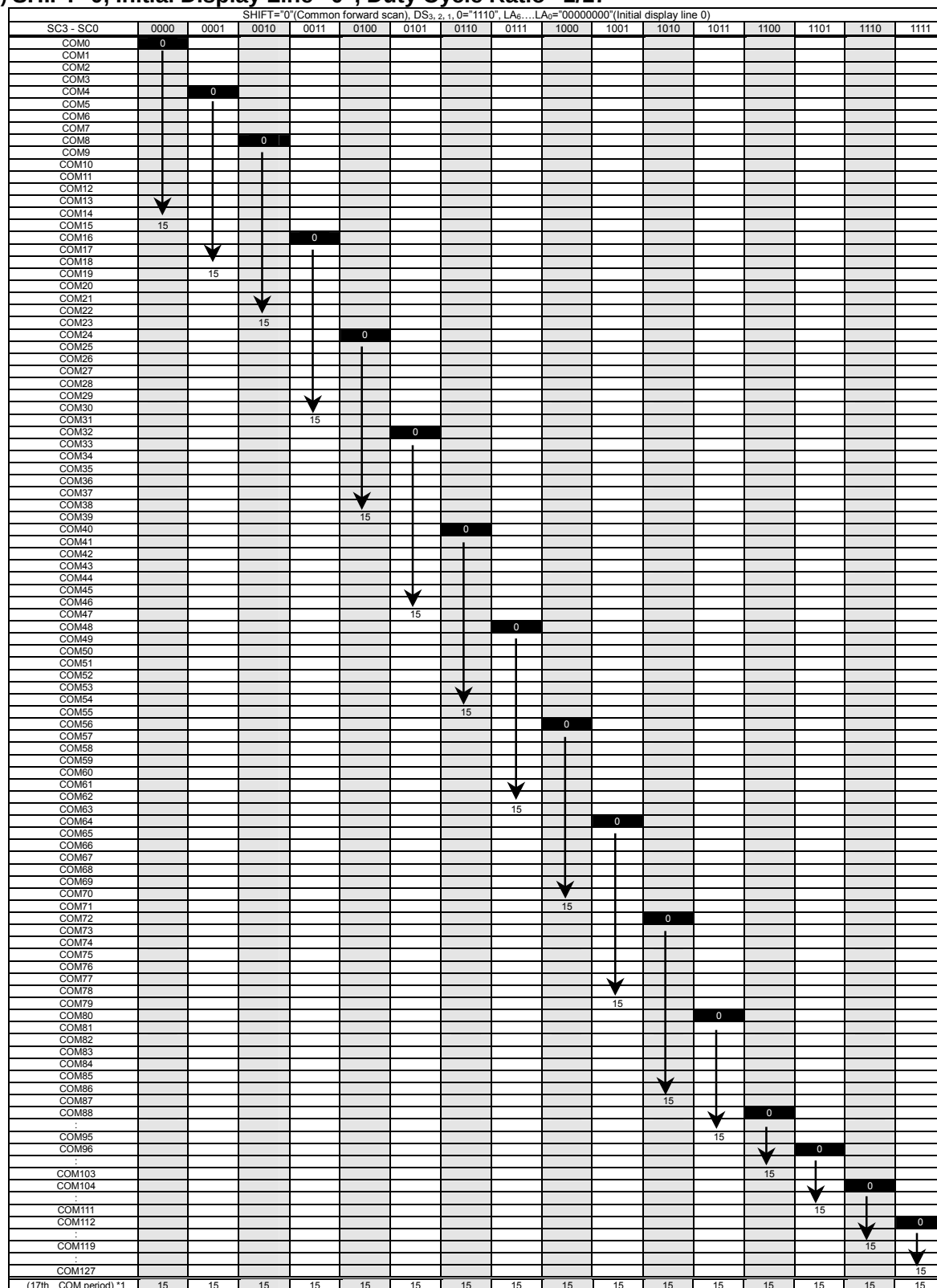


Fig 25 Relation between Row address and Common Driver (2)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 17th COM timing are the same as for 16th COM timing (Row address "15").

(18-3) SHIFT=1, Initial Display Line “0”, Duty Cycle Ratio “1/129”

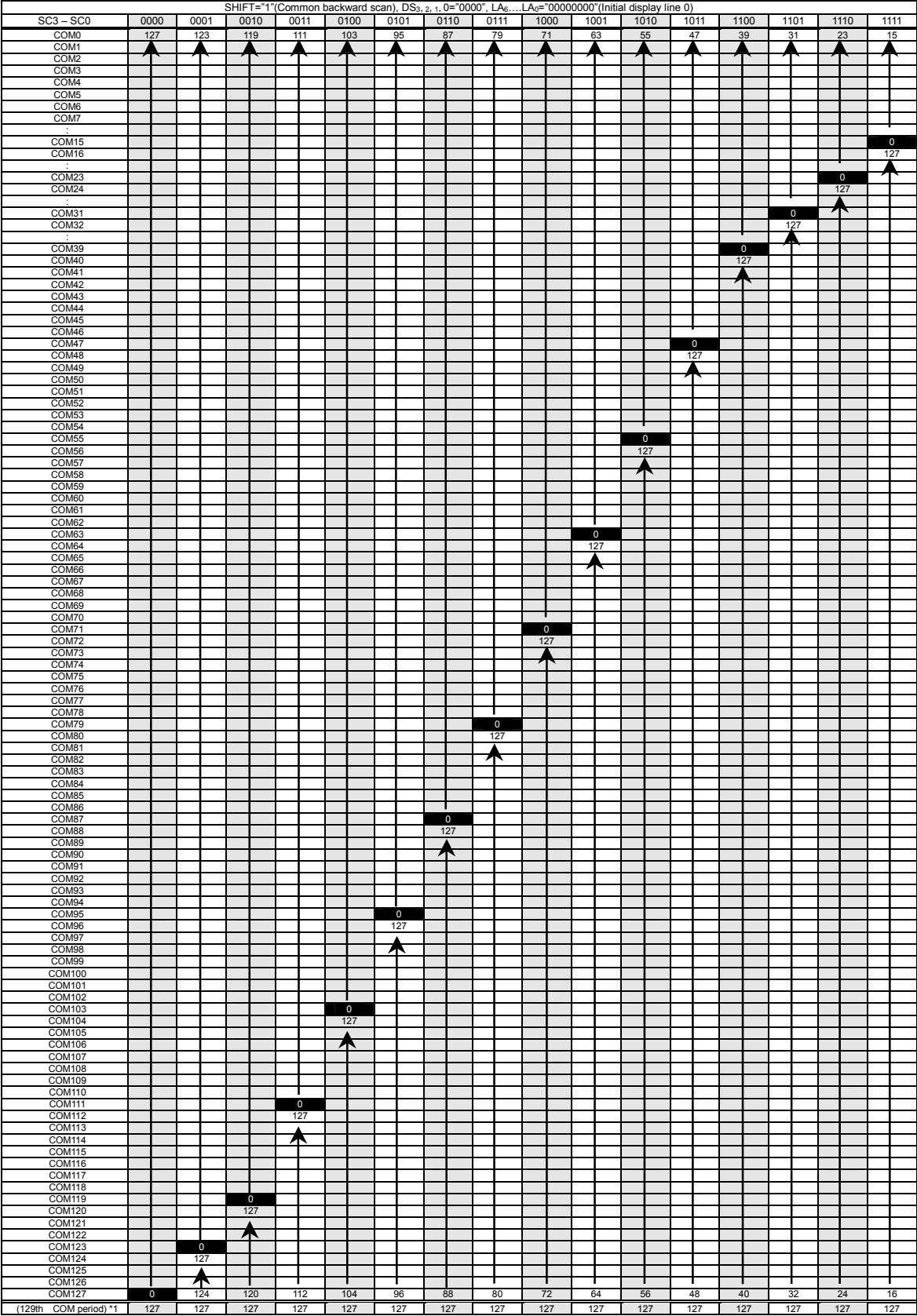


Fig 26 Relation between Row address and Common Driver (3)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address
NOTE2) Segment waveforms for 129th COM timing are the same as for 128th COM timing (Row address “127”).

(18-4) SHIFT=0, Initial Display Line "5", Duty Cycle Ratio "1/129"

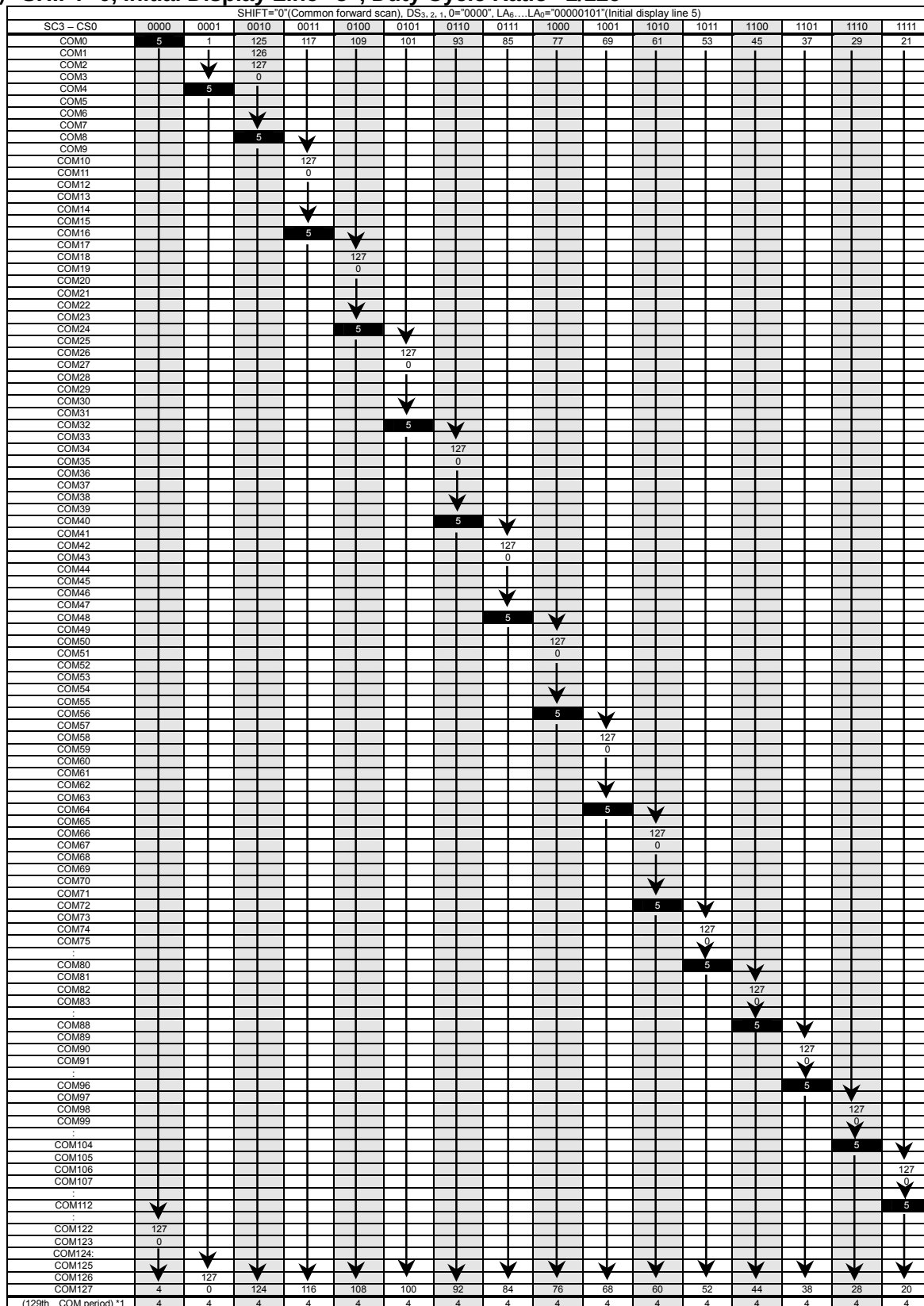


Fig 27 Relation between Row address and Common Driver (4)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

NOTE2) Segment waveforms for 129th COM timing are the same as for 128th COM timing.

(18-5) SHIFT=0, Initial Display Line “0”, Duty Cycle Ratio “1/128” (Dity-1 ON)

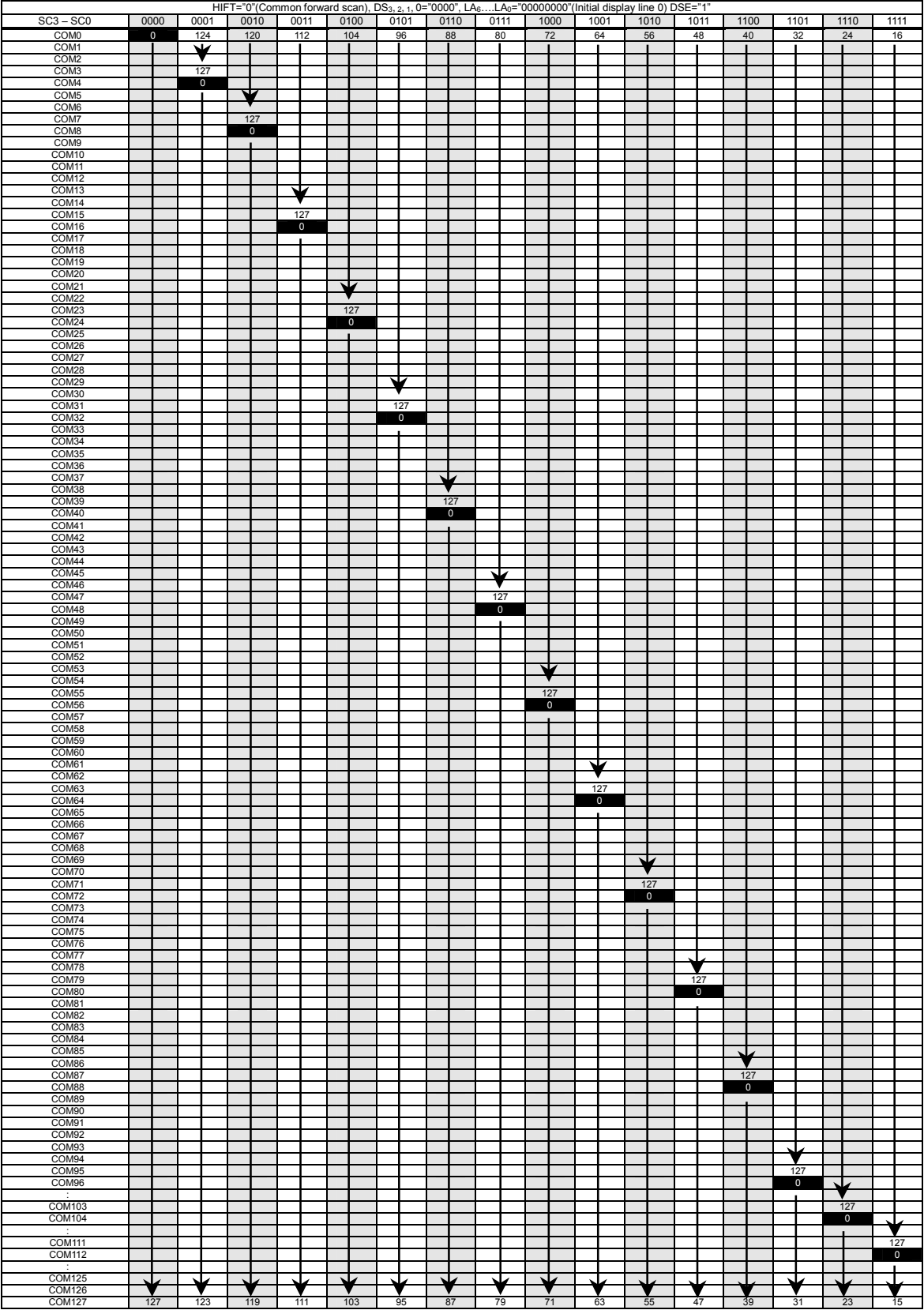
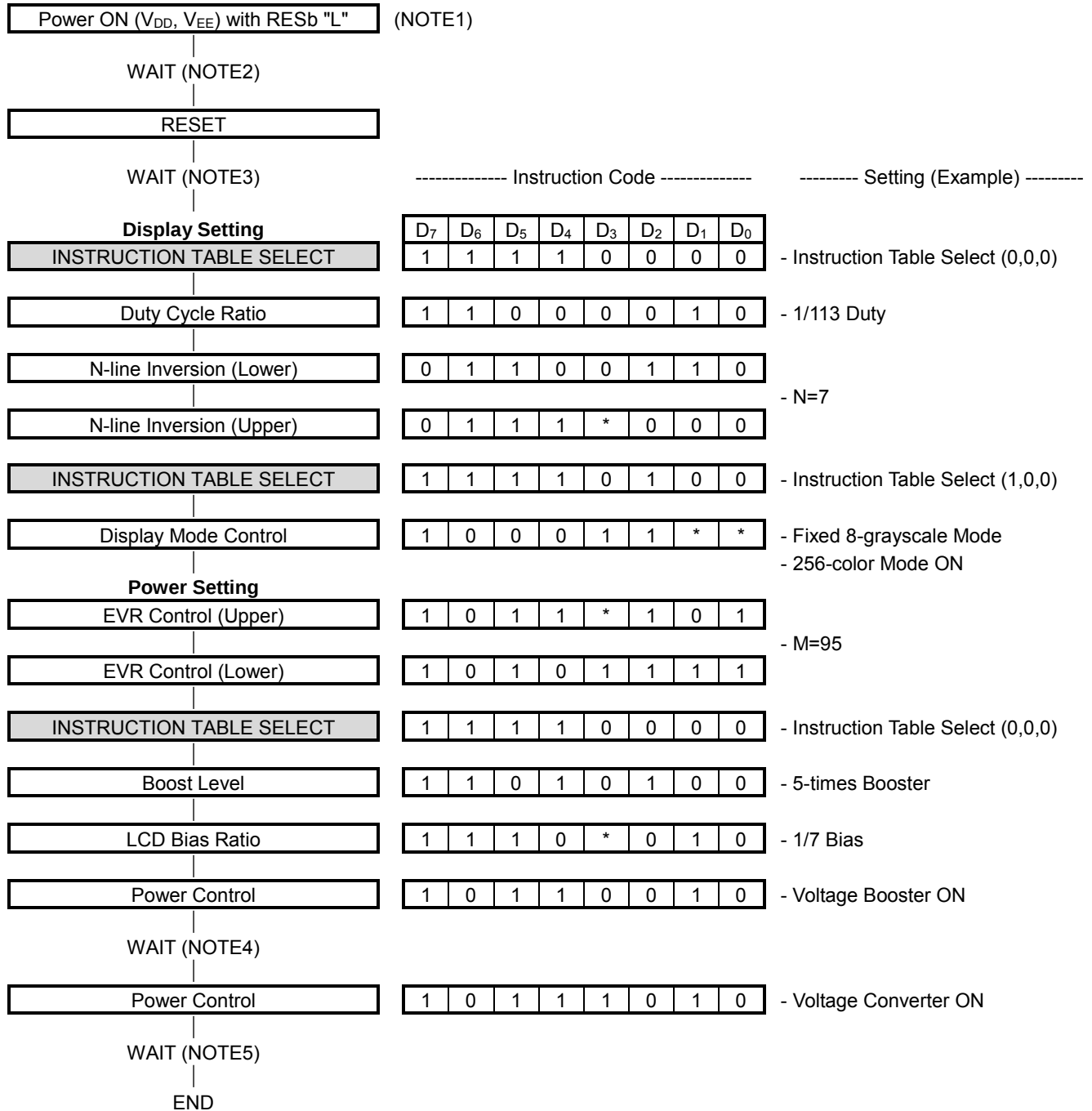


Fig 28 Relation between Row address and Common Driver (5)

NOTE1) DS: Duty Cycle Ratio / SC: Initial COM / LA: Initial Display Line Address

(19) TYPICAL INSTRUCTION SEQUENCES

(19-1) Initialization Sequence in Using Internal LCD Power Supply



NOTE1) If different power sources are applied to the V_{DD} and the V_{EE} , turn on the V_{DD} first.

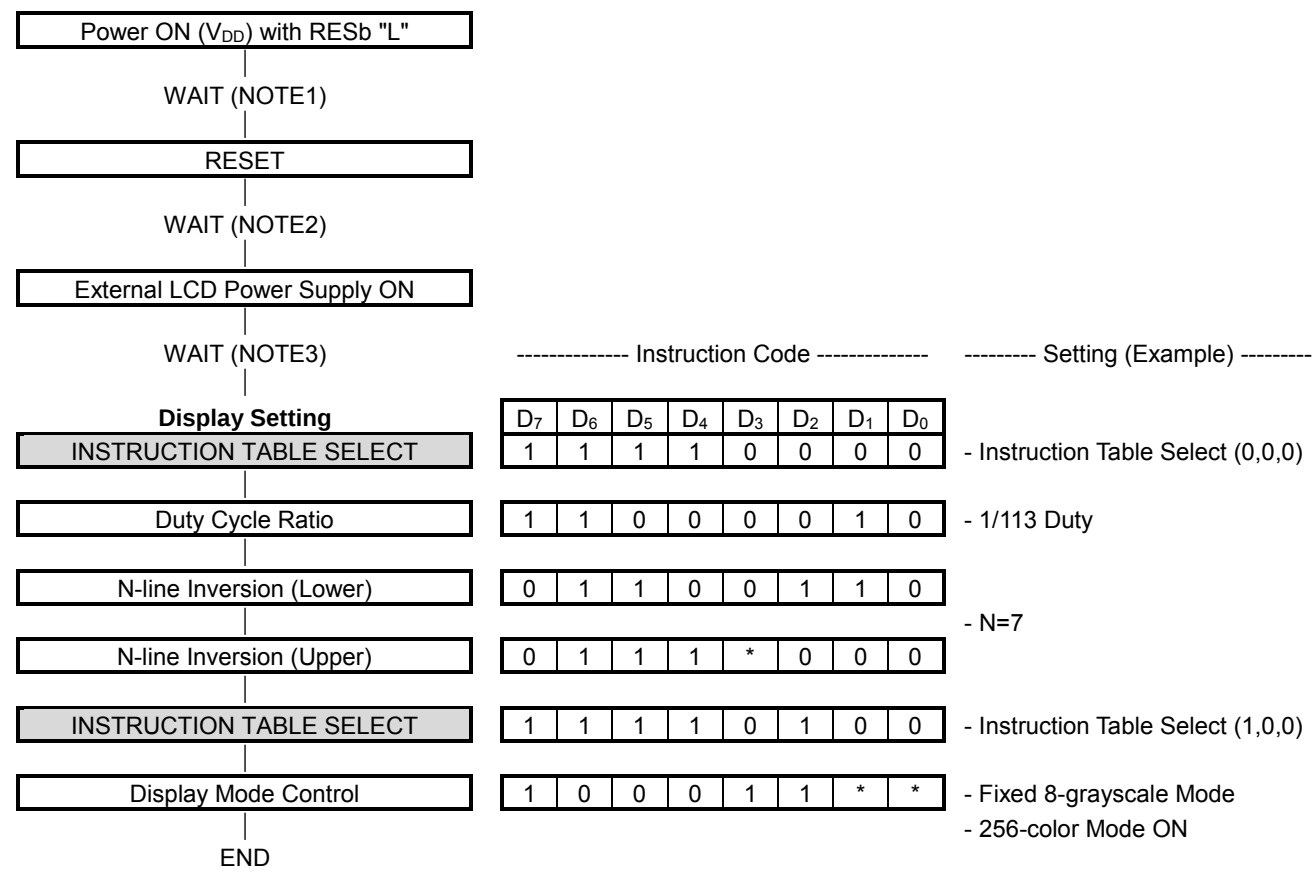
NOTE2) Wait until the V_{DD} and V_{EE} are stabilized.

NOTE3) Wait 10 [μ s] or more.

NOTE4) Wait until the V_{OUT} is stabilized.

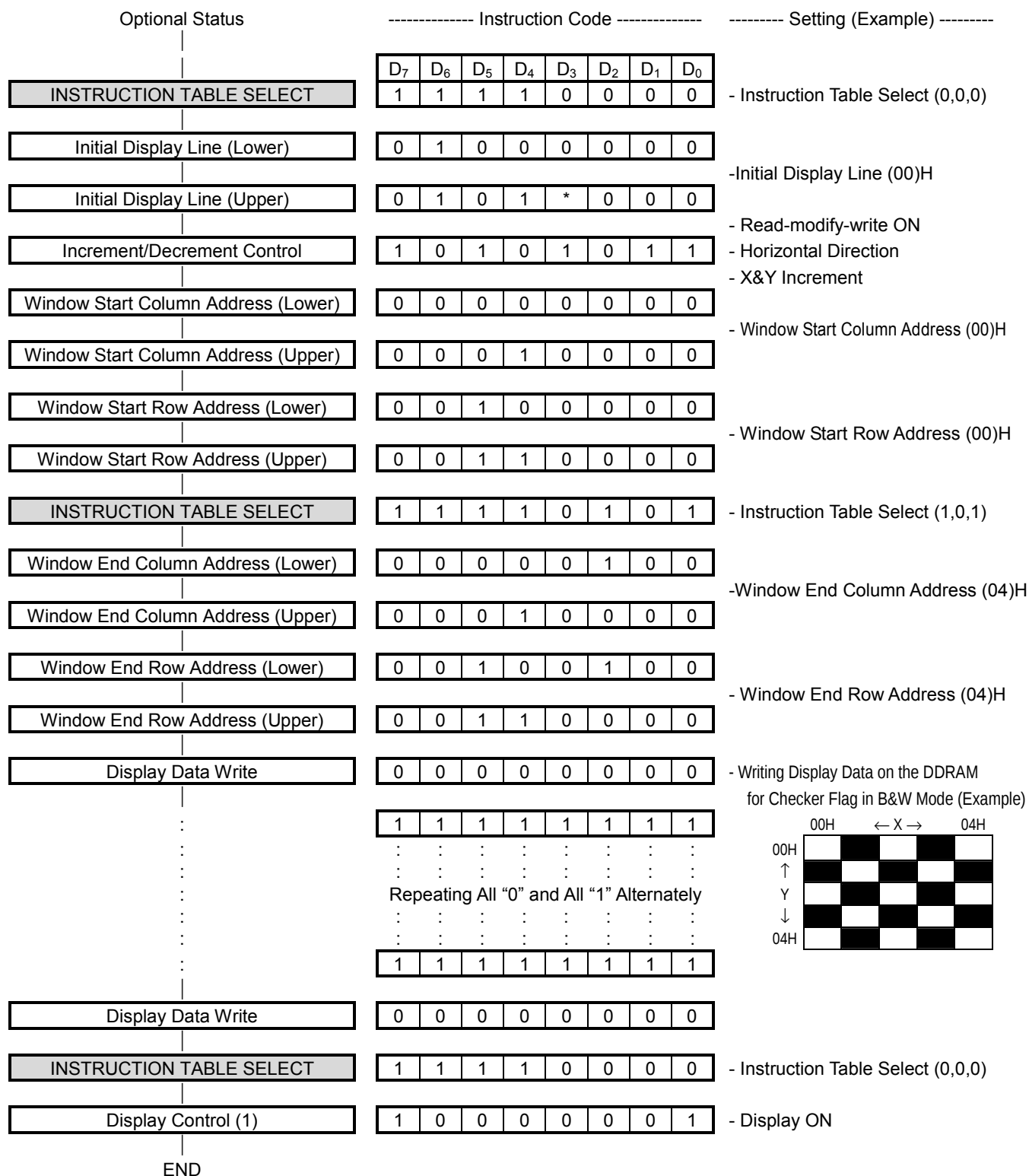
NOTE5) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(19-2) Initialization Sequence in Using External LCD Power Supply

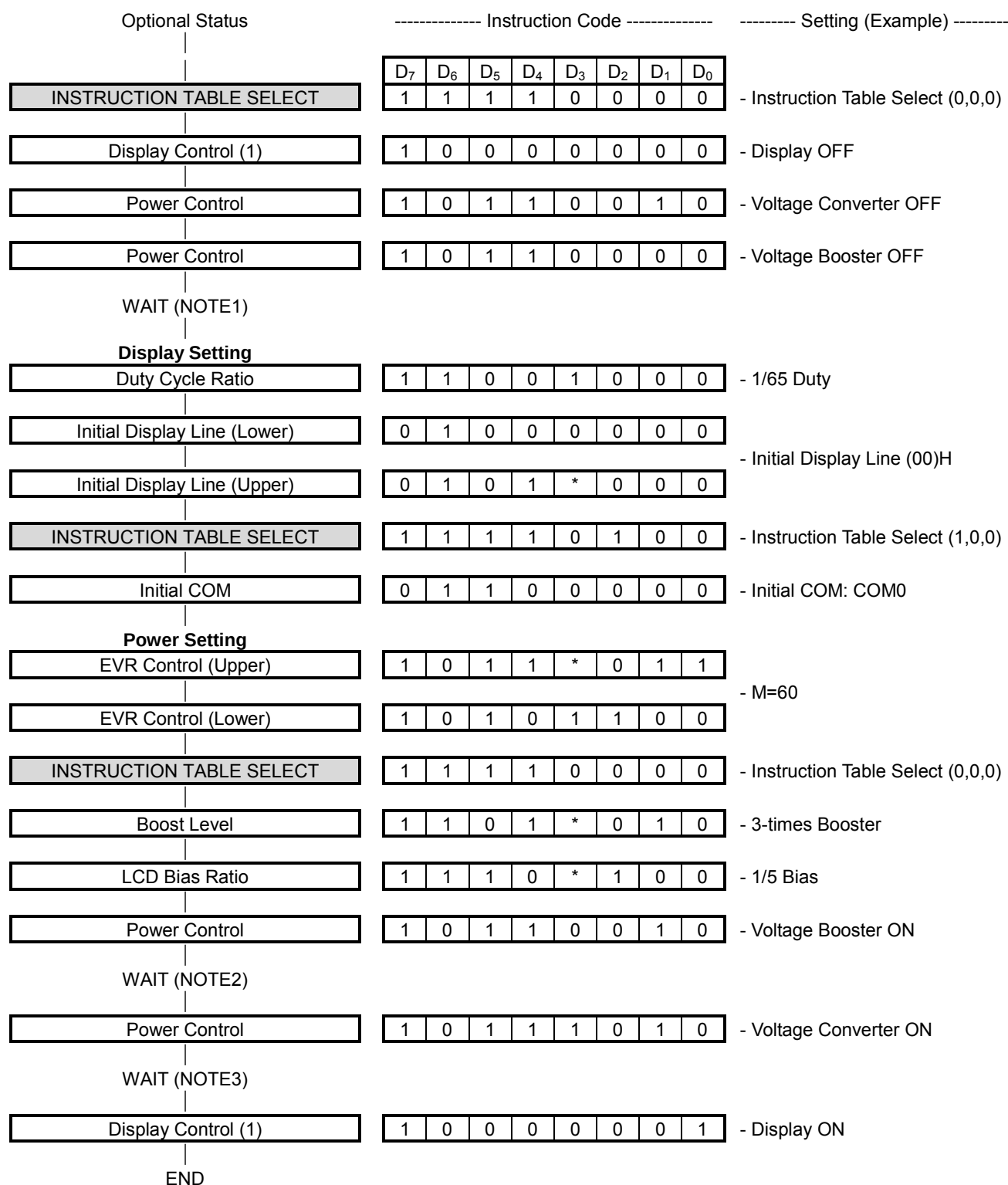


NOTE1) Wait until the V_{DD} is stabilized.
NOTE2) Wait 10 [us] or more.
NOTE3) Wait until the external LCD power supply (V_{OUT} , V_{LCD} , V_1 - V_4) are stabilized.

(19-3) Display Data Write Sequence



(19-4) Partial Display Sequence

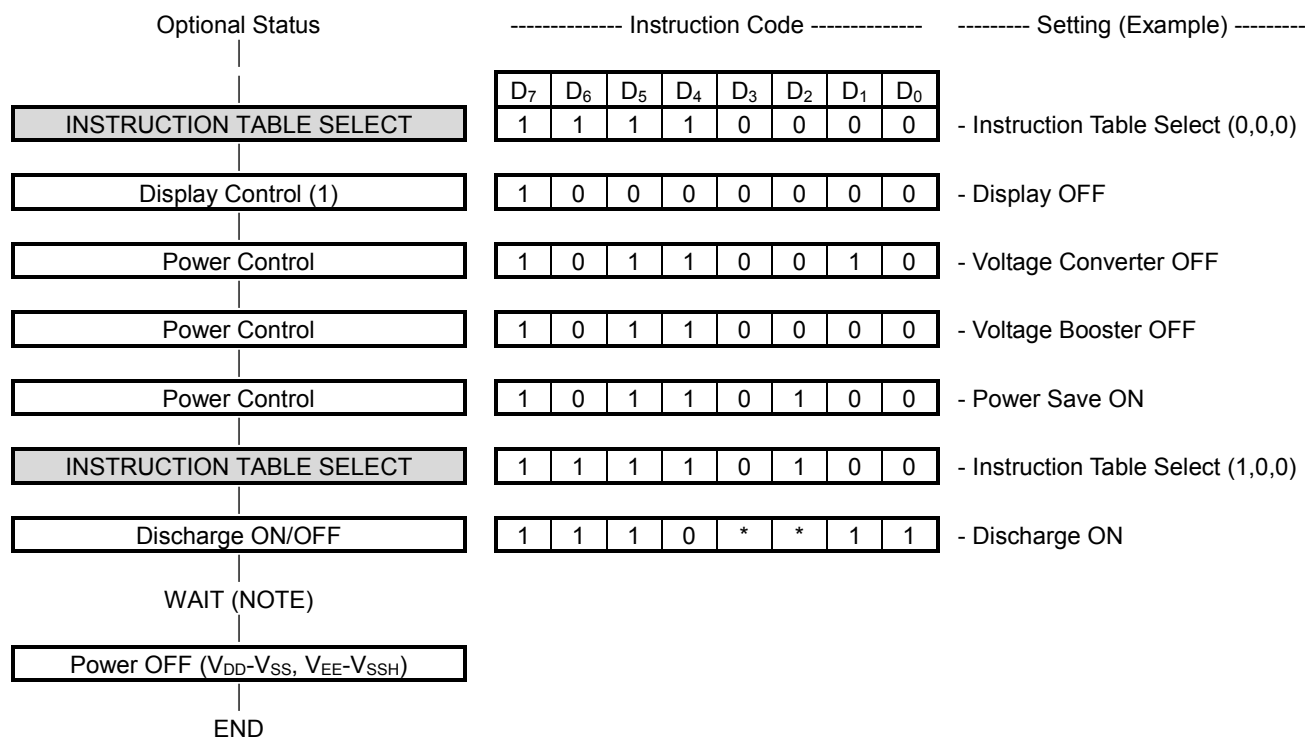


NOTE1) Wait until the voltage booster is completely turned off. Make sure what is the wait time in the particular application.

NOTE2) Wait until the V_{OUT} is stabilized.

NOTE3) Wait until the V_{LCD} and V_1 - V_4 are stabilized.

(19-5) Power OFF Sequence



NOTE) Wait until the Discharge is completed.

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	TERMINAL	RATING	UNIT
Supply Voltage (1)	V_{DD}	$V_{SS}=0V$ $V_{SSH}=0V$ $T_a = +25^{\circ}C$	V_{DD}	-0.3 to +4.0	V
Supply Voltage (2)	V_{EE}		V_{EE}	-0.3 to +4.0	V
Supply Voltage (3)	V_{OUT}		V_{OUT}	-0.3 to +20.0	V
Supply Voltage (4)	V_{REG}		V_{REG}	-0.3 to +20.0	V
Supply Voltage (5)	V_{LCD}		V_{LCD}	-0.3 to +20.0	V
Supply Voltage (6)	V_1, V_2, V_3, V_4		V_1, V_2, V_3, V_4	-0.3 to $V_{LCD} + 0.3$	V
Input Voltage	V_I		*1	-0.3 to $V_{DD} + 0.3$	V
Storage Temperature	T_{stg}			-45 to +125	$^{\circ}C$

NOTE1) D_0 to D_{15} , CSb, RS, RDb, WRb, OSC1, RESb, TEST1, and TEST2

NOTE2) To stabilize the LSI operation, place decoupling capacitors between V_{DD} and V_{SS} and between V_{EE} and V_{SSH} .

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TERMINAL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage	V_{DD1}	V_{DD}	1.7		3.3	V	1
	V_{DD2}		2.4		3.3	V	2
	V_{EE}	V_{EE}	2.4		3.3	V	3
Operating Voltage	V_{LCD}	V_{LCD}	5		18.0	V	4
	V_{OUT}	V_{OUT}			18.0	V	
	V_{REG}	V_{REG}			$V_{OUT} \times 0.9$	V	
	V_{REF}	V_{REF}	2.1		3.3	V	5
Operating Temperature	T_{opr}		-30		85	$^{\circ}C$	

NOTE1) Applied to the condition when the reference voltage generator is not used.

NOTE2) Applied to the condition when the reference voltage generator is used.

NOTE3) Applied to the condition when the voltage booster is used.

NOTE4) The following relation among the LCD bias voltages must be maintained.

$$V_{SSH} < V_4 < V_3 < V_2 < V_1 < V_{LCD} < V_{OUT}$$

NOTE5) Relation: $V_{REF} < V_{EE}$ must be maintained.

■ DC CHARACTERISTICS

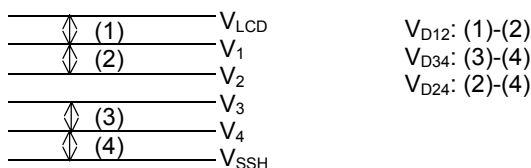
$V_{SS}=0V$, $V_{SSH}=0V$, $V_{DD}=+1.7$ to $+3.3V$, $T_a=-30$ to $+85^{\circ}C$

PARAMETER	SYM BOL	CONDITION	MIN	TYP	MAX	UNIT	NOTE
"H" Level Input Voltage	V_{IH}		$0.8 V_{DD}$		V_{DD}	V	1
"L" Level Input Voltage	V_{IL}		0		$0.2V_{DD}$	V	1
"H" Level Output Voltage	V_{OH1}	$I_{OH} = -0.4mA$	$V_{DD} - 0.4$			V	2
"L" Level Output Voltage	V_{OL1}	$I_{OL} = 0.4mA$			0.4	V	2
"H" Level Output Voltage	V_{OH2}	$I_{OH} = -0.1mA$	$V_{DD} - 0.4$			V	3
"L" Level Output Voltage	V_{OL2}	$I_{OL} = 0.1mA$			0.4	V	3
Input Leakage Current	I_{LI}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	4
Output Leakage Current	I_{LO}	$V_I = V_{SS}$ or V_{DD}	-10		10	μA	5
Driver ON-resistance	R_{ON1}	$ \Delta V_{ON} = 0.5V$ $V_{LCD} = 10V$ $V_{LCD} = 6V$		1 2	2 4	$k\Omega$	6
Stand-by Current	I_{STB}	$CSb = V_{DD}$, $T_a = 25^{\circ}C$ $V_{DD} = 3V$			15	μA	7
Oscillation Frequency Using Internal Resistor	f_{OSC1}	$V_{DD} = 3V$ $T_a = 25^{\circ}C$	490	600	710	kHz	8
	f_{OSC2}		110	135.5	160		9
	f_{OSC3}		15.9	19.4	22.9		10
Oscillation Frequency Using External Resistor	f_{r1}	$R_f = 15k\Omega$		575		kHz	11
	f_{r2}	$R_f = 68k\Omega$		135			
	f_{r3}	$R_f = 510k\Omega$		19.6			
Voltage Booster Output Voltage	V_{OUT}	N-time boost (N=2 to 6) $RL = 500k\Omega$ ($V_{OUT} - V_{SSH}$)	$(N \times V_{EE}) \times 0.95$			V	12
Operating Current (1)	I_{DD1}	$V_{DD} = 3V$, 6-time boost All pixels ON		760	1140	μA	13
Operating Current (2)	I_{DD2}	$V_{DD} = 3V$, 6-time boost Checker flag display		930	1400		
Operating Current (3)	I_{DD3}	$V_{DD} = 3V$, 5-time boost All pixels ON		520	780		
Operating Current (4)	I_{DD4}	$V_{DD} = 3V$, 5-time boost Checker flag display		650	980		
Operating Current (5)	I_{DD5}	$V_{DD} = 3V$, 4-time boost All pixels ON		360	540		
Operating Current (6)	I_{DD6}	$V_{DD} = 3V$, 4-time boost Checker flag display		450	680		
V_{BA} Output Voltage	V_{BA}	$V_{EE} = 2.4$ to $3.3V$	$(0.9 V_{EE}) \times 0.98$	$0.9 V_{EE}$	$(0.9 V_{EE}) \times 1.02$	V	14
V_{REG} Output Voltage	V_{REG}	$V_{EE} = 2.4$ to $3.3V$ $V_{REF} = 0.9 \times V_{EE}$ N-time boost (N=2 to 6)	$(V_{REF} \times N) \times 0.97$	$(V_{REF} \times N)$	$(V_{REF} \times N) \times 1.03$	V	15
LCD Bias Voltages	V_2		-100	0	+100	mV	16
	V_3		-100	0	+100		
	V_{D12}		-30	0	+30		
	V_{D34}		-30	0	+30		
	V_{D24}		-30	0	+30		

■ OSCILLATION FREQUENCY AND FRAME FREQUENCY

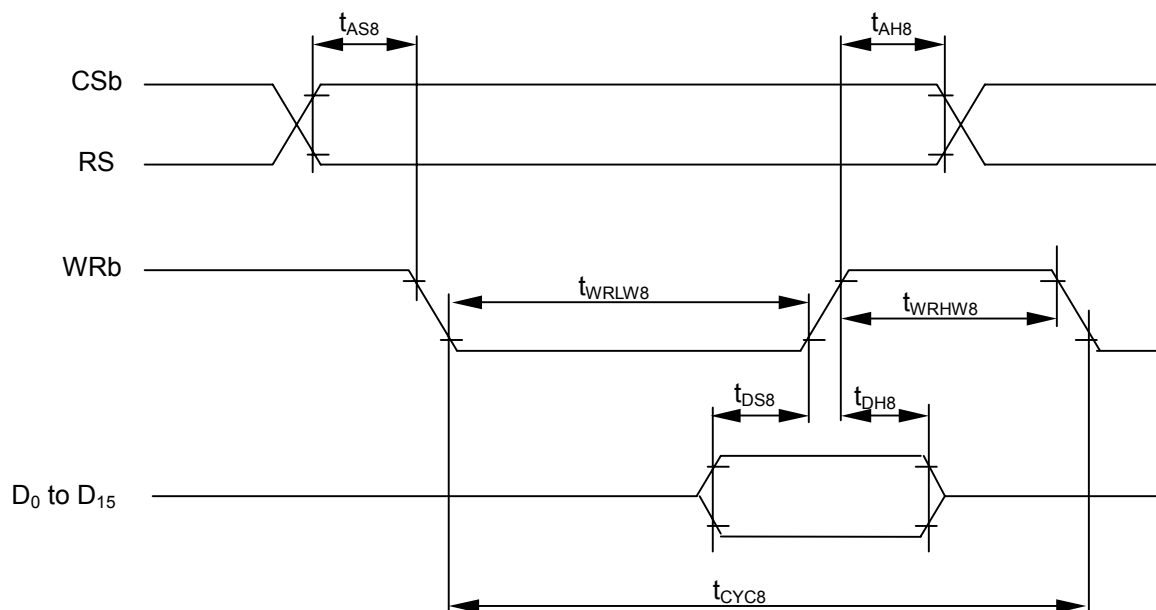
OSCILLATOR /EXTERNAL CLOCK	SYM BOL	DISPLAY MODE	FRAME FREQUENCY (FLM)			
			DUTY CYCLE RATIO (1/D) <DSE=0>			
			1/129 to 1/81	1/73 to 1/41	1/33 to 1/25	1/17
Using Internal Oscillator	f _{OSC1}	Variable 8-/16-level Grayscale Mode	f _{OSC} / (62xD)	f _{OSC} / (62xDx2)	f _{OSC} / (62xDx4)	f _{OSC} / (62xDx8)
	f _{OSC2}	Fixed 8-level Grayscale Mode	f _{OSC} / (14xD)	f _{OSC} / (14xDx2)	f _{OSC} / (14xDx4)	f _{OSC} / (14xDx8)
	f _{OSC3}	B&W Mode	f _{OSC} / (2xD)	f _{OSC} / (2xDx2)	f _{OSC} / (2xDx4)	f _{OSC} / (2xDx8)
Using External Clock	f _{CK1}	Variable 8-/16-level Grayscale Mode	f _{CK} / (62xD)	f _{CK} / (62xDx2)	f _{CK} / (62xDx4)	f _{CK} / (62xDx8)
	f _{CK2}	Fixed 8-level Grayscale Mode	f _{CK} / (14xD)	f _{CK} / (14xDx2)	f _{CK} / (14xDx4)	f _{CK} / (14xDx8)
	f _{CK3}	B&W Mode	f _{CK} / (2xD)	f _{CK} / (2xDx2)	f _{CK} / (2xDx4)	f _{CK} / (2xDx8)

- NOTE1) D_0 - D_{15} , CSb, RS, RDb, WRb, P/S, SEL68 and RESb
- NOTE2) D_0 - D_{15}
- NOTE3) CL, FLM, FR and CLK
- NOTE4) CSb, RS, SEL68, RDb, WRb, P/S, RESb and OSC1
- NOTE5) D_0 - D_{15} in high impedance
- NOTE6) SEGA₀-SEGA₁₂₇, SEGB₀-SEGB₁₂₇, SEGC₀-SEGC₁₂₇, COM₀-COM₁₂₇, SEGSA₀, SEGSA₁, SEGSB₀, SEGSB₁, SEGSC₀ and SEGSC₁
This parameter defines the resistance between each COM/SEG and each LCD bias (V_{LCD} , V_1 , V_2 , V_3 and V_4).
- 0.5V Difference / 1/9 LCD Bias
- NOTE7) V_{DD}
Oscillator is halted.
- CSb=1 (Disabled) / No-load on COM/SEG
- NOTE8) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the Variable grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE9) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the 8-level fixed grayscale mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE10) CLK
This parameter defines the oscillation frequency by using the internal resistor, in the B&W mode.
- (Rf2, Rf1, Rf0)=(0,0,0)
- NOTE11) OSC2
- $V_{DD}=3V$ / $T_a=25^\circ C$
- NOTE12) V_{OUT}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- $V_{EE}=2.4V$ to $3.3V$ / EVR= (1,1,1,1,1,1,1) / 1/5 to 1/12 LCD Bias / 1/129 Duty Cycle / No-load on COM/SEG / RL=500k Ω between V_{OUT} and V_{SSH} / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1"
- NOTE13) V_{SS} , V_{SSH}
This parameter is applied to the condition that the internal LCD power supply and the internal oscillator are used.
- EVR= (1,1,1,1,1,1,1) / All Pixels ON or Checker Flag Display / No-load on COM/SEG / No-access from MPU / $V_{DD}=V_{EE}$ / $V_{REF}=0.9V_{EE}$ / CA1=CA2=1.0uF / CA3=0.1uF / DCON="1" / AMPON="1" / NLIN="0" / 1/129 Duty cycle / $T_a=25^\circ C$
- NOTE14) V_{BA}
- $V_{BA}=V_{REF}$ / Boost Level (N)="1", / DCON="0" / $V_{OUT}=13.5V$
- NOTE15) V_{REG}
- $V_{EE}=2.4V$ to $3.3V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=18V$ / 1/5 to 1/12 LCD bias ratio / 1/129 duty cycle / EVR=(1,1,1,1,1,1,1) / Checker flag display / No-load on COM/SEG / Boost Level (N)="2" to "6" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1" / NLIN="0"
- NOTE16) V_{LCD} , V_1 , V_2 , V_3 and V_4
- $V_{EE}=3.0V$ / $V_{REF}=0.9V_{EE}$ / $V_{OUT}=15V$ / 1/5 to 1/12 LCD Bias / EVR= (1,1,1,1,1,1,1) / Display OFF / No-load on COM/SEG / Boost Level (N)="5" / CA1=CA2=1.0uF / CA3=0.1uF / DCON="0" / AMPON="1"



■ AC CHARACTERISTICS

(1) Write Operation (Parallel Interface / 80-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		90		ns	
Enable "L" level pulse width	t_{WRLW8}		35		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		35		ns	
Data setup time	t_{DS8}		30		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

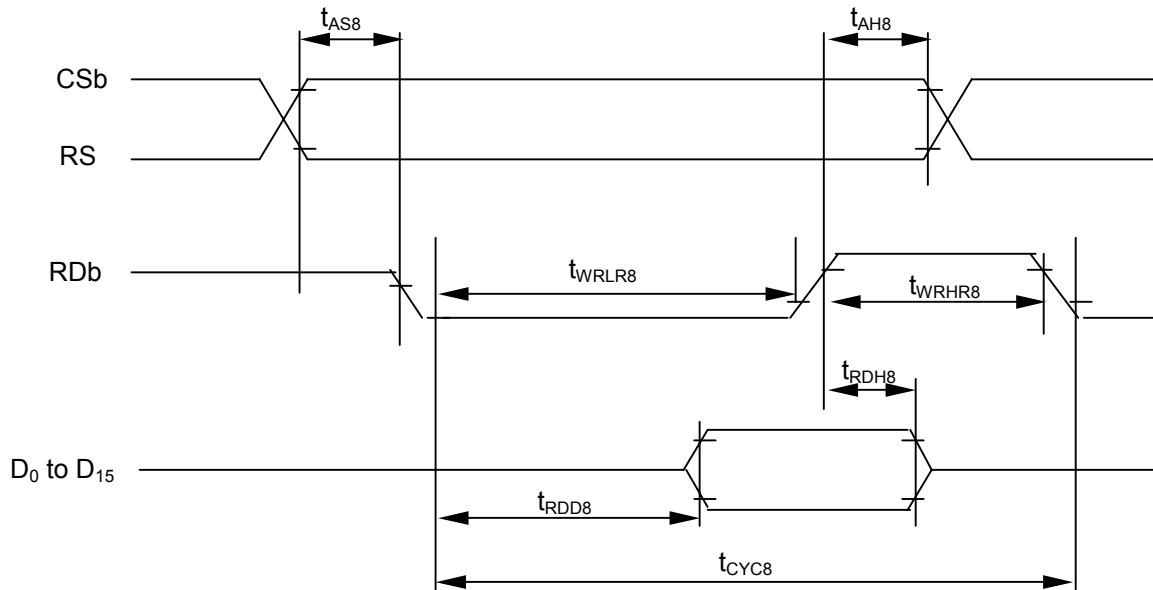
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		160		ns	
Enable "L" level pulse width	t_{WRLW8}		70		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		70		ns	
Data setup time	t_{DS8}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH8}		0		ns	CSb
Address setup time	t_{AS8}		0		ns	RS
System cycle time	t_{CYC8}		180		ns	
Enable "L" level pulse width	t_{WRLW8}		80		ns	WRb
Enable "H" level pulse width	t_{WRHW8}		80		ns	
Data setup time	t_{DS8}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH8}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(2) Read Operation (Parallel Interface / 80-series MPU)



(V_{DD}=2.5 to 3.3V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSb
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		180		ns	RDb
Enable "L" level pulse width	t _{WRLR8}		80		ns	
Enable "H" level pulse width	t _{WRHR8}		80		ns	
Read Data delay time	t _{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH8}		0		ns	

(V_{DD}=2.2 to 2.5V, Ta=-30 to +85°C)

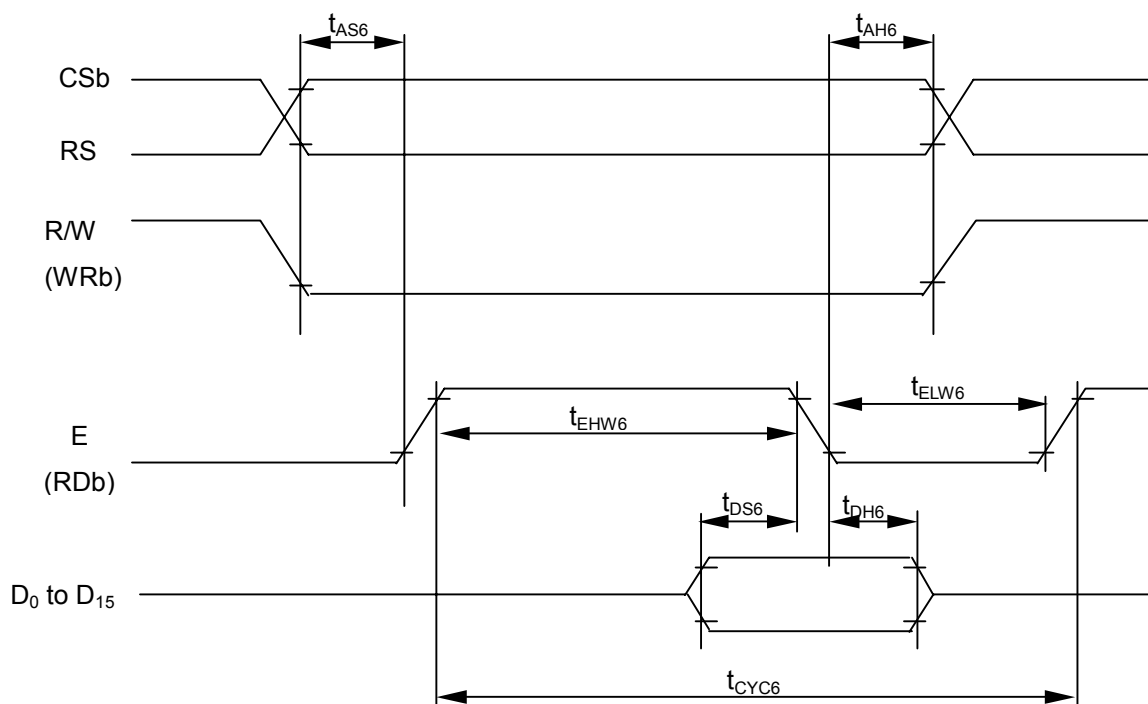
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSb
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		180		ns	RDb
Enable "L" level pulse width	t _{WRLR8}		80		ns	
Enable "H" level pulse width	t _{WRHR8}		80		ns	
Read Data delay time	t _{RDD8}	CL=15pF	0	60	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH8}		0		ns	

(V_{DD}=1.7 to 2.2V, Ta=-30 to +85°C)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t _{AH8}		0		ns	CSb
Address setup time	t _{AS8}		0		ns	RS
System cycle time	t _{CYC8}		250		ns	RDb
Enable "L" level pulse width	t _{WRLR8}		120		ns	
Enable "H" level pulse width	t _{WRHR8}		120		ns	
Read Data delay time	t _{RDD8}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t _{RDH8}		0		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD}.

(3) Write Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		90		ns	E
Enable "L" level pulse width	t_{ELW6}		35		ns	
Enable "H" level pulse width	t_{EHW6}		35		ns	
Data setup time	t_{DS6}		40		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

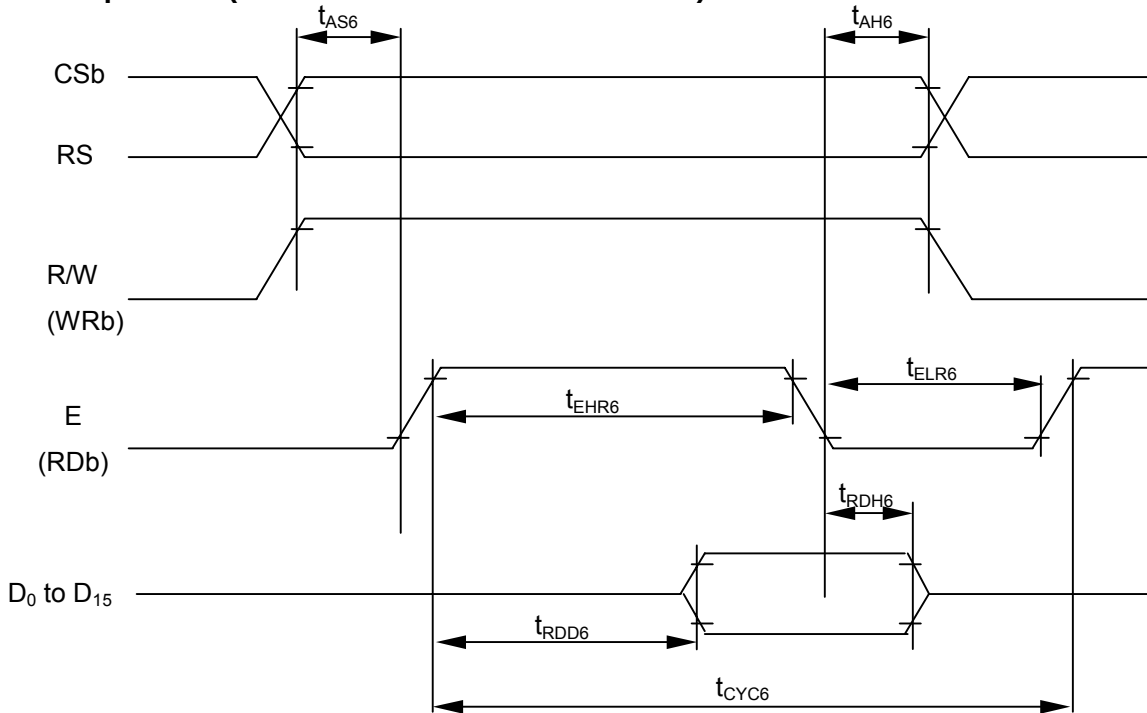
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		160		ns	E
Enable "L" level pulse width	t_{ELW6}		70		ns	
Enable "H" level pulse width	t_{EHW6}		70		ns	
Data setup time	t_{DS6}		50		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		5		ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELW6}		80		ns	
Enable "H" level pulse width	t_{EHW6}		80		ns	
Data setup time	t_{DS6}		70		ns	D ₀ to D ₁₅
Data hold time	t_{DH6}		10		ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(4) Read Operation (Parallel Interface / 68-series MPU)



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

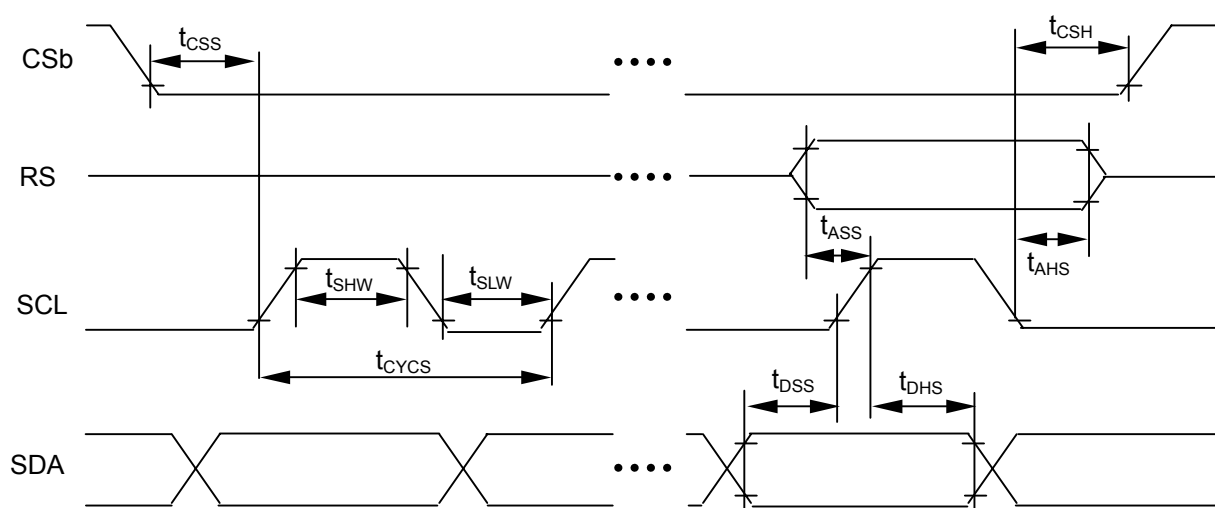
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		180		ns	E
Enable "L" level pulse width	t_{ELR6}		80		ns	
Enable "H" level pulse width	t_{EHR6}		80		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	70	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Address hold time	t_{AH6}		0		ns	CSb
Address setup time	t_{AS6}		0		ns	RS
System cycle time	t_{CYC6}		250		ns	E
Enable "L" level pulse width	t_{ELR6}		120		ns	
Enable "H" level pulse width	t_{EHR6}		120		ns	
Read Data delay time	t_{RDD6}	CL=15pF	0	110	ns	D ₀ to D ₁₅
Read Data hold time	t_{RDH6}				ns	

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(5) Serial Interface



($V_{DD}=2.5$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		100		ns	SCL
SCL "H" level pulse width	t_{SHW}		45		ns	SCL
SCL "L" level pulse width	t_{SLW}		45		ns	SCL
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	RS
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	SDA
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	CSb

($V_{DD}=2.2$ to $2.5V$, $T_a=-30$ to $+85^{\circ}C$)

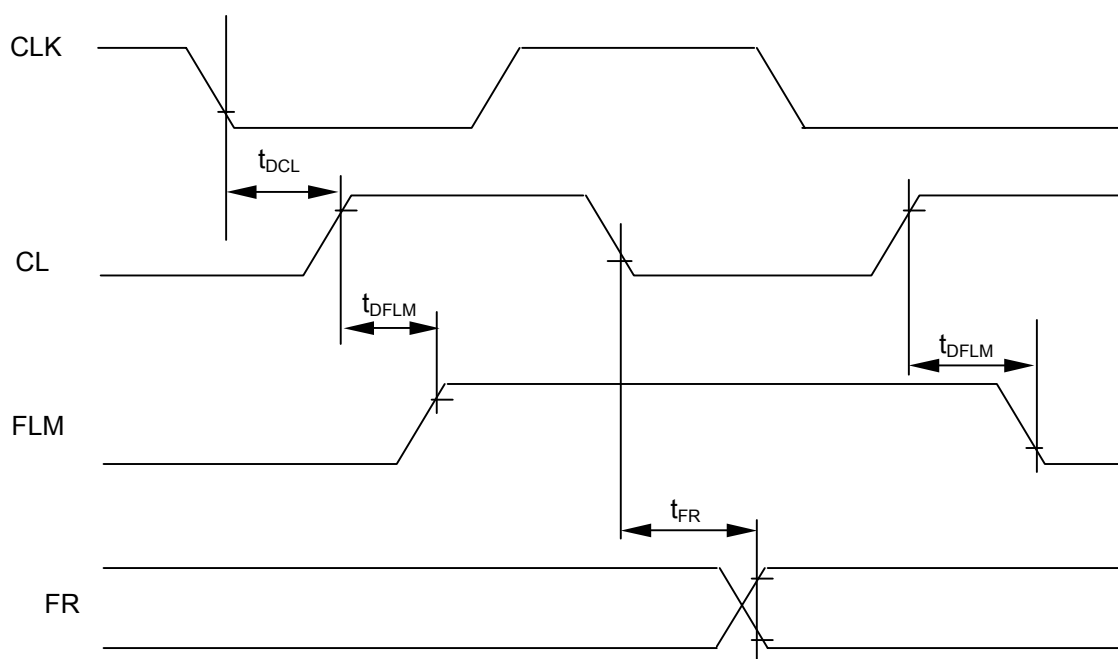
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		100		ns	SCL
SCL "H" level pulse width	t_{SHW}		45		ns	SCL
SCL "L" level pulse width	t_{SLW}		45		ns	SCL
Address setup time	t_{ASS}		20		ns	RS
Address hold time	t_{AHS}		20		ns	RS
Data setup time	t_{DSS}		20		ns	SDA
Data hold time	t_{DHS}		20		ns	SDA
CSb – SCL time	t_{CSS}		20		ns	CSb
CSb hold time	t_{CSH}		20		ns	CSb

($V_{DD}=1.7$ to $2.2V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
Serial clock cycle	t_{CYCS}		160		ns	SCL
SCL "H" level pulse width	t_{SHW}		75		ns	SCL
SCL "L" level pulse width	t_{SLW}		75		ns	SCL
Address setup time	t_{ASS}		35		ns	RS
Address hold time	t_{AHS}		35		ns	RS
Data setup time	t_{DSS}		35		ns	SDA
Data hold time	t_{DHS}		35		ns	SDA
CSb – SCL time	t_{CSS}		35		ns	CSb
CSb hold time	t_{CSH}		35		ns	CSb

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(6) Display Control Timing



Output timing

($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	500	ns	FLM
FR delay time	t_{FR}		0	500	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

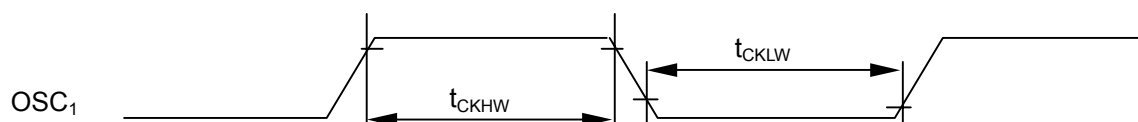
Output timing

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
FLM delay time	t_{DCLM}	CL=15pF	0	1000	ns	FLM
FR delay time	t_{FR}		0	1000	ns	FR
CL delay time	t_{DCL}		0	200	ns	CL

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

(7) Input Clock Timing



($V_{DD}=1.7$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	TERMINAL
OSC1 "H" level pulse width (1)	t_{CKHW1}		0.70	1.02	μs	OSC1 (NOTE2)
OSC1 "L" level pulse width (1)	t_{CKLW1}		0.70	1.02	μs	
OSC1 "H" level pulse width (2)	t_{CKHW2}		3.13	4.55	μs	OSC1 (NOTE3)
OSC1 "L" level pulse width (2)	t_{CKLW2}		3.13	4.55	μs	
OSC1 "H" level pulse width (3)	t_{CKHW3}		21.8	31.4	μs	OSC1 (NOTE4)
OSC1 "L" level pulse width (3)	t_{CKLW3}		21.8	31.4	μs	

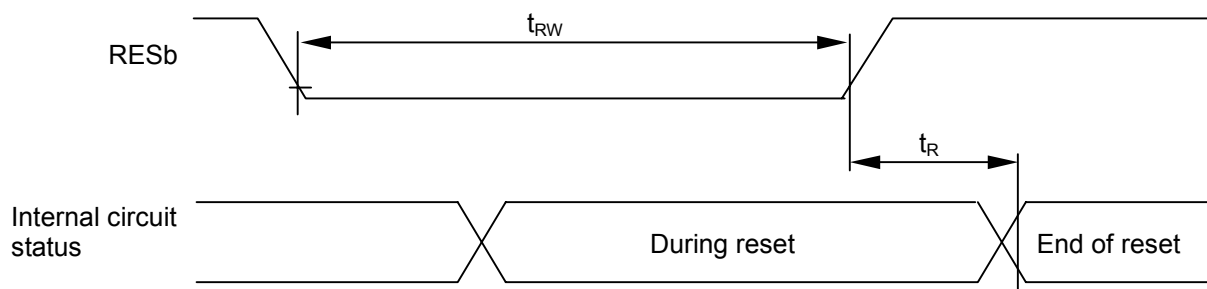
NOTE1) Each timing is specified based on 20% and 80% of V_{DD} .

NOTE2) Applied to Variable 8-/16-level grayscale mode (MON="0", PWM="0")

NOTE3) Applied to fixed 8-level grayscale mode (MON="0", PWM="1")

NOTE4) Applied to B&W mode (MON="1")

(8) Reset Input Timing



($V_{DD}=2.4$ to $3.3V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.0	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

($V_{DD}=1.7$ to $2.4V$, $T_a=-30$ to $+85^{\circ}C$)

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT	Terminal
Reset time	t_R			1.5	μs	
RESb "L" level pulse width	t_{RW}		10.0		μs	RESb

NOTE) Each timing is specified based on 20% and 80% of V_{DD} .

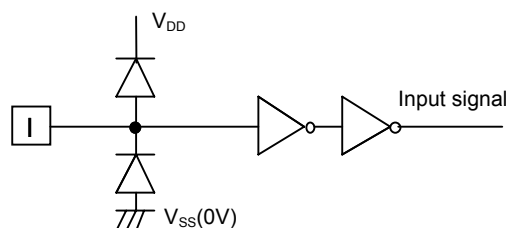
(9) Delay Time of Gate

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Delay time of gate	$T_a=+25^{\circ}C$, $V_{SS}=0V$, $V_{DD}=3.0V$		10		ns

INPUT/OUTPUT BLOCK DIAGRAMS

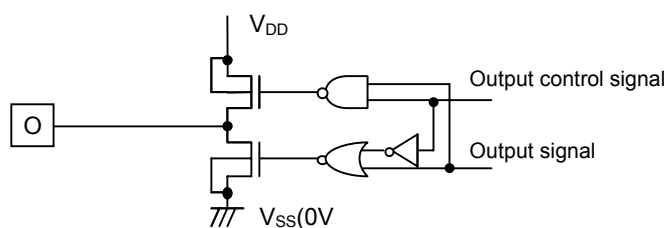
Input Block Diagram

Terminals CSb, RS, RDb, WRb, SEL68, P/S, RESb



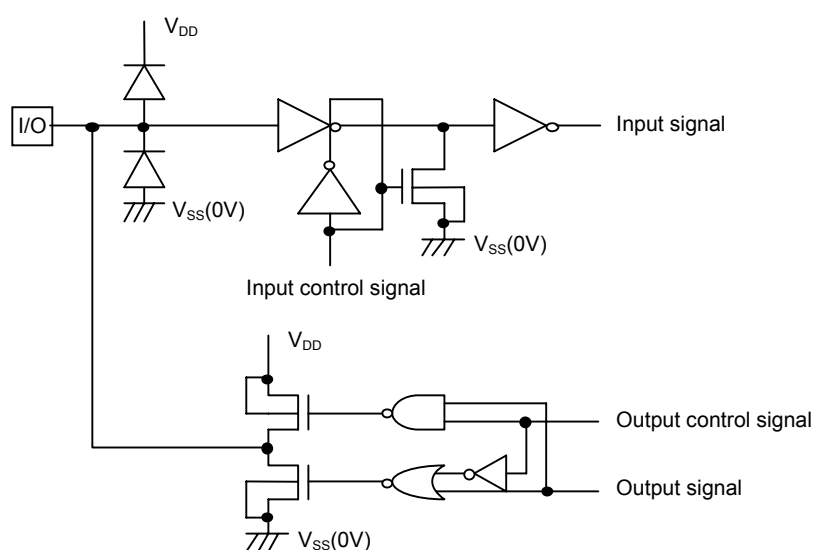
Output Block Diagram

Terminals : FLM, CL, FR, CLK



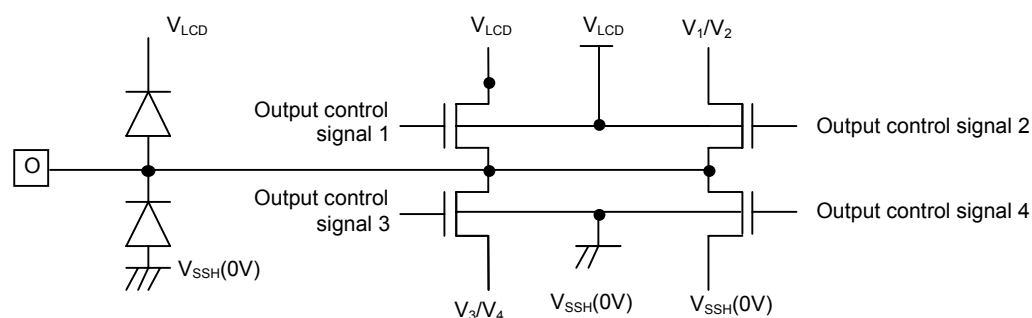
Input/Output Block Diagram

Terminals : D₀ - D₁₅



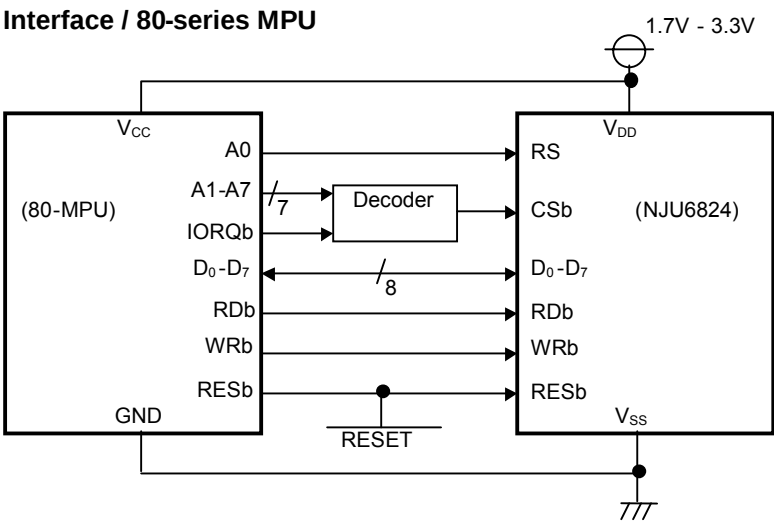
COM/SEG Driver Block Diagram

Terminals : SEGA₀/B₀/C₀ - SEGA₁₂₇/B₁₂₇/C₁₂₇, COM₀ - COM₁₂₇

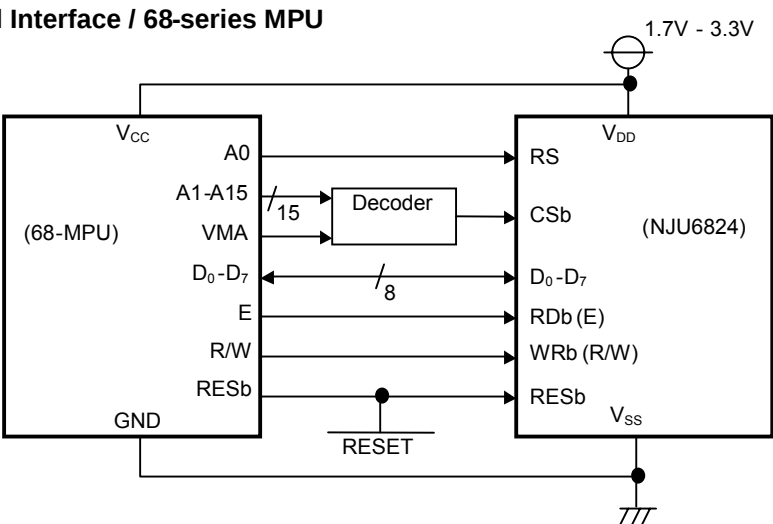


■ MPU CONNECTIONS

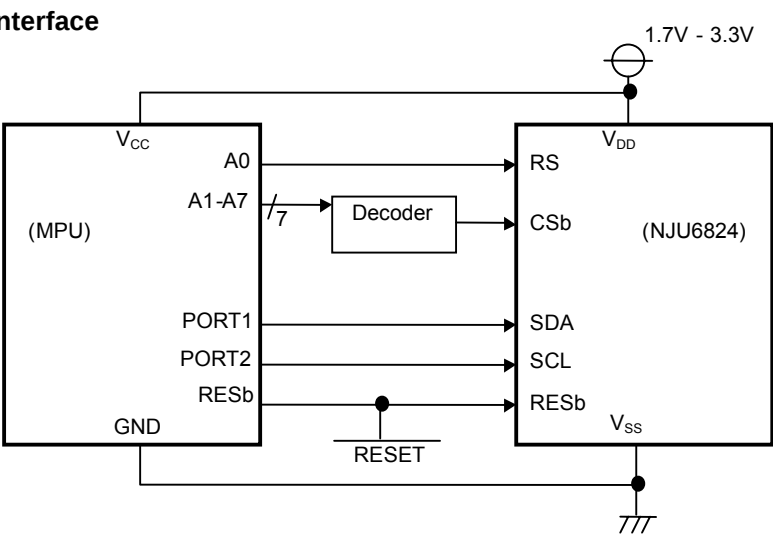
Parallel Interface / 80-series MPU



Parallel Interface / 68-series MPU



Serial Interface



[CAUTION]
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