National Semiconductor

MILITARY DATA SHEET

MNNSC800-4-X REV 0A0

Original Creation Date: 12/05/94
Last Update Date: 12/05/94
Last Major Revision Date: 12/05/94

8 BIT MICROPROCESSOR (P2 CMOS) 4MHz

General Description

The NSC800 is an 8-bit CMOS microprocessor that functions as the central processing unit (CPU) in National Semiconductor's NSC800 microcomputer family. National's microCMOS technology used to fabricate this device provides system designers with performance equivalent to comparable NMOS products, but with the low power advantage of CMOS. Some of the many system functions incorporated on the device are vectored priority interrupts, refresh control, power-save feature and interrupt acknowledge. The NSC800 is available in dual-in-line and surface mounted chip carrier packages.

The system designer can choose not only from the dedicated CMOS peripherals that allow direct interfacing to the NSC800 but from the full line of National's CMOS products to allow a low-power system solution. The dedicated peripheral is the NSC810A RAM I/O Timer.

All devices are available in military temperature range in accordance with Method 5004 of MIL-STD-883.

Industry Part Number

NSC800-4

NS Part Numbers

NSC800TD-4-MIL
NSC800TE-4-MIL

Prime Die

MM47644, NT800

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+90
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+90
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+90
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+90
11	Switching tests at	-55

Features

- Fully compatible with Z80 (R) instruction set:
  Powerful set of 158 instructions
  10 addressing modes
  22 internal registers
- Low power: 50 mW at 5V Vcc
- Unique power-save feature
- Multiplexed bus structure
- Schmitt trigger input on reset
- On-chip bus controller and clock gernerator
- On-chip 8-bit dynamic RAM refresh circuitry
- Speed: 1.0 uS instruction cycle at 4.0 MHz
  NSC800-4 4.0MHz
  NSC800-35 3.5MHz
  NSC800 2.5MHz
- Capable of addressing 64k bytes of memory and 256 I/O devices
- Five interruptrequest lines on-chip

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Voltage on Any Pin WRT Ground	-0.3V to Vcc +0.3V
Maximum Vcc	7V
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300 C

Note 1: Absolute Maximum Ratings indicate limits beyond which permanent damage may occur. Continuous operations at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

Recommended Operating Conditions

Ta	-55 C to +90 C

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vcc = 5V ±10%, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vih	Logical "1" Input Voltage		1, 2		.8Vcc	Vcc	V	1, 2, 3
Vil	Logical "0" Input Voltage		1, 2		0	.2Vcc	V	1, 2, 3
VHY	Hysteresis at Reset IN	Vcc = 5V	2		.25		V	1, 2, 3
Voh1	Logical "1" Output Voltage	IOUT = -1mA	1		2.4		V	1, 2, 3
Voh2	Logical "1" Output Voltage	IOUT = -10uA	1		Vcc-.5		V	1, 2, 3
Vol1	Logical "0" Output Voltage	IOUT = 2mA	1		0	.4	V	1, 2, 3
Vol2	Logical "0" Output Voltage	IOUT = 10uA	1		0	.1	V	1, 2, 3
IIL	Input Leakage Current	0 <= Vin <= Vcc	1		-10	10	uA	1, 2, 3
IOL	Output Leakage Current	0 <= Vin <= Vcc	1		-10	10	uA	1, 2, 3
ICCA	Active Supply Current	IOUT = 0, (XIN) = 8MHz	1			21	mA	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%, GND = 0V

tX	Period at XIN and XOUT		1, 2, 3		125	3333	nS	9, 10, 11
T	Period at Clock Output		1, 2, 3		250	6667	nS	9, 10, 11
tR	Clock Rise Time	Measured from 10% - 90%	1, 3			80	nS	9, 10, 11
tF	Clock Fall Time	Measured from 10% - 90%	1, 3			50	nS	9, 10, 11
tL	Clock Low Time	50% duty cycle, square wave input on XIN	1, 3		80		nS	9, 10, 11
tH	Clock High Time	50% duty cycle, square wave input on XIN	1, 3		75		nS	9, 10, 11
tACC(OP)	ALE to Valid Data Opcode Fetch	Add t for each WAIT STATE	1, 3			300	nS	9, 10, 11
tACC(MR)	ALE to Valid Data Memory Read	Add t for each WAIT STATE	1, 3			360	nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tAFR	AD (0-7) Float After $\overline{RD}$ Falling		2			0	nS	9, 10, 11
tBABE	$\overline{BACK}$ Rising to BUS Enable		2			250	nS	9, 10, 11
tBABF	$\overline{BACK}$ Falling to BUS Float		2			50	nS	9, 10, 11
tBACL	$\overline{BACK}$ Falling to Clock Falling		1, 3		55		nS	9, 10, 11
tBRH	$\overline{BREQ}$ Hold Time		2		0		nS	9, 10, 11
tBRS	$\overline{BREQ}$ Set-Up Time		1, 3		45		nS	9, 10, 11
tCAF	Clock Falling to ALE Falling		1, 3		0	55	nS	9, 10, 11
tCAR	Clock Rising to ALE Falling		1, 3		0	80	nS	9, 10, 11
tCRD	Clock Rising to Read Rising		1, 3			80	nS	9, 10, 11
tCRF	Clock Rising to Refresh Falling		1, 3			65	nS	9, 10, 11
tDAI	ALE Falling to $\overline{INTA}$ Falling		1, 3		85		nS	9, 10, 11
tDAR	ALE Falling to $\overline{RD}$ Falling		1, 3		90	160	nS	9, 10, 11
tDAW	ALE Falling to $\overline{WR}$ Falling		1, 3		200	265	nS	9, 10, 11
tD (BACK)1	ALE Falling to $\overline{BACK}$ Falling	Add t for each $\overline{WAIT}$ state; Add t for opcode fetch cycles	1, 3		560		nS	9, 10, 11
tD (BACK)2	$\overline{BREQ}$ Rising to $\overline{BACK}$ Rising		1, 3		125	475	nS	9, 10, 11
tD(1)	ALE Falling to $\overline{INTR}$, $\overline{NMI}$, $\overline{RSTA-C}$, $\overline{PS}$, $\overline{BREQ}$, Inputs Valid	Add t for each $\overline{WAIT}$ state; Add t for opcode fetch cycles	1, 3			250	nS	9, 10, 11
tDPA	Rising $\overline{PS}$ to Falling ALE		1, 3		125	510	nS	9, 10, 11
tD(WAIT)	ALE Falling to $\overline{WAIT}$ Input Valid		1, 3			125	nS	9, 10, 11
tH(ADH)1	A(8-15) Hold Time During opcode fetch		2		0		nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tH(ADH)2	A(8-15) Hold Time During Memory or IO, $\overline{RD}$ and $\overline{WR}$		2		60		nS	9, 10, 11
tH(ADL)	AD(0-7) Hold Time		2		30		nS	9, 10, 11
tH(WD)	Write Data Hold Time		1, 3		75		nS	9, 10, 11
tINH	Interrupt Hold Time		2		0		nS	9, 10, 11
tINS	Interrupt Set-Up Time		1, 3		45		nS	9, 10, 11
tNMI	Width of NMI Input		2		20		nS	9, 10, 11
tRDH	Data Hold After Read		2		0		nS	9, 10, 11
tRFLF	$\overline{RFSH}$ Rising to ALE Falling		1, 3		40		nS	9, 10, 11
tRL(MR)	$\overline{RD}$ Rising to ALE Rising (Memory Read)		1, 3		45		nS	9, 10, 11
tS(AD)	AD(0-7) Set-Up Time		1, 3		40		nS	9, 10, 11
tS(ALE)	A(8-15), S0, S1, IO/M Set-Up Time		1, 3		50		nS	9, 10, 11
tS(WD)	Write Data Set-Up Time		1, 3		30		nS	9, 10, 11
tW(ALE)	ALE Width		1, 3		100		nS	9, 10, 11
tWH	WAIT Hold Time		2		0		nS	9, 10, 11
tW(1)	Width of $\overline{INTR}$, $\overline{RSTA-C}$, $\overline{PS}$, $\overline{BREQ}$		1, 3		125		nS	9, 10, 11
tW(INTA)	$\overline{INTA}$ Strobe Width	Add two T states for first $\overline{INTA}$ of each interrupt response string; Add T for each $\overline{WAIT}$ state	1, 3		200		nS	9, 10, 11
tWL	$\overline{WR}$ Rising to ALE Rising		1, 3		70		nS	9, 10, 11
tW(RD)	Read Strobe Width during opcode fetch	ADD t for each $\overline{WAIT}$ state; ADD t/2 for Memory Read cycles	1, 3		185		nS	9, 10, 11
tW(RFSH)	Refresh Strobe Width		1, 3		395		nS	9, 10, 11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: Vcc = 5V ±10%, GND = 0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tWS	$\overline{WAIT}$ Set-Up Time		1, 3		55		nS	9, 10, 11
tW(WAIT)	$\overline{WAIT}$ Input Width		1, 3		175		nS	9, 10, 11
tW(WR)	Write Strobe Width	Add t for each $\overline{WAIT}$ state	1, 3		220		nS	9, 10, 11
tXCF	XIN to Clock Falling		1, 3		5	80	nS	9, 10, 11
tXCR	XIN to Clock Rising		1, 3		5	80	nS	9, 10, 11

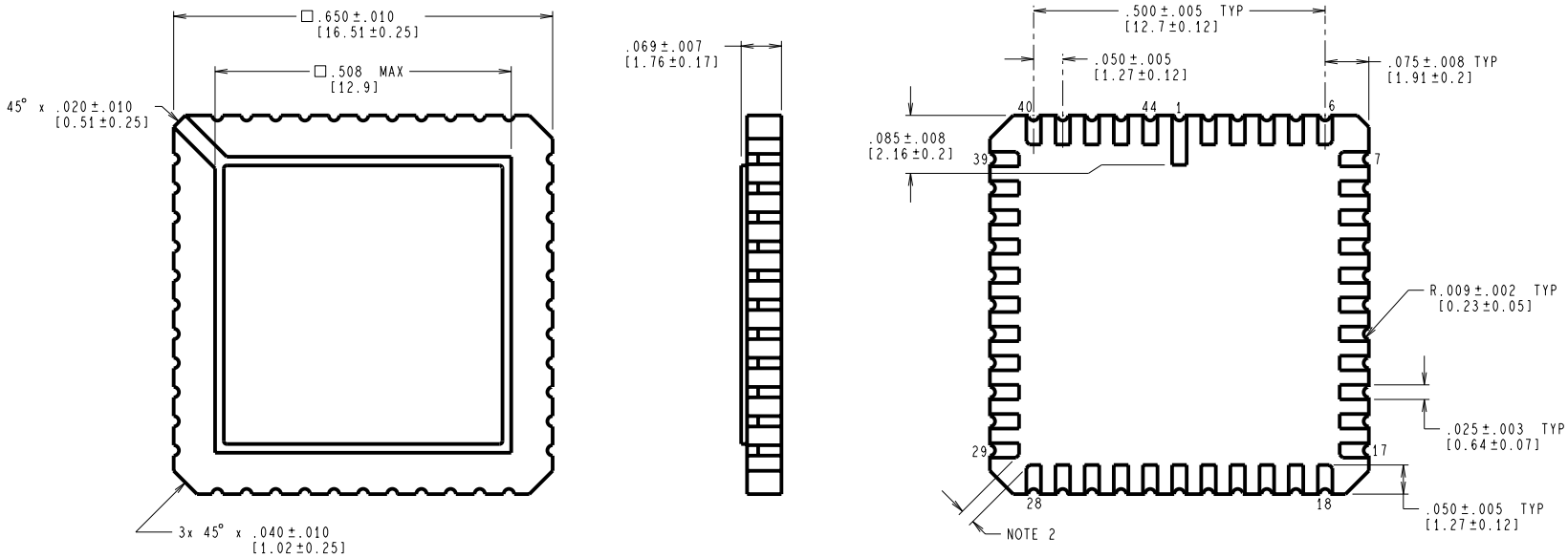
Note 1: Parameter tested go-no-go only.
Note 2: Guaranteed by design.
Note 3: Test conditions: T = 250ns.

Graphics and Diagrams

GRAPHICS#	DESCRIPTION
5240HRC1	DIP, SIDEBRAZED CERAMIC, 40 LEAD (B/I CKT)
5241HRC1	LDLESS CHIP CARRIER, TYPE C, 44LD (B/I CKT)
D40CRL	DIP, S/B CERAMIC, 40LD (P/P DWG)
E44ARF	LDLESS CHIP CARRIER,TYPE C,44TERMINAL(P/P DWG)
P000011A	DIP, S/BRAZED CERAMIC, 40LD (PIN OUT)
P000012A	LDLESS CHIP CARRIER, TYPE C, 44LD (PIN OUT)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
F	REVISE AND REDRAW PER NEW STANDARD.	10006	02/17/94	DEG/



CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS

NOTES: UNLESS OTHERWISE SPECIFIED.

1. LEAD FINISH TO BE ONE OF THE FOLLOWING:

   a. 50 MICROINCHES/1.27 MICROMETERS MINIMUM GOLD PLATING OVER 50-350 MICROINCHES/1.27-8.89 MICROMETERS NICKEL.

   b. SOLDER DIP.
   SOLDER THICKNESS PER LATEST REVISION OF MIL-STD-1835.

2. CORNER PADS MAY HAVE A 45°X.020IN/0.51mm MAXIMUM CHAMFER TO ACCOMPLISH THE .015IN/0.38mm DIMENSION.

4. REFERENCE JEDEC REGISTRATION MS-004, VARIATION CD, DATED 7/90.

MIL/AERO
CONFIGURATION CONTROL

APPROVALS	DATE
DRAWN: Dwayne Grady	02/17/94
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION

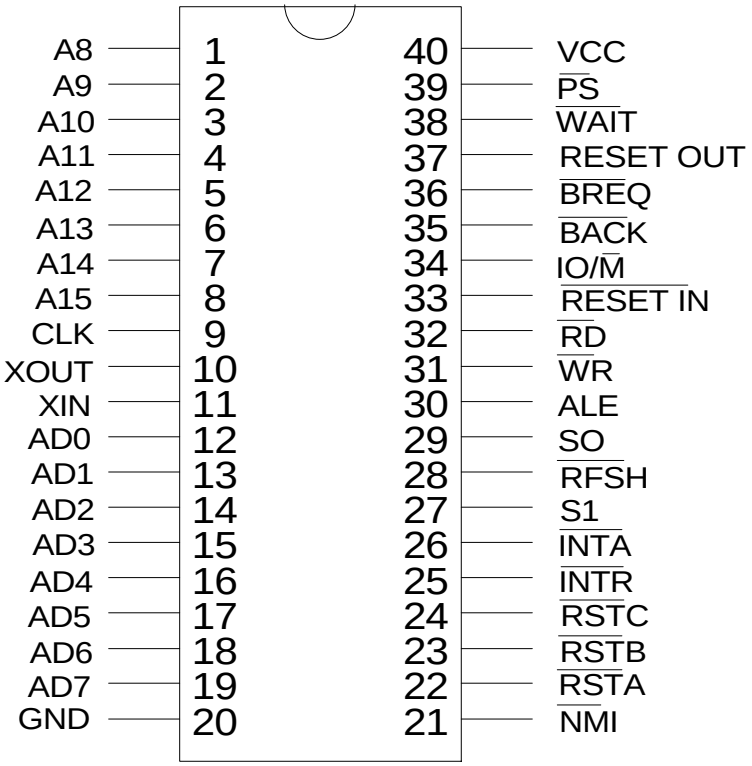
INCH [MM]

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

LEADLESS CHIP CARRIER, TYPE C, 44 TERMINAL

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-E44A	F

DO NOT SCALE DRAWING | SHEET 1 of 1



NSC800D/883, NSC800D-35/883, and NSC800TD-4-MIL

CONNECTION DIAGRAM
40-LEAD DIP
(TOP VIEW)

P000011A