NW1507
Multi-Rate Time Division Switch Matrix

Preliminary, May 2000 (Ver1.1)

Features

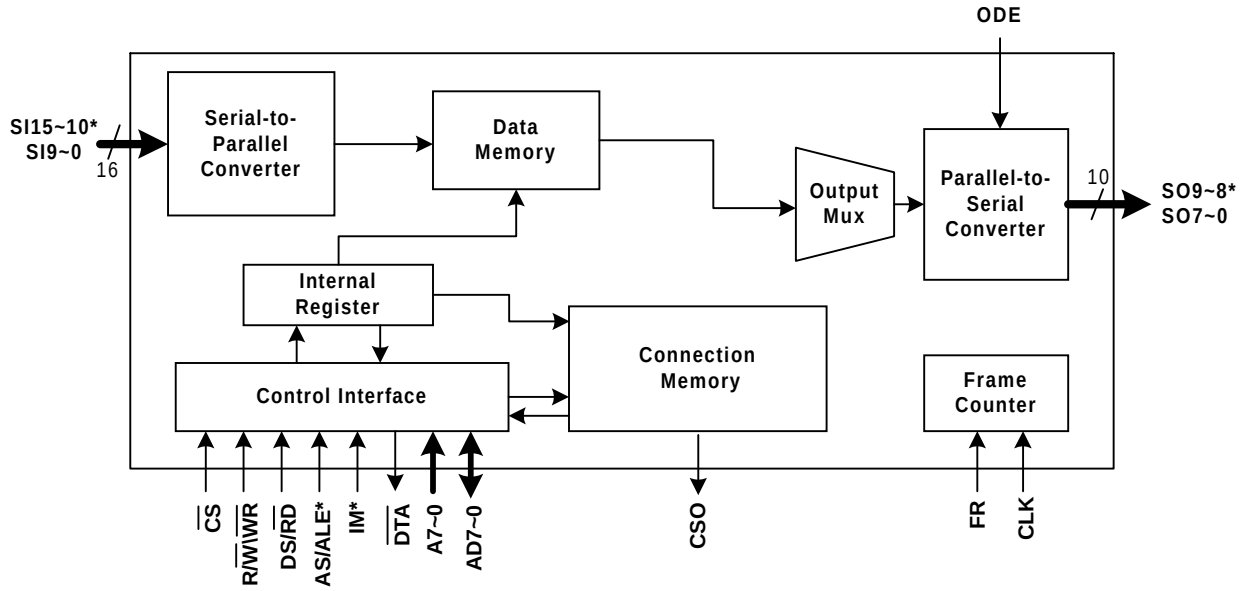
- 256 × 256 non-blocking or 512 × 256 blocking switching
- Support 8-bit or 4-bit channel switching
- Operating at rate of 2.048, 4.096 or 8.192Mbits/s
- Identical & Different I/O data rate selection
- Input frame offset selection
- Per-channel variable/constant throughput delay selection
- Tri-state outputs
- ST-BUS/GCI interfaces identified automatically
- Control port compatible to Motorola/Intel multiplexed buses and Motorola non-multiplexed bus
- +5 V single power supply
- Low power consumption (30 mW Typ.)
- Operating temperature range:
  -40 °C to +85 °C
- Packages available:
  NW1507-XL 44-pin PLCC
  NW1507-XD 40-pin DIP
  (where X is the revision ID)

Description

The NW1507 is a digital switch matrix, providing 256 × 256 non-blocking or 512 × 256 blocking switching configurations. The serial input and output streams may have data rates of 2.048, 4.096 or 8.192Mbits/s with 32, 64 or 128 channels respectively. Variable/constant throughput delay selection is provided on per channel basis to maintain the data sequence integrity during the non-blocking switching. In addition, the control interface of the NW1507, compatible with Motorola/ Intel CPUs, provides read and write access to internal registers and memories. The NW1507 can also be used for switching 32Kbits/s channels in ADPCM application.

Applications

The NW1507 device can be used for the switching of digitized data, voice and video in applications as: Central Office Switch, Private Branch Exchange (PBX), Wireless Base Station, Access Networks, ISDN, Voice/Data multiplexer and voice card.



* 44 pin package only

Figrue-1. Block Diagram

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Pin Connection

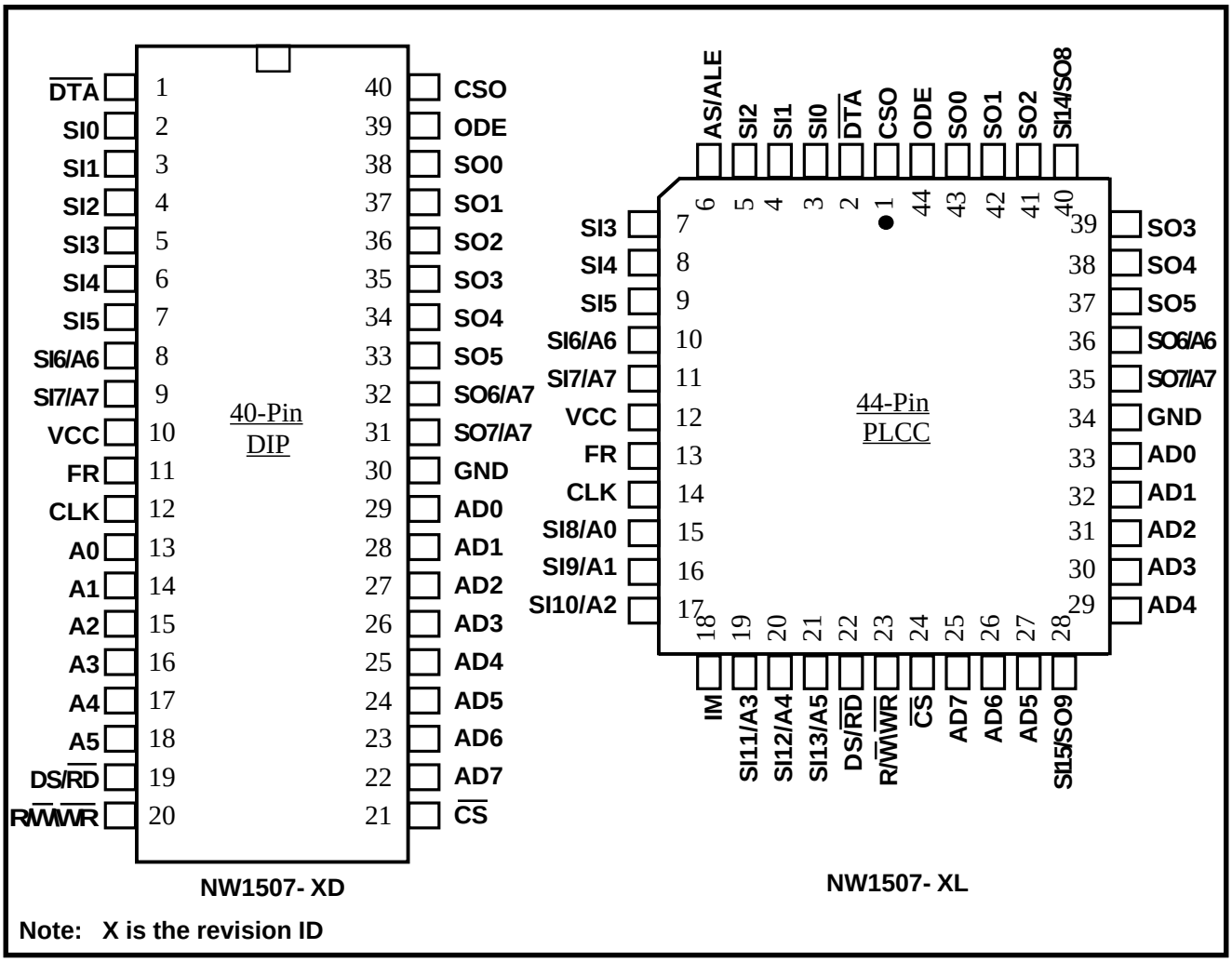


Figure-2. Pin Connections

Pin Description

Name	Type	Pin Number		DESCRIPTION
		40 DIP	44 PLCC	
DTA	O	1	2	**Data Acknowledgement** (Open Drain Output). This is a pin on the microprocessor interface. When this pin is LOW, the data is ready to be accessed. An external 10 KΩ pull-up resistor is required at this output pin.
SI0	I	2	3	**Serial ST-BUS™ Input.** Pins for serial input streams, which may have data rates of 2.048, 4.096 or 8.192Mbits/s with 32, 64 or 128 channels per frame respectively.
SI1		3	4	
SI2		4	5	
SI3		5	7	
SI4		6	8	
SI5		7	9	

Name	Type	Pin Number		DESCRIPTION
		40 DIP	44 PLCC	
SI6/A6	I	8	10	**ST-BUS Input 6/Address Input 6** When multiplexed CPU bus* is selected or input data rate is 2.048 or 4.096Mbits/s, this pin is used as data stream input SI6. When non-multiplexed CPU bus is selected and the input data rate is 4.096 or 8.192Mbits/s, this pin is used as address input A6. Please refer to Table-1, 2, 8&9. If SI6 and A6 are required simultaneously, the A6 input should be connected to pin SO6/A6.
SI7/A7	I	9	11	**ST-BUS Input 7/Address Input 7** When multiplexed CPU bus* is selected or input data rate is 2.048 or 4.096Mbits/s, this pin is used as data stream input SI7. When non-multiplexed CPU bus is selected and the input data rate is 4.096or 8.192Mbits/s, this pin is used as address input A7. Please refer to Table-1, 2, 8&9. If SI7 and A7 are required simultaneously, the A7 input should be connected to pin SO7/A7.
VCC	--	10	12	**Power Supply of +5V.**
FR	I	11	13	**Frame Input** Frame synchronization signals input pin, ST-BUS or GCI are automatically identified.
CLK	I	12	14	**Clock Input** Pin of clock input for shifting data I/O on the serial streams, which may be 4.096 or 8.192MHz.
A0/SI8 A1/SI9 A2/SI10 A3/SI11 A4/SI12 A5/SI13	I	13 14 15 16 17 18	15 16 17 19 20 21	**Address Input/Serial Streams Input** When non-multiplexed CPU bus is selected, address input function is provided. When 16 × 8 switching configuration* is selected, the serial streams input function with data rate of 2.048mbits/s is provided.
DS/$\overline{RD}$	I	19	22	**Data Strobe/Read** When non-multiplexed CPU bus or Motorola multiplexed bus* is selected, the data strobe function is provided. When Intel/National multiplexed bus* is selected, the read function is provided. This active low input configures the AD0~7 as outputs.
R/$\overline{W}$\$\overline{WR}$	I	20	23	**Read/Write \ Write** When non-multiplexed or Motorola multiplexed bus* is selected, the read/write function is enabled: High for read, Low for write. When Intel/National multiplexed bus* is selected, the write function is provided. This active low signal configures the AD0~7 as inputs.
$\overline{CS}$	I	21	24	**Chip Select** Active low Chip Select on the microprocessor interface.
AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0	I/O	22 23 24 25 26 27 28 29	25 26 27 29 30 31 32 33	**Data Bus of Tri-state I/O** Pins of microprocessor access to the internal control registers, Connection Memory High and Low and Data Memory. When multiplexed bus* is selected, address input function is provided. The pins have internal pull down resisters.
GND	--	30	34	**Ground.**

Name	Type	Pin Number		DESCRIPTION
		40 DIP	44 PLCC	
SO7/A7	**O/I**	**31**	**35**	**ST-BUS Output 7/Address Input 7** When multiplexed CPU bus* is selected or data rate is 2.048Mbits/s, this pin is used as data stream output SO7. When non-multiplexed CPU bus is selected and the data rate is 8.192 or 4.096Mbits/s, this pin is used as address input A7. And this pin has internal pull down resister. Please refer to Table-1, 2, 8&9. If SO7 and A7 are required simultaneously, the A7 input should be connected to pin SI7/A7. When both pin SI7/A7 and pin SO7/A7 can be used as A7, pin SO7/A7 is preferred.
SO6/A6	**O/I**	**32**	**36**	**ST-BUS Output 6/Address Input 6** When multiplexed CPU bus* is selected or data rate is 2.048Mbits/s, this pin is used as data stream output SO6. When non-multiplexed CPU bus is selected and the data rate is 8.192 or 4.096Mbits/s, this pin is used as address input A6. And this pin has internal pull down resister. Please refer to Table-1, 2, 8&9. If SO6 and A6 are required simultaneously, the A6 input should be connected to pin SI6/A6. When both pin SI6/A6 and pin SO6/A6 can be used as A6, pin SO6/A6 is preferred.
SO5 **SO4** **SO3** **SO2** **SO1** **SO0**	**O**	**33** **34** **35** **36** **37** **38**	**37** **38** **39** **41** **42** **43**	**Serial ST-BUS™ Output** Pins for serial output streams, which may have data rates of 2.048, 4.096 or 8.192Mbits/s with 32, 64 or 128 channels per frame respectively.
ODE	**I**	**39**	**44**	**Output Drive Enable** Pin to enable the output stream bus. When HIGH, SO9~0 output drivers function normally. When LOW, output drivers go into high impedance state.
CSO	**O**	**40**	**1**	**Control ST-BUS™ Output** Pin of 2.048Mbits/s output with 256 bits per frame. The values of these bits are decided by bit CMH1 of the CMH.
AS/ALE	**I**	**-**	**6**	**Address Strobe or Latch Enable** Effective only when multiplexed bus* is selected via the IM input pin. The address is sampled into address latch circuit at the falling edge of this input. And this pin has internal pull down resister.
IM	**I**	**-**	**18**	**CPU Interface Mode** When HIGH, the device is in multiplexed microprocessor interface mode. When LOW or left open, it is in non-multiplexed CPU interface mode. And this pin has internal pull down resister.
SI15/SO9 **SI14/SO8**	**I/O**	**-**	**28** **40**	**ST-BUS™ Input 15~14/ ST-BUS™ Output 9~8** Effective only when multiplexed bus* is selected. When non-multiplexed bus is selected, the pins are open. When 16 × 8 switching configuration is selected, they are pins for serial ST-BUS™ Input streams, SI15 and SI14, with data rate of 2.048Mbits/s. When Stream Pair Selection is selected, they are pins for serial ST-BUS™ output streams, SO9 and SO8. The pins have internal pull down resisters.

* 44 pin packages only

FUNCTIONAL DESCRIPTION

The NW1507 device, multi-rate time division switch matrix, is designed for switching 32, 64 or N×64Kbits/s data, while guaranteeing the frame integrity for wideband channels and minimum delay for voice channels. The serial streams can operate at the rate of 2.048, 4.096 or 8.192Mbits/s with 32, 64 and 128 time-slots respectively. The width of each frame is 125 μs.

The NW1507 device can be interconnected to backplanes of various speeds like 2.048, 4.096 or 8.192Mbits/s with the use of its built-in rate conversion circuit. The device is compatible with ST-BUS and GCI interface. It can also identify the polarity of the frame synchronization input signal automatically.

Through the CPU Interface Mode input pin, both multiplexed and non-multiplexed bus interfaces can be provided in the 44 pin packages, as well as the compatibility with Intel/ National multiplexed and Motorola multiplexed/non-multiplexed buses. In the 44 pin packages, the NW1507 device can be configured as 16 × 8, which provides a 512 × 256 channel block switching. And the Stream Pair Selection (SPS) function can be used to select which pair of input and output streams will be connected to a internal 128 × 128 channel non-blocking switching.

BLOCK DESCRIPTION

DATA MEMORY & CONNECTION MEMORY

In NW1507, there are two memories used to store data: Data Memory & Connection Memory.

Data Memory, with a capacity of 512 bytes, is used to store byte-wide data converted from input serial data stream. Each location in Data Memory is associated with a specific input stream and channel address. Data Memory can also be read by the controlling microprocessor via MCU Interface.

Connection Memory is used to store the switching configuration originated from the microprocessor. Each location of the Connection Memory is associated with a specific output stream and channel. Connection Memory is divided into two sections: Connection Memory Low (CML) and Connection Memory High (CMH). CML stores the address of the Data Memory, and data in the address will be transmitted to the specific output stream and channel. CMH can control if an individual output channel is placed into the high-impedance state.

CONNECTION MODE

In Connection Mode, the CMH and CML, storing the addresses of the input data, are mapped in a way which each location will correspond to an output channel. After the source address bits being programmed by CPU, the corresponding data in Data Memory will be transmitted to the parallel-to-serial converter. In the case of broadcast facility, an input channel is switched to several output channels.

It is CMH bits that control each output channel's features: constant or variable throughput delay, enable or disable the output driver. For some configuration, additional stream and channel address bits are available in the CMH. In 2.048 Mbits/s applications, one bit is provided by the CMH to control the CSO output.

By pulling the ODE input pin LOW, all output channels can be placed in high impedance. While with the CMH bits, per-channel tri-state control is achievable.

The Data Memory data comes from Serial-to-Parallel Converter, while the Connection Memory data is from control interface. All the data are addressed through the Control register bits and address input pins. The higher order address bits, capable of being written or read via MCU interface, are from the Control register, while the lower ones are from address input pins.

SERIAL STREAM INTERFACE

The serial data rate is usually 2.048, 4.096 or 8.194Mbits/s. Data rates must be same among input streams or output streams. While between input and output, data rates can be identical or different. Therefore, the NW1507 device can be applied in backplanes of various rates or rate conversion applications. Identical or Different I/O rates is selected by the IC7 bit in Interface Configuration Register (ICR). And then the IC2-1 bits select the switch configuration and the I/O streams number. When system power on, the IC6-3 bits are also set up.

For applications of Identical I/O rate, the master clock is at 4.096 or 8.192Mbits/s, that is, twice or equal to the data rate, which is selected by the IC0 bit in ICR. For ST-BUS or GCI format, the I/O rate is 2.048Mbits/s, the IC0 bit is set LOW to make the clock 4.096MHz, twice of the data rate. While for applications with I/O rate of 4.096 or 8.192Mbits/s, the IC0 bit is set HIGH to make the clock equal to the data rate. In applications of Different I/O rate, the IC0 bit is not used.

In ST-BUS or GCI format, the input frame pulse is 8kHz. The NW1507 device can automatically identify it, as well as the serial interface. According to the type of backplane on the serial interface, suitable transmit and sampling edges are established by the internal timing unit. In ST-BUS format, bit transmit operation is performed on every second falling edge of the clock, while bit sampling on the rising edge, at three-quarters of the bit boundary. In GCI format, these edges inverted.

For applications of identical I/O data rate of 4.096 or 8.192Mbits/s, the interface clock is equal to the data rate. For positive frame pulse polarity, every rising edge of the clock marks the bit boundary, while data sampling is performed on every falling edge. For negative frame pulse polarity, every falling edge of the clock marks the bit boundary, while data sampling is performed on every rising edge.

For applications of different I/O data rate, in the 2.048Mbits/s side, the transmit and sampling edges are established as in ST-BUS or GCI format; in the 4.096 or 8.192Mbits/s side, the edges vary according to the applied frame pulse polarity.

SWITCHING CONFIGURATIONS

Switching configurations vary according to the I/O serial rates. For identical I/O rates, the IC7 bit of the ICR is LOW, and IC2-1 bits determine the switching configuration. For different I/O rates, the IC7 bit is HIGH, and the IC6-3 bits define the switching configuration as non-blocking with different I/O stream number.

Identical I/O rates

When bit IC7 is LOW and the identical I/O rate is determined, bits IC6-5 select the I/O rate. (Bits IC4-3 are ignored.) And bits IC2-1 determine the switching configuration.

I. 2.048Mbits/s serial rates

When the I/O rate is selected to be 2.048Mbits/s by bits IC6-5, bits IC2-1 determine the switching configuration among 4 possible types: 8 × 8, 16 × 8, 4 × 4 with SPS (Stream Pair Selection), and nibble switching.

1. Switching configuration of 8 × 8
   8 serial streams input and 8 output with 32 64Kbits/s channels each, resulting in 256 × 256 non-blocking switchings; ST-BUS and GCI format compatible; variable and constant throughput delay provided; 4.096Mbits/s master clock; 40 and 44 pin packages available.
2. Switching configuration of 16 × 8
   16 serial streams input and 8 output with 32 64Kbits/s channels each, resulting in 512 × 256 blocking switchings; ST-BUS and GCI format compatible; Multiplex bus mode controller interface; only variable throughput delay provided; 4.096Mbits/s master clock; 44 pin packages available.
3. Switching configuration of 4 × 4 with Stream Pair Selection (SPS)
   4 serial streams input and 4 output. 2 pairs of them (SI0/SO0 & SI1/SO1) are permanently linked. The other 2 pairs (Called Pair A & Pair B) are selected from the remaining 8 pairs of serial streams (SI2/SO2 to SI9/SO9) by SPS register. While CML is set, SI0~3 and SO0~3 are connected respectively.
   128 × 128 non-blocking switchings. ST-BUS and GCI format compatible; variable and constant throughput delay provided; 4.096Mbits/s master clock; 44 pin packages available.
4. Nibble switching
   4-bit wide 32Kbits/s data is transferred on each serial stream with 64 nibbles per frame. 8 serial streams input and 4 output, resulting in 512 × 256 blocking switchings. In addition, the NW1507 device can also provide 256 × 256 non-blocking switchings, with any 4 of the 8 input streams selected. 4.096Mbits/s master clock.

II. 4.096Mbits/s serial rates

2 types of switching configurations are available: 8 × 4 and 4 × 4.

1. Switching configuration of 8 × 4
   8 serial streams input and 4 output with 64 64Kbits/s channels each, resulting in 512 × 256 blocking switchings; only variable throughput delay provided; 4.096Mbits/s master clock.
2. Switching configuration of 4 × 4
   4 serial streams input and 4 output with 64 64Kbits/s channels each, resulting in 256 × 256 non-blocking switchings; variable and constant throughput delay provided;

III. 8.192Mbits/s serial rates
Only one type of switching configurations is available: 2 × 2. 2 serial streams input and 2 output with 128 64Kbits/s channels each, resulting in 256 × 256 non-blocking switchings. 8.192Mbits/s master clock.

Serial I/O rates (Mbits/s)	Serial Streams (I × O)		I/O Streams Selected	Switching Matrix (channels)	Blocking or Non-blocking	Timeslots per Frame	Throughput Delay Selection	Packages (40/44 pin)	Master Clock (MHz)
2.048	* 8 × 8		SI0~7/ SO0~7	256 × 256	Non-blocking	32	Variable & Constant	40 & 44 pin	4.096
	* 16 × 8		SI0~15/ SO0~7	512 × 256	Blocking		Variable Only	44 pin only	
	** 10 × 10		SI0~9/ SO0~9	128 × 128	Non-blocking		Variable & Constant	44 pin only	
	Nibble Switch	8 × 4	SI0~7/ SO0~3	512 × 256	Blocking	64 nibbles	Variable Only	40 & 44 pin	
		*** 8 × 4		256 × 256	Non-blocking				
4.096	8 × 4		SI0~7/ SO0~3	512 × 256	Blocking	64	Variable Only	40 & 44 pin	4.096
	4 × 4		SI0~3/ SO0~3	256 × 256	Non-blocking		Variable & Constant	40 & 44 pin	
8.192	2 × 2		SI0~1/ SO0~1	256 × 256	Non-blocking	128	Variable & Constant	40 & 44 pin	8.192

* ST-BUS and GCI interface compatible
** Only 4 input × 4 output will be selected by SPS
*** Only 4 of the 8 input streams are selected

Table-1. Switching Configurations for identical I/O rates

Different I/O rates

After bit IC7 in ICR determine the different I/O rates, bits IC6-5 select the input data rates, while bits IC4-3 select the output. (Bits IC2-1 are ignored.) The NW1507 device can convert 2.048Mbits/s serial data into 4.096Mbits/s or 8.192Mbits/s, and vice-versa.

256 × 256 non-blocking switchings are provided, and also the per-channel selection between variable and constant throughput delay.

4 types of switching configurations are available with different master clock and different input stream number and output stream number. *As the following table*

Input Rate (Mbits/s)	Output Rate (Mbits/s)	Serial Streams (I × O)	Input Streams Selected	Output Streams Selected	Switching Matrix (channels)	Blocking or Non-blocking	Throughput Delay Selection	Master Clock (MHz)
2.048	4.096	8 × 4	SI0-7	SO0-3	256 × 256	Non-blocking	Variable & Constant	4.096
2.048	8.192	8 × 2	SI0-7	SO0-1				8.192
4.096	2.048	4 × 8	SI0-3	SO0-7				4.096
8.192	2.048	2 × 8	SI0-1	SO0-7				8.192

Table-2. Switching Configurations for different I/O rates

Input Frame Offset Selection

Because of different backplanes applied, different delay occurs to the input serial data. That is, the serial data are input a little bit later than the frame synchronization signals.

To offset the delay, the function, Input Frame Offset Selection, is offered by the NW1507 device, while the serial interface is at 4.096Mbits/s or 8.192Mbits/s. In this operation, depending on the CPU in the Frame Input Offset Register (FIOR), an internal delay of up to 4 clock periods is added to the input serial data sampling, so as to create a new input frame reference, aligning with the framing of input data.

Meanwhile the frame of the output data is still aligned with the original system frame synchronization. And this function also can be disabled by the FIOR.

THROUGHPUT DELAY

Delay occurs when data pass through the switch matrix. To cover it, the NW1507 provides 2 types of throughput delay: one is Variable Delay, provided for voice data to ensure minimum delay; the other is Constant Delay, provided for wideband data to guarantee the frame integrity.

Bit CMH6 of the CMH determines the type of the throughput delay. When bit CMH6 = 0, Variable Delay is selected. When bit CMH6 = 1, Constant Delay is selected.

I. In Variable Mode
For identical I/O Data Rates, it is the input and output channels that determine the throughput delay, while the serial data rate determine the achievable minimum delay. If the throughput delay is more than the minimum, it must be equal to the difference of the input & output channels. *Details can be found in Table-3.*

For different I/O Data Rates, the throughput delay is determined by the output streams in cases of 4.096 to 2.048Mbits/s and 8.192 to 2.048Mbits/s rate conversions, and by input streams in cases of 2.048 to 4.096Mbits/s and 2.048 to 8.192Mbits/s. *Details can be found in Table-4 & 5.*

II. In Constant Mode
Multiple Data-Memory buffers are used to maintain the data sequence integrity. Suppose the data is written in the buffers during frame n, it will be read out during frame n+2. Therefore, the throughput delay is ranged from 1 frame to (3 frames – 2 timeslots). *Details can be found in Table-6:*

I/O Rate (Mbits/s)	Timeslot Value (µs)	Minimum Delay (timeslots)	Throughput Delay Value (timeslots)				
			dc < 0	dc = 0, 1, 2	dc = 3, 4	dc = 5, 6, 7, 8	dc > 8
2.048	3.9	3	32 + dc	32 + dc	dc	dc	dc
4.096	1.95	5	64 + dc	64 + dc	64 + dc	dc	dc
8.192	0.975	9	128 + dc	128 + dc	128 + dc	128 + dc	dc

* dc(difference of the output & input channels) = output channel – input channel

Table-3. Variable Delay Values for identical I/O rates

Input Rate (Mbits/s)	Output Rate (Mbits/s)	Throughput Delay (µs)	Output Streams			
			0, 1	2, 3	4, 5	6, 7
2.048	4.096	Maximum	4b + d			
		Minimum	5b			
2.048	8.192	Maximum	8a + d			
		Minimum	9a			
4.096	2.048	Maximum	2c + d		c + b + d	
		Minimum	3c		2c + b	
8.192	2.048	Maximum	2c + d	c + 3a +d	c + 2a +d	c + a +d
		Minimum	3c	2c + 3a	2c + 2a	2c + a

* a = 8Mbits/s timeslot = 0.975µs; b = 4Mbits/s timeslot = 1.95µs; c = 2Mbits/s timeslot = 3.9 µs; d = 1fr. = 125µs

Table-4. Variable Delay Values for different I/O rates (with SO)

Input Rate (Mbits/s)	Output Rate (Mbits/s)	Throughput Delay (µs)	Input Streams			
			0, 1	2, 3	4, 5	6, 7
2.048	4.096	Maximum	2c + d		c + b + d	
		Minimum	3c		2c + b	
2.048	8.192	Maximum	2c + d	c + 3a +d	c + 2a +d	c + a +d
		Minimum	3c	2c + 3a	2c + 2a	2c + a
4.096	2.048	Maximum	4b + d			
		Minimum	5b			
8.192	2.048	Maximum	8a + d			
		Minimum	9a			

* a = 8Mbits/s timeslot = 0.975µs; b = 4Mbits/s timeslot = 1.95µs; c = 2Mbits/s timeslot = 3.9 µs; d = 1fr. = 125µs

Table-5. Variable Delay Values for different I/O rates (with SI)

Serial Rate (Mbits/s)	2.048	4.096	8.192
Timeslot Value (µs)	3.9	1.95	0.975
Throughput Delay (timeslots)	(32 – i) + 32 + (o - 1)	(64 - i) + 64 + (o - 1)	(128 - i) + 128 + (o - 1)
Range of i & o	1 ~ 32	1 ~ 64	1 ~ 128

* i: input timeslot; o: output timeslot

Table-6. Constant Delay Values

MCU Interface

In the 44 pin packages, the NW1507 device provides both non-multiplexed bus interface and multiplexed bus interface, which is determined by the CPU Interface Mode (IM) input pin. When the pin is open or grounded, non-multiplexed bus interface is provided compatible to Motorola CPUs; when it is connected to HIGH, multiplexed bus interface is provided compatible to Motorola, National and Intel CPUs.

The type of CPU bus connected is automatically identified by the MOTEL circuit (Motorola and Intel compatible bus) with the use of DS/$\overline{RD}$ input pin. While the level of the pin is LOW at the rising edge of AS/ALE, the Motorola bus timing is selected. While it is HIGH, the Intel bus timing is selected.

While Motorola, National or Intel multiplexed bus interfaces are used, following signals are available for controlling the NW1507 device: AD7~0, AS/ALE, DS/$\overline{RD}$, R/$\overline{W}$\$\overline{WR}$, $\overline{CS}$ and $\overline{DTA}$. While Motorola non-multiplexed bus interfaces are used, following signals are available for controlling the NW1507 device: AD7~0, A0~5, DS/$\overline{RD}$, R/$\overline{W}$\$\overline{WR}$, $\overline{CS}$ and $\overline{DTA}$.

Via the bus interfaces, the CPU can set connection to Data Memory, Connection Memory, Control Registers, Interface Configuration Register. The Data Memory can be read only, while the others can be both read and written.

SOFTWARE CONTROL DESCRIPTION

Address input pins A7~0 determine the internal registers and memories. When A5 is LOW, the combination of A1 and A0 determines the Internal Registers: Internal Control, Interface Mode, Stream Pair Selection and Frame Input Offset registers. When A5 is HIGH, all the other address input pins participate in determining the memory subsections, which is up to 128 locations specifying the input and output channels. *Details can be found in Table-7.*

A7	A6	A5	A4	A3	A2	A1	A0	Internal Registers / Memory Locations
×	×	0	×	×	×	0	0	Control Register
×	×	0	×	×	×	0	1	Interface Mode Select Register
×	×	0	×	×	×	1	0	Stream Pair Select Register
×	×	0	×	×	×	1	1	Frame Input Offset Register
0	0	1	0 ∫ 1	0 ∫ 1	0 ∫ 1	0 ∫ 1	0 ∫ 1	Channel 0 ∫ Channel 31
0	1	1	0 ∫ 1	0 ∫ 1	0 ∫ 1	0 ∫ 1	0 ∫ 1	Channel 32 ∫ Channel 63
1	0 ∫ 1	1	0 ∫ 1	0 ∫ 1	0 ∫ 1	0 ∫ 1	0 ∫ 1	Channel 64 ∫ Channel 127

* Channel 0~31 are applied in 2.048Mbits/s (8 × 8, 16 × 8 and 10 × 10)
* Channel 0~63 are applied in 4.096Mbits/s (4 × 4, 8 × 4, nibble or different I/O rates)
* Channel 0~127 are applied in 8.192Mbits/s (2 × 2 or different I/O rates)

Table-7. Address Memory Map

Address input pins and bits of the Control Register determine all sections of the Data Memory and Connection Memory HIGH & LOW.

Bits of the Control Register are divided into 4 types: Split Memory bits, Connection Mode bits, Memory Select bits and Stream Address bits. *Details can be found in Figure 3.*

Bit CR7 of the Control Register, Split Memory bit, determines the split memory operation: reading from the Data Memory and writing to Connection Memory LOW.

Bits CR4 & CR3, Memory Select bits, determine the selection of the Data Memory, the Connection Memory HIGH and LOW.

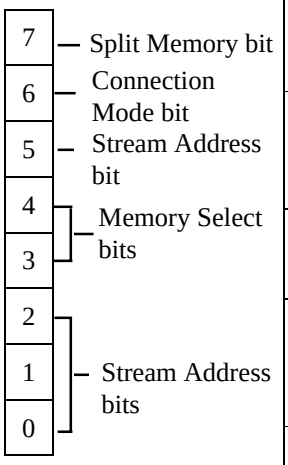
Bits CR5 and CR2~1, Stream Address bits, determine the memory subsections specifying the input and output channels.

Bit CR6, Connection Mode bit, determines the content of output channels when it is LOW.

When ODE input pin is LOW, all the output channels are in high impedance. When ODE is HIGH, bits CMH0 of the CMH determine the output drivers for the output stream and channel related.

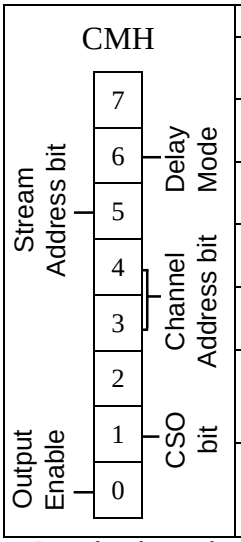
Bit CMH1 of the CMH is only available in 2.048Mbits/s applications. The content of the bit is transmitted on to the CSO pin, synchronous to the ST-BUS stream. When bit CMH1 is HIGH, the related bit on CSO pin is transmitted HIGH. When it is LOW, the related bit is also LOW. The content of the bit is transmitted one channel before the related channel on the output streams.

Bit CMH6 determines Variable and Constant throughput delay modes on per channel basis. *Details can be found in Figure 4a.*



Bit	State	Description
CR7	0	Memory Select bit specifies the memory for subsequent operation
	1	All reads are from Data Memory, while writes are to CML if CR3=0, or to CMH if CR3=1
CR6	0	The Connection Memory bits determine the content of output channel related
	1	Reserved
CR5		It is only used in 16 × 8 switching configuration of 44 pin packages. With bits CR2~0, it can determine the input serial stream selection.
CR4 × CR3	0 × 0	Undefined
	0 × 1	For selection of Data Memory (if read)
	1 × 0	For selection of CML
	1 × 1	For selection of CMH
CR2 CR1 CR0		These bits expressed in binary notation indicate the input or output streams corresponding to the subsection of memory made accessible for subsequent operations

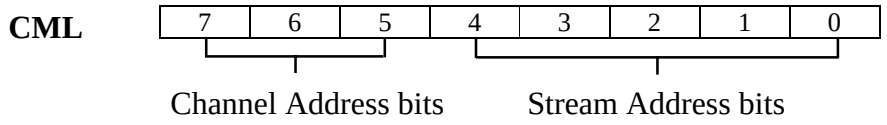
Figure-3. Control Register Bits



Bit	Description
CMH7	Unused
CMH6	Providing per-channel selection of Variable/Constant Throughput Delay Mode while the switching configuration has this function.
CMH5	Used together with bits CML7~5 of CML to select up to 16 different source streams for the connection. *
CMH4 CMH3	Used together with bits CML4~0 of CML to select up to 128 different source channels for the connection. *
CMH2	No effect
CMH1	Available only in 2.048Mbits/s applications. The content of this bit is output sequentially on to the CSO pin, one channel earlier than the related channel on the ST-BUS streams.
CMH0	Effective only when CR6 is LOW. When '1', the output driver of the location's channel and stream is enabled. When '0', the individual channel on individual stream is made high-impedance.

* Depending the switching configuration and the data rate used in the application, not all the bits have to be used. *Details can be found in table 9 &10.*

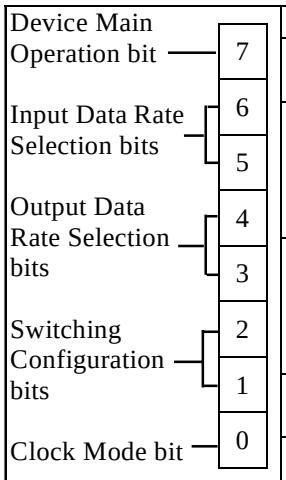
Figure-4a. Connection Memory High Bits



Bit	Description
CML7~5	Used together with bits CMH5 of CMH to select up to 16 different source streams for the connection. *
CML4~0	Used together with bits CMH4~3 of CMH to select up to 128 different source channels for the connection. *

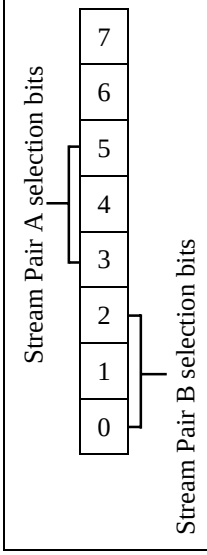
* Depending the switching configuration and the data rate used in the application, not all the bits have to be used. *Details can be found in table 9 &10.*

Figure-4b. Connection Memory Low Bits



Bit	Description	State	Selection
IC7	Used to determine Identical or Different I/O data rate.	0	Identical I/O rate
		1	Different I/O rate
IC6 × IC5	Used to determine the input data rate. And also determine the output data rate when IC7 is LOW.	0 × 0	2.048Mbits/s
		0 × 1	4.096Mbits/s
		1 × 0	8.192Mbits/s
		1 × 1	Undefined
IC4 × IC3	Used to determine the output data rate. It is not effective when IC7 is LOW.	0 × 0	2.048Mbits/s
		0 × 1	4.096Mbits/s
		1 × 0	8.192Mbits/s
		1 × 1	Undefined
IC2 IC1	It is effective only when IC7 is LOW.	*Details can be found in Table-10.*	
IC0	No effect.		

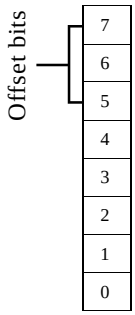
Figure-5. Interface Configuration Register



Bit	Description				
SPS7 SPS6	Ignored				
SPS5 SPS4 SPS3	Besides the two pairs of permanently connected streams SI1/SO1 & SI0/SO0, another two pairs of streams are selected respectively from the remaining streams SI2~9/SO2~9. *	SPS5	SPS4	SPS3	Stream Pair A Connected
		0	0	0	SI2/SO2
		0	0	1	SI3/SO3
		0	1	0	SI4/SO4
		0	1	1	SI5/SO5
		1	0	0	SI6/SO6
		1	0	1	SI7/SO7
		1	1	0	SI8/SO8
		1	1	1	SI9/SO9
SPS2 SPS1 SPS0		SPS2	SPS1	SPS0	Stream Pair B Connected
		0	0	0	SI2/SO2
		0	0	1	SI3/SO3
		0	1	0	SI4/SO4
		0	1	1	SI5/SO5
		1	0	0	SI6/SO6
		1	0	1	SI7/SO7
		1	1	0	SI8/SO8
		1	1	1	SI9/SO9

* These bits are only effective while 2.048Mbits/s data rate is selected and bit IC2 = 1 & bit IC1 = 0.

Figure-6. SPS Register Bits



Bit	Description				
FIO7 FIO6 FIO5	Depending on these bits, an internal delay of up to 4 clock periods to the actual data input sampling, to create an virtual frame aligning with the input serial data framing. *	FIO7	FIO6	FIO5	Number of Clock Periods
		0	0	0	0
		0	0	1	1
		0	1	0	2
		0	1	1	3
		1	0	0	4
		1	0	1	Undefined
		1	1	0	Undefined
		1	1	1	Undefined
FIO4~0	Ignored				

* If this function is not required, the register should be set up during system initialization to a state where offset function are disabled.

Figure-7. FIO Register Bits

Serial I/O rates (Mbits/s)	Serial Streams (I × O)	Bits for Data Memory subsections selection	Bits for Connection Memory subsections selection	Input Address pins for individual Data & Connection Memory positions access
2.048	8 × 8	SA2~0	SA2~0	A4~0
	* 4 × 4	SA1~0	SA1~0	A4~0
	* 16 × 8	SA3~0	SA2~0	A4~0
2.048 (Nibble)	8 × 4	SA2~0	SA1~0	A6, A4~0
4.096	4 × 4	SA1~0	SA1~0	A6, A4~0
	8 × 4	SA2~0	SA1~0	A6, A4~0
8.192	2 × 2	SA0	SA0	** A7~6, A4~0

***** Available only in 44 pin package
** Pin A0 is not required for Data Memory Read operations

Table-8. Use of Stream Address Bits for Identical I/O Data Rate Operation

Input Serial Rate (Mbits/s)	Output Serial Rate (Mbits/s)	Serial Streams (I × O)	Bits for Data Memory subsections selection	Bits for Connection Memory subsections selection	Input Address pins for individual Data Memory positions access	Input Address pins for individual Connection Memory positions access
2.048	4.096	8 × 4	SA2~0	SA1~0	A4~0	A7~6, A4~0
2.048	8.192	8 × 2	SA2~0	SA0	A4~0	A6, A4~0
4.096	2.048	4 × 8	SA1~0	SA2~0	A6, A4~0	A4~0
8.192	2.048	2 × 8	SA0	SA2~0	A7~6, A4~0	A4~0

Table-9. Use of Stream Address Bits for Different I/O Data Rate Operation

Bit IC7	Data Rate (Mbits/s)	IC2	IC1	Switching Configuration	Blocking/ Non-blocking
* IC7 = 0, Identical I/O rates determined.	2.048	0	0	8 × 8	Non-blocking
		0	1	** 16 × 8	Blocking
		1	0	** 4 × 4 (with SPS)	Non-blocking
		1	1	8 × 4 (Nibble)	Blocking
	4.096	0	0	8 × 4	Blocking
		0	1	4 × 4	Non-blocking
		1	0	Undefined	
		1	1	Undefined	
	8.192	No effect		2 × 2	Non-blocking

* When IC7 = 1, different I/O rates is determined, the Switching Configurations bits are not effective, and the device is in Non-blocking switch configuration with a 256 × 256 channel capacity.
** Available only in 44 pin packages.

Table-10. Switching Configurations Bits for Identical I/O Rates

Serial I/O Rate (Mbits/s)	Serial Streams (I × O)	Source Stream Address Bits used	Source Channel Address Bits used	Source channels determined (channels/stream)
2.048	8 × 8	CML7~5	CML4~0	32
	* 4 × 4	CML7~6		
	* 16 × 8	CMH5, CML7~5		
Nibble Switch (2.048)	8 × 4	CML7~5	CMH3 CML4~0	64
4.096	4 × 4	CML7~6	CMH3 CML4~0	64 (nibbles/stream)
	8 × 4	CML7~5		
8.192	2 × 2	CML7	CMH4~3 CML4~0	128

* Available only in 44 pin package

Table-11. Stream & Channel Address Bits used for Identical I/O Rate Applications

Input Serial Rate (Mbits/s)	Output Serial Rate (Mbits/s)	Serial Streams (I × O)	Source Stream Address Bits used	Source Channel Address Bits used	Source channels determined (channels/stream)
2.048	4.096	8 × 4	CML7~5	CML4~0	32
2.048	8.192	8 × 2	CML7~5		
4.096	2.048	4 × 8	CML7~6	CMH3, CML4~0	64
8.192	2.048	2 × 8	CML7	CMH4~3, CML4~0	128

Table 12. Stream & Channel Address Bits used for Different I/O Rate Applications

Application Information

Switch Matrices

While guaranteeing the integrity of grouped data and minimum delay for voice, the NW1507 device can provides non-blocking switch matrices of up to 512 channels with different connections at different data rates. *Examples see Figure 8~10.*

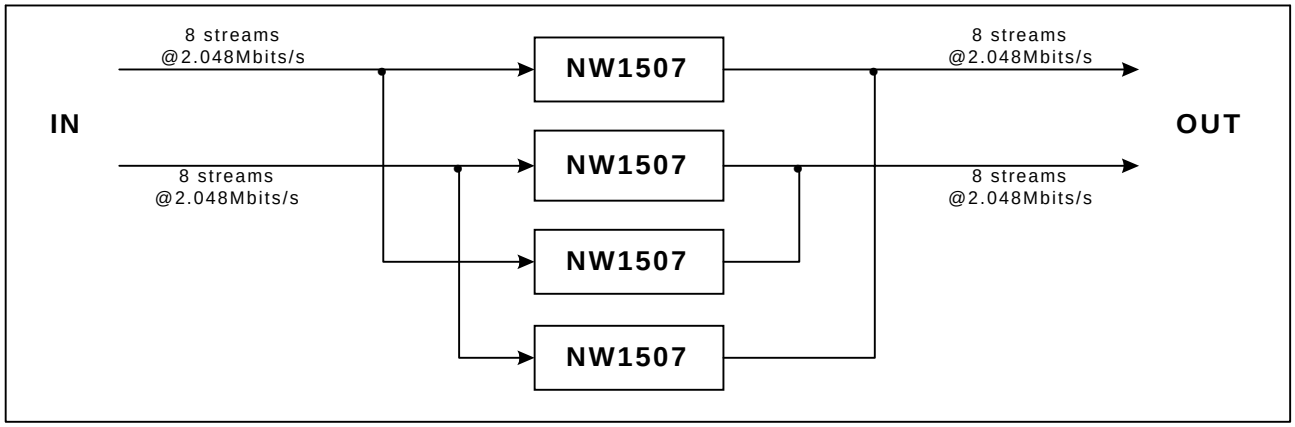


Figure-8. 512-Channel Switch with Data Rate at 2.048 and 4.096 Mbits/s

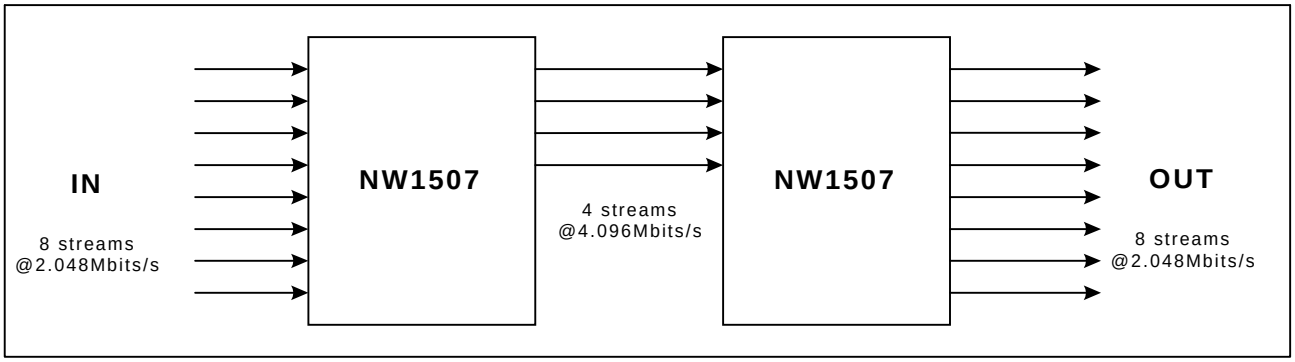


Figure-9. 256-Channel Switch with Rate Conversion between 2.048 and 4.096 Mbits/s

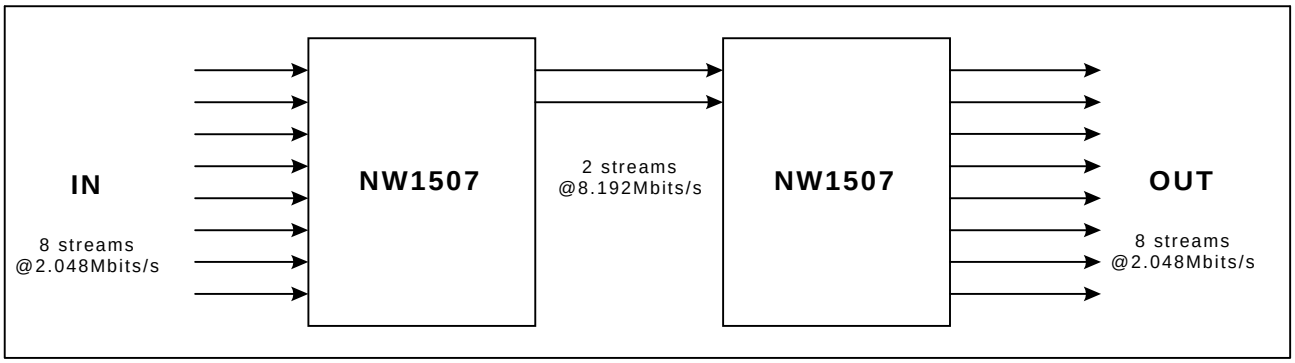


Figure-10. 256-Channel Switch with Rate Conversion between 2.048 and 8.192 Mbits/s

Furthermore, the NW1507 device can also provide non-blocking matrices of up to 1024 channels, while only variable throughput delay is guaranteed. *Examples see Figure 11~12.*

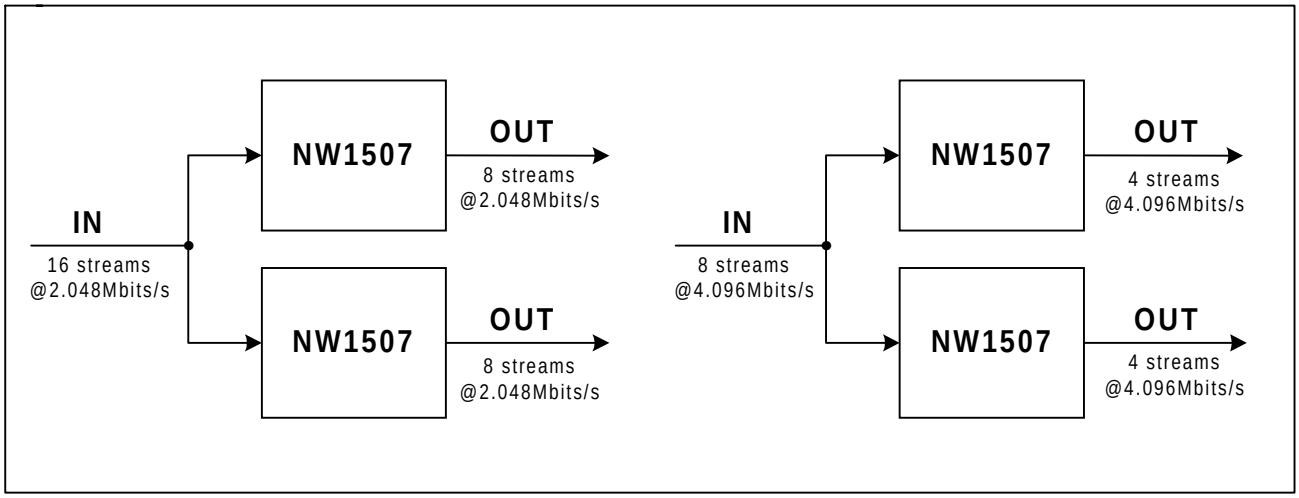


Figure-11. 512-Channel Non-Blocking Switch Matrix with Data Rate at 2.048 or 4.096Mbits/s

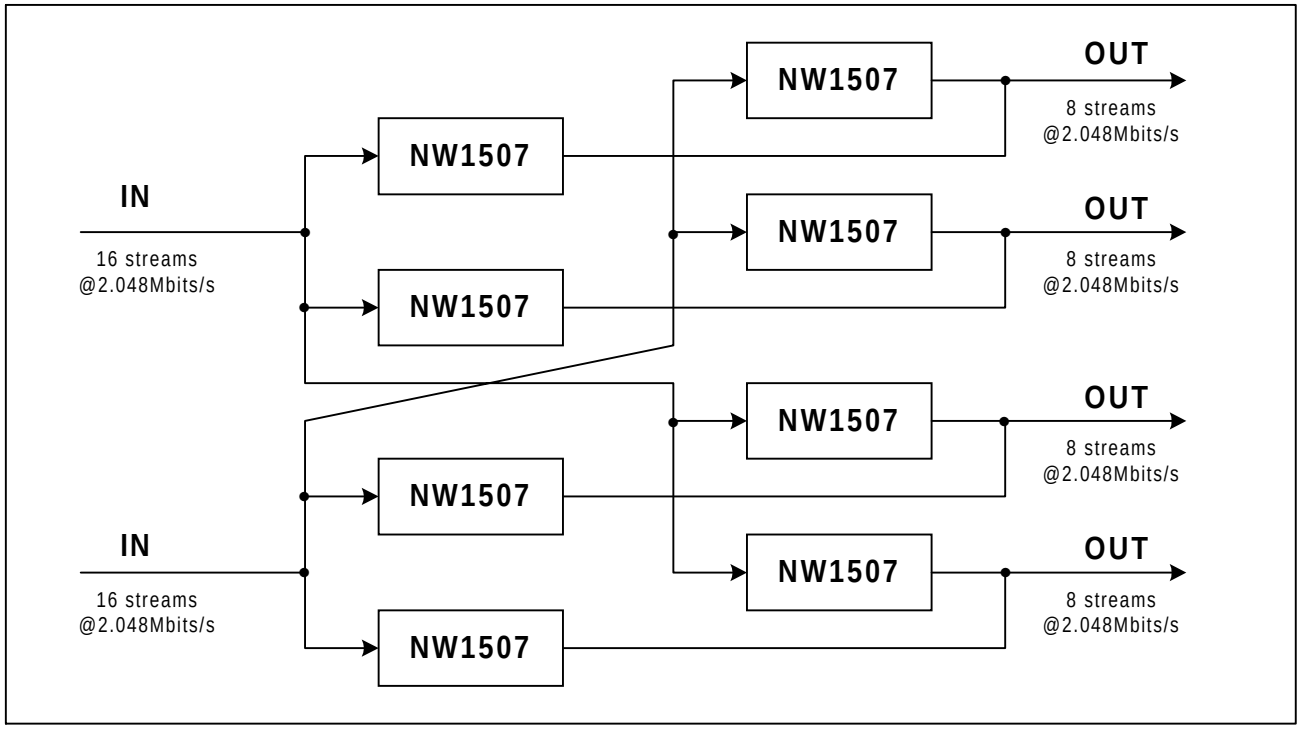


Figure-12. 1024-Channel Non-Blocking Switch Matrix with Data Rate at 2.048Mbits/s

Interfacing Microcontroller 8051

In applications where the NW1507 device is connected to Intel 8051, some external logic are necessary to be provided in the connection to allow read/write operation. *The typical application diagram see Figure-13.*

When reading or writing to NW1507, the address decoded signal ($\overline{NWA}$) latches signals $\overline{RD}$, $\overline{WR}$ and ALE, and releases it when NW1507 output the $\overline{DTA}$ signal. During a write, Latch U5 stores the 8051 data when $\overline{DTA}$ goes low.

During a read, Latch U4 stores NW1507 output data when $\overline{DTA}$ goes low.

One write operation is enough when writing to NW1507, while two read operations are required when reading (only the second operation is valid).

Sufficient time should be guaranteed between two CPU accesses to allow for an internal NW1507 reaction over the first $\overline{RD}$/$\overline{WR}$ access. For a read, at least 1220ns; while for a write, at least 800ns.

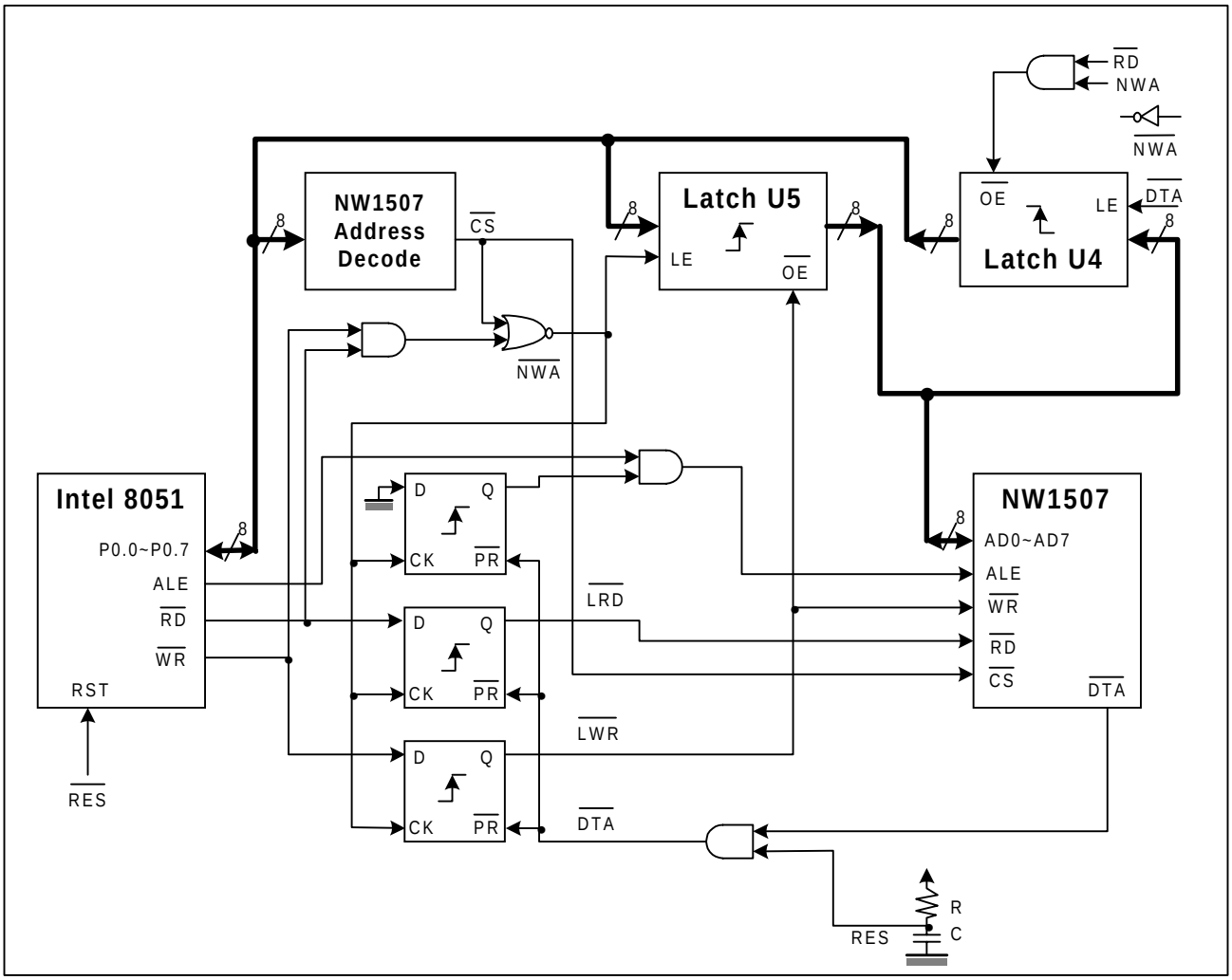


Figure-13. Interfacing NW1507 with Intel 8051

Maximum Rating

Supply Voltage: -0.3V to 7V
Digital Input Voltage: -0.3V to 7V
Digital Output Voltage: -0.3V to 7V
Digital Output Current: ≤ 40mA
Package Power Dissipation: ≤ 2W
Storage Temperature: -65°C to +150°C

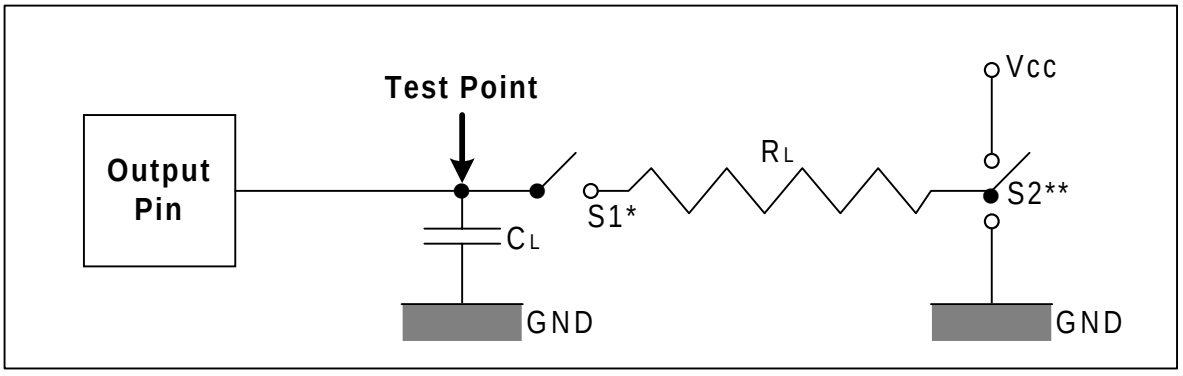
Recommended Operating Conditions

Operating Temperature: -40°C to +85°C
Power Supply: 4.75V to 5.25V
Input Voltage: 0V to Vcc

DC Electrical Characteristics

Par-meter	Description		Min	Typ*	Max	Units	Test Conditions
V_{OH}	Output High Voltage		2.4			V	I_{OH} = 10mA
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 5mA
V_{IH}	Input High Voltage		2.0			V	
V_{IL}	Input Low Voltage				0.8	V	
I_{CC}	Supply Current			10	15	mA	All outputs unloaded
I_{OH}	Output High Current			-15	-10	mA	V_{OH} = 2.4V
I_{OL}	Output Low Current		5	10		mA	V_{OL} = 0.4V
I_{IL}	Input Leakage	Input pins			5	µA	V_I between Vcc and GND
		I/O pins,IM,AS		34	100		
I_{OZ}	High Impedance Leakage				5	µA	V_O between Vcc and GND
C_O	Output Pin Capacitance			8		pF	
C_I	Input Pin Capacitance			8		pF	

*Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



*S1 is open circuit except when testing output levels or high impedance states.
**S2 is switched to Vcc or GND when testing output levels or high impedance states.

Figure-13. Output Test Load

AC Electrical Characteristics - ST-BUS Timing & GCI Timing

Par-meter	Description	Min	Typ	Max	Units	Test Conditions
t1	Clock Period	190	244	300	ns	
t10		150				
t2	Clock Width High	85	122	150	ns	
t11		73				
t3	Clock Width Low	85	122	150	ns	
t12		73				
t4	Frame Signal Setup Time	10		190	ns	
t13						
t5	Frame Signal Hold Time	20		190	ns	
t14						
t6	Frame Signal Width		244		ns	
t15						
t7	SO Delay Active to Active		45	100	ns	C_L=150pF
t16						
t8	SI Setup Time	20			ns	
t17						
t9	SI Hold Time	20			ns	
t18						

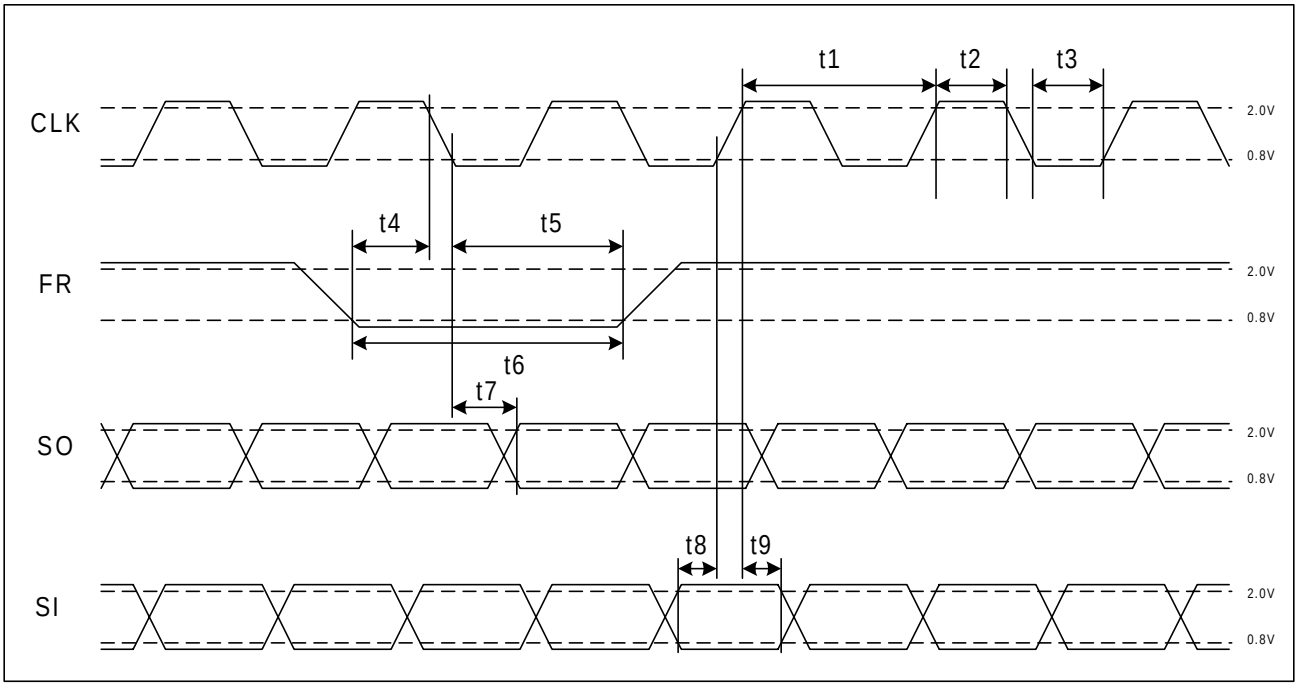


Figure-14. ST-BUS Timing

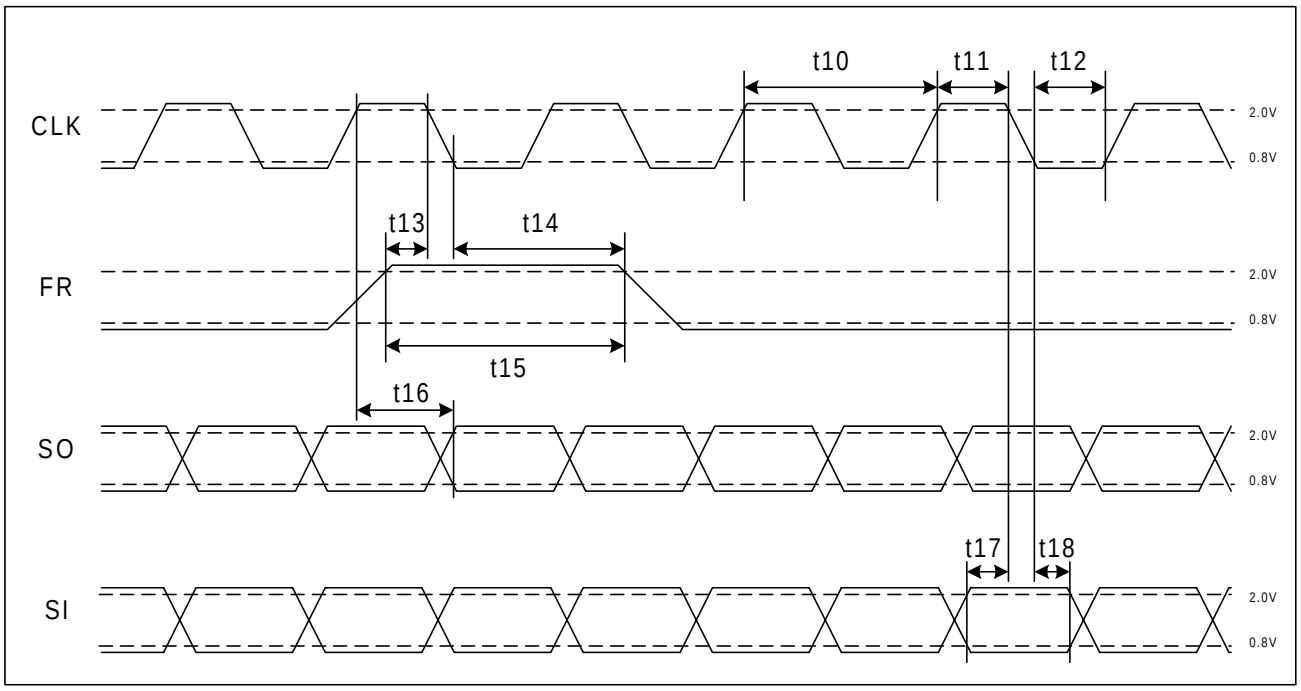


Figure-15. GCI Timing

AC Electrical Characteristics - Serial Streams for ST-BUS and GCI Backplanes (2.048Mbits/s)

Par-meter	Description	Min	Typ	Max	Units	Test Conditions
t19	SO Delay Active to High Z			100	ns	R_L=1KΩ, C_L=150pF
t20	SO Delay High Z to Active			100	ns	C_L=150pF
t21	External Control Delay	0		60	ns	R_L=1KΩ, C_L=150pF
t22	Output Driver Enable Delay			65	ns	C_L=150pF

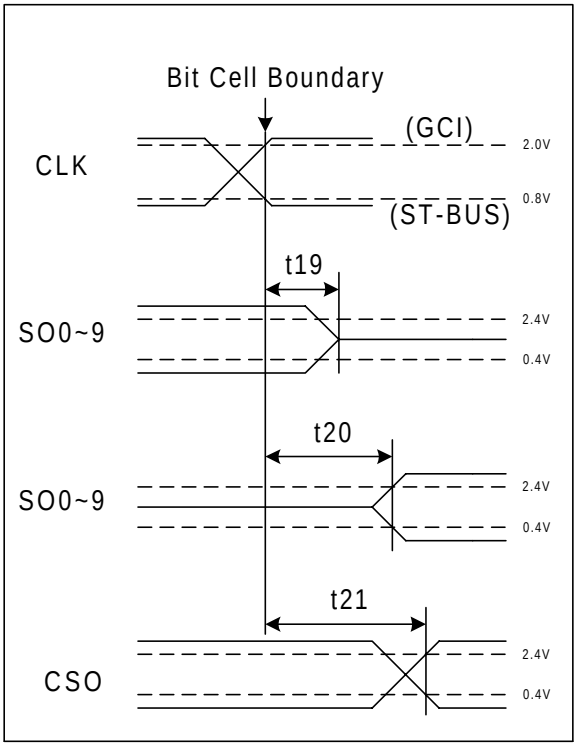


Figure-16. Serial Outputs and External Control

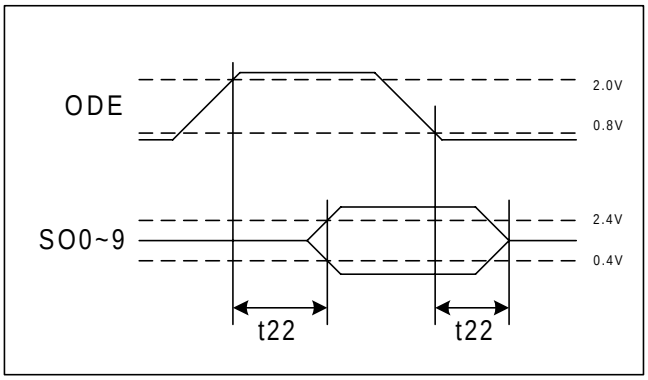


Figure-17. Output Driver Enable

AC Electrical Characteristics - Serial Streams at 4.096 & 8.192Mbits/s

Par-meter	Description	Data Rates	Min	Typ	Max	Units	Test Conditions
t23	Clock Period	4.096	190	244	300	ns	
		8.192	110	122	150	ns	
t24	Clock Width High	4.096	85	122	150	ns	
		8.192	50	60	70	ns	
t25	Clock Width Low	4.096	85	122	150	ns	
		8.192	50	60	70	ns	
t26	Frame Signal Setup Time	4.096	10		190	ns	
		8.192	10		90	ns	
t27	Frame Signal Hold Time	4.096	20		190	ns	
		8.192	20		90	ns	
t28	Frame Signal Width	4.096		244		ns	
		8.192		122		ns	
t29	SO Delay Active to Active	4.096		40	80	ns	C_L=150pF
		8.192		30	50	ns	C_L=50pF
t30	SI Setup Time	4.096	20			ns	
		8.192	20			ns	
t31	SI Hold Time	4.096	20			ns	
		8.192	20			ns	
t32	SO Delay Active to High Z	4.096			80	ns	R_L=1KΩ, C_L=150pF
		8.192			50	ns	R_L=1KΩ, C_L=50pF
t33	SO Delay High Z to Active	4.096			80	ns	C_L=150pF
		8.192			50	ns	C_L=50pF
t34	Output Driver Enable Delay	4.096			65	ns	R_L=1KΩ, C_L=150pF
		8.192			65	ns	R_L=1KΩ, C_L=50pF

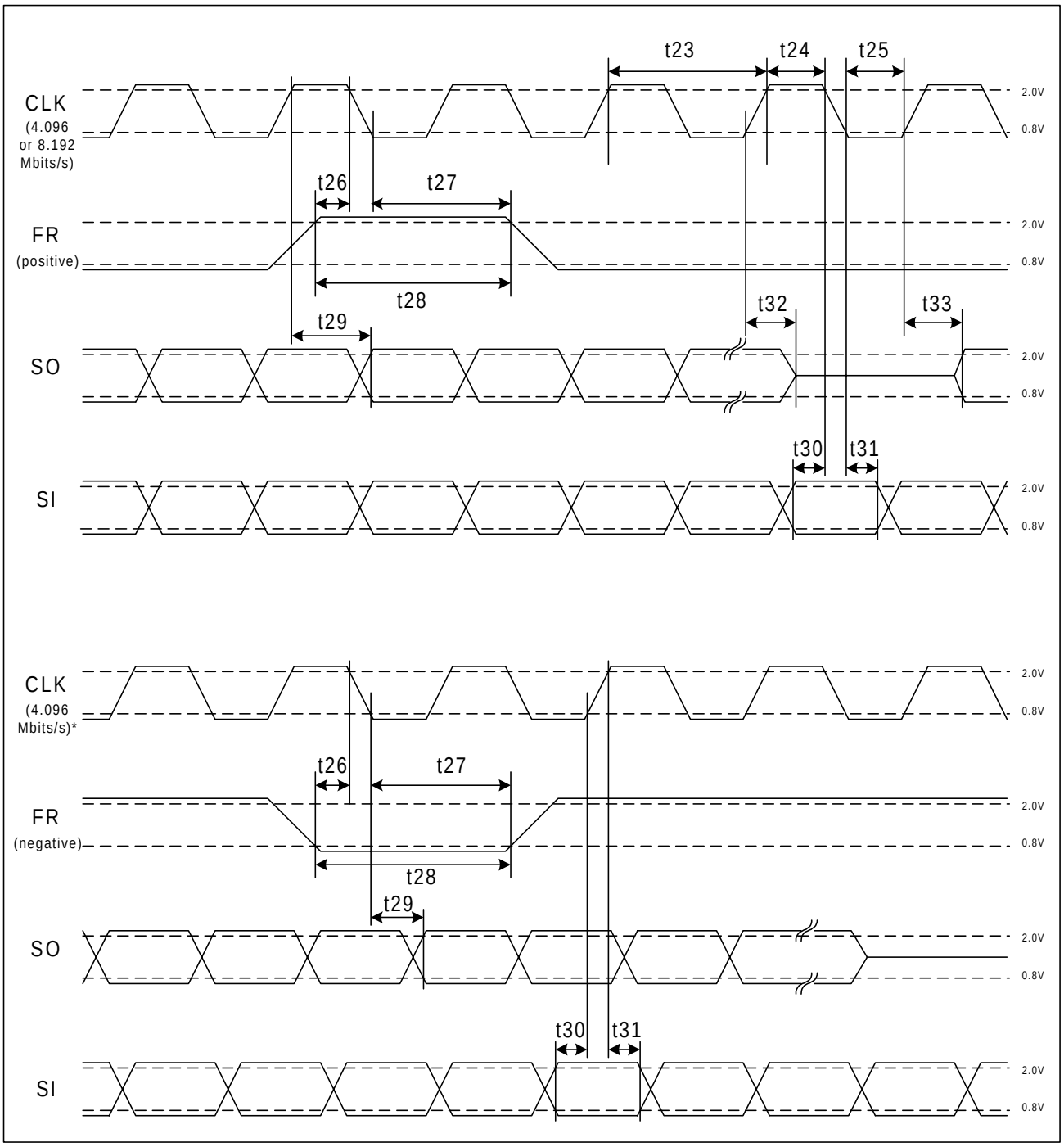


Figure-18. Serial Interface Timing at 4.096 and 8.192Mbits/s

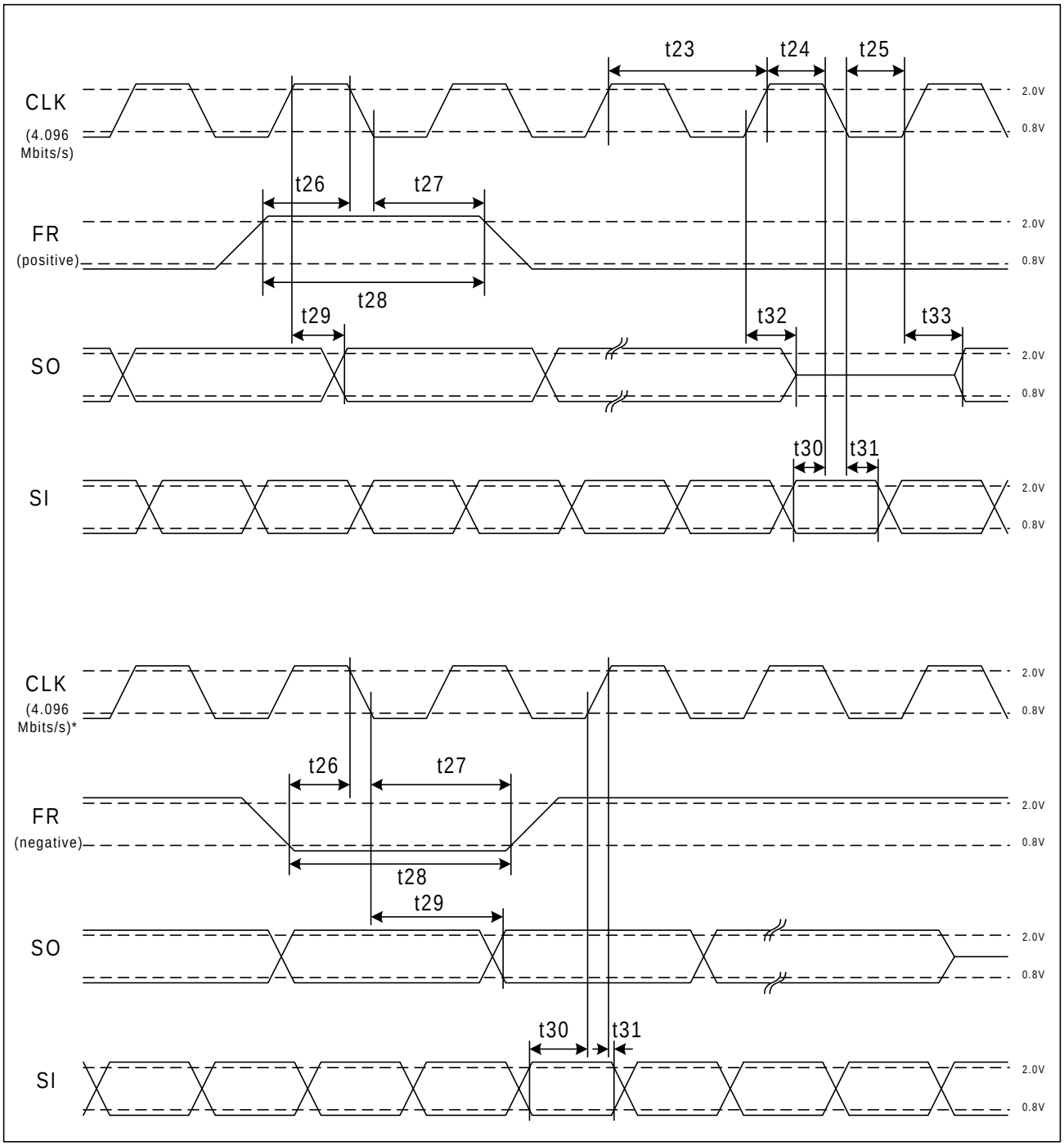


Figure-19. Rate Conversion Mode (4.096 to 2.048Mbits/s)

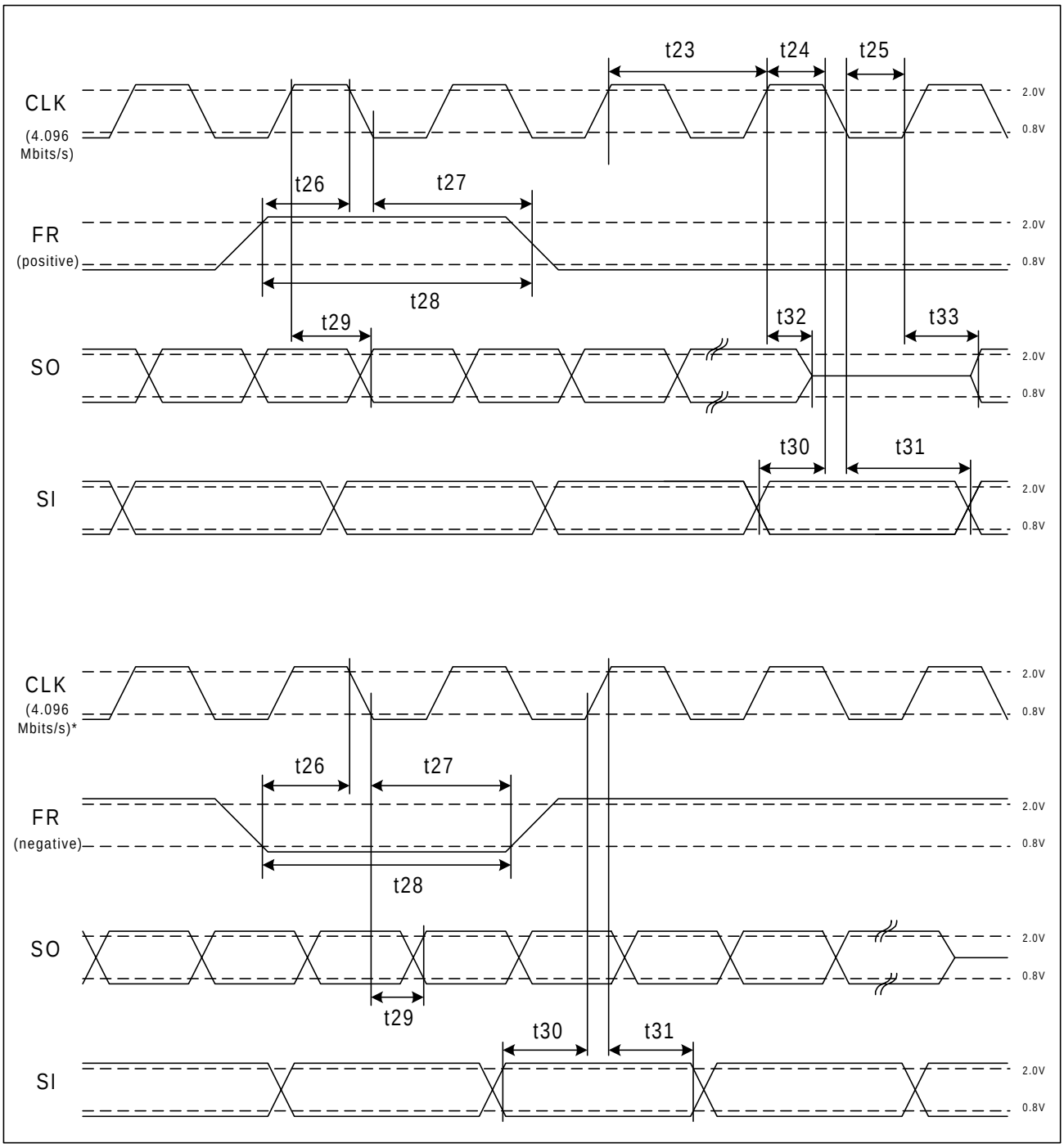


Figure-20. Rate Conversion Mode (2.048 to 4.096Mbits/s)

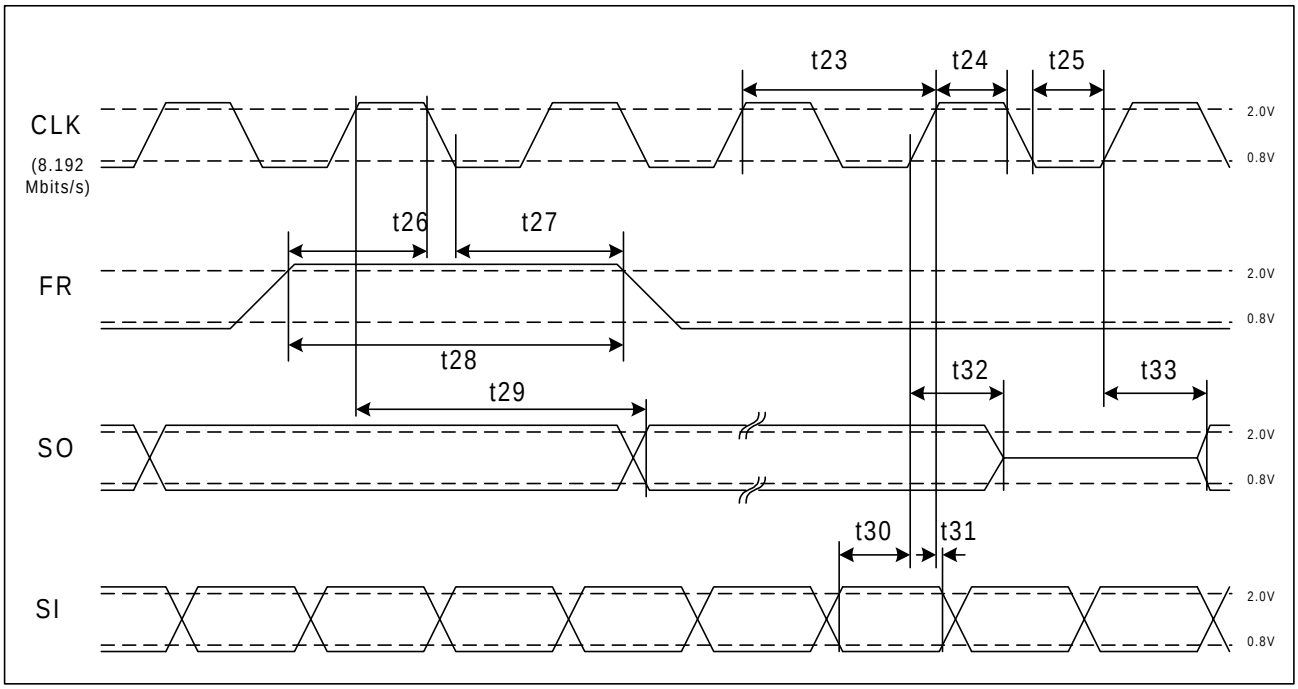


Figure-21. Rate Conversion Mode (8.192 to 2.048Mbits/s)

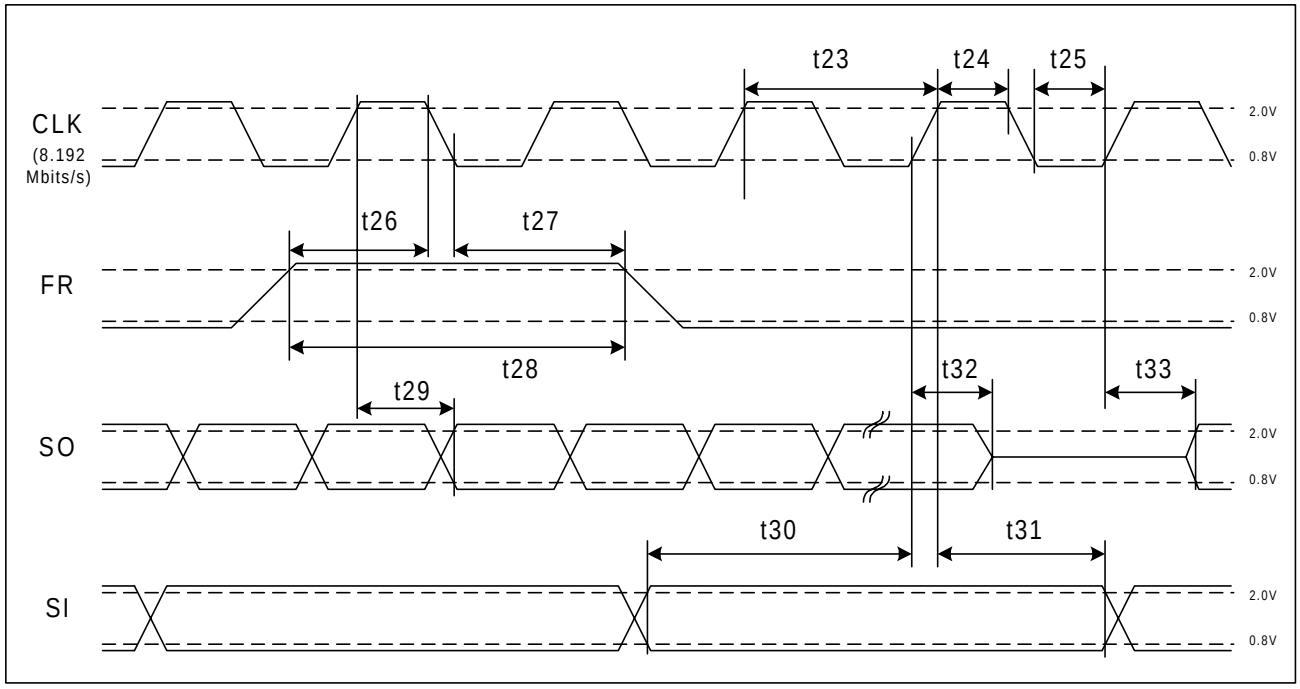


Figure-22. Rate Conversion Mode (2.048 to 8.192Mbits/s)

AC Electrical Characteristics - Intel/National - HPC Multiplexed Bus Mode

Par-meter	Description		Min	Typ*	Max	Units	Test Conditions
t35	ALE Signal Width		20			ns	
t36	Address Setup from ALE Falling		8			ns	
t37	Address Hold from ALE Falling		9			ns	
t38	$\overline{CS}$ Hold after $\overline{RD}$/$\overline{WR}$		0			ns	
t39	$\overline{CS}$ Setup from $\overline{RD}$		0			ns	
t40	$\overline{RD}$ Active after ALE Falling		9			ns	
t41	$\overline{RD}$ Signal Width(fast read)			80		ns	
t42	Data Hold after $\overline{RD}$		10	50	90	ns	R_L=1KΩ**, C_L=150pF
t43	$\overline{CS}$ Setup from $\overline{WR}$		0			ns	
t44	Valid Data Delay on Write(slow write)				122	ns	
t45	Data Setup from $\overline{WR}$(fast write)					ns	
t46	$\overline{WR}$ Delay after ALE Falling		10			ns	
t47	$\overline{WR}$ Signal Width(fast write)			90		ns	
t48	Data Hold after $\overline{WR}$		8			ns	
t49	Data Setup from $\overline{DTA}$ Low on Read		10			ns	C_L=150pF
t50	$\overline{DTA}$ Hold Time		10	60	110	ns	R_L=1KΩ**, C_L=150pF
t51	$\overline{DTA}$ Delay	Reading Data Memory		560	1220	ns	C_L=150pF
		Reading Connection Memory		300	730	ns	
		Writing Connection Memory		400	950	ns	
		Writing to Control & Mode Reg.		47	95	ns	
		Reading from Control & Mode Reg.		60	125	ns	

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

** High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

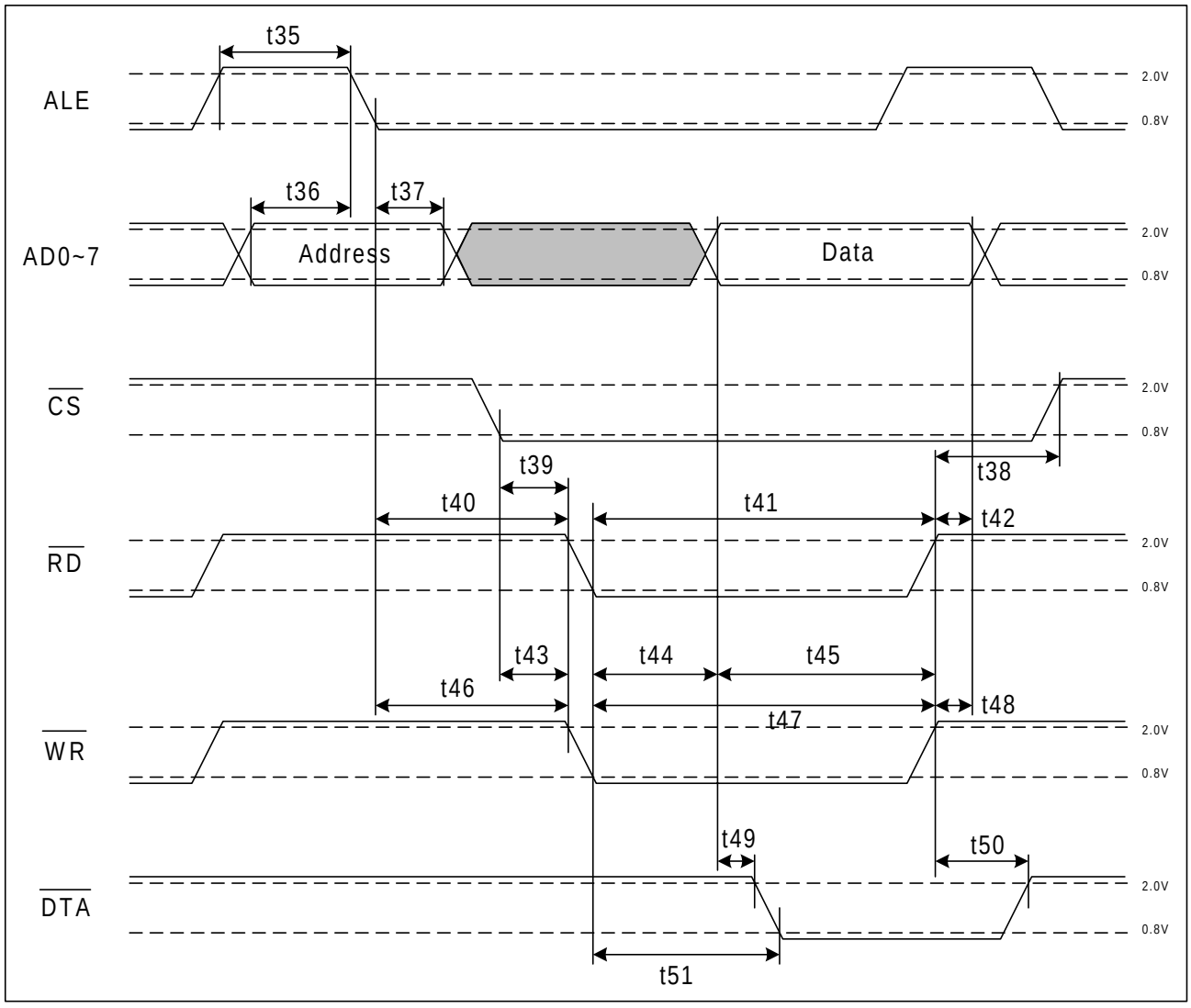


Figure-23.Intel/National Multiplexed Bus Timing

AC Electrical Characteristics – Motorola Multiplexed Bus Mode

Par-meter	Description		Min	Typ*	Max	Units	Test Conditions
t52	R/$\overline{W}$ Setup from DS Rising		60			ns	
t53	R/$\overline{W}$ Hold after DS Falling		9			ns	
t54	AS Signal Width		80			ns	
t55	DS Delay after AS falling		10			ns	
t56	Address Setup from AS Falling		8			ns	
t57	Address Hold from AS Falling		9			ns	
t58	Valid Data Delay on Write (slow write)				122	ns	
t59	Data Setup from DS (fast write)		25			ns	
t60	Data Hold after Write		8			ns	
t61	Data Hold after Read		10	50	90	ns	R_L=1KΩ**, C_L=150pF
t62	$\overline{CS}$ Setup from DS Rising		0			ns	
t63	$\overline{CS}$ Hold after DS Falling		0			ns	
t64	Data Setup from $\overline{DTA}$ Low on Read		10			ns	C_L=150pF
t65	$\overline{DTA}$ Hold Time		10	60	110	ns	R_L=1KΩ**, C_L=150pF
t66	$\overline{DTA}$ Delay	Reading Data Memory		560	1220	ns	C_L=150pF
		Reading Connection Memory		300	730	ns	
		Writing Connection Memory		400	950	ns	
		Writing to Control & Mode Reg.		47	95	ns	
		Reading from Control & Mode Reg.		73	125	ns	

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

** High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

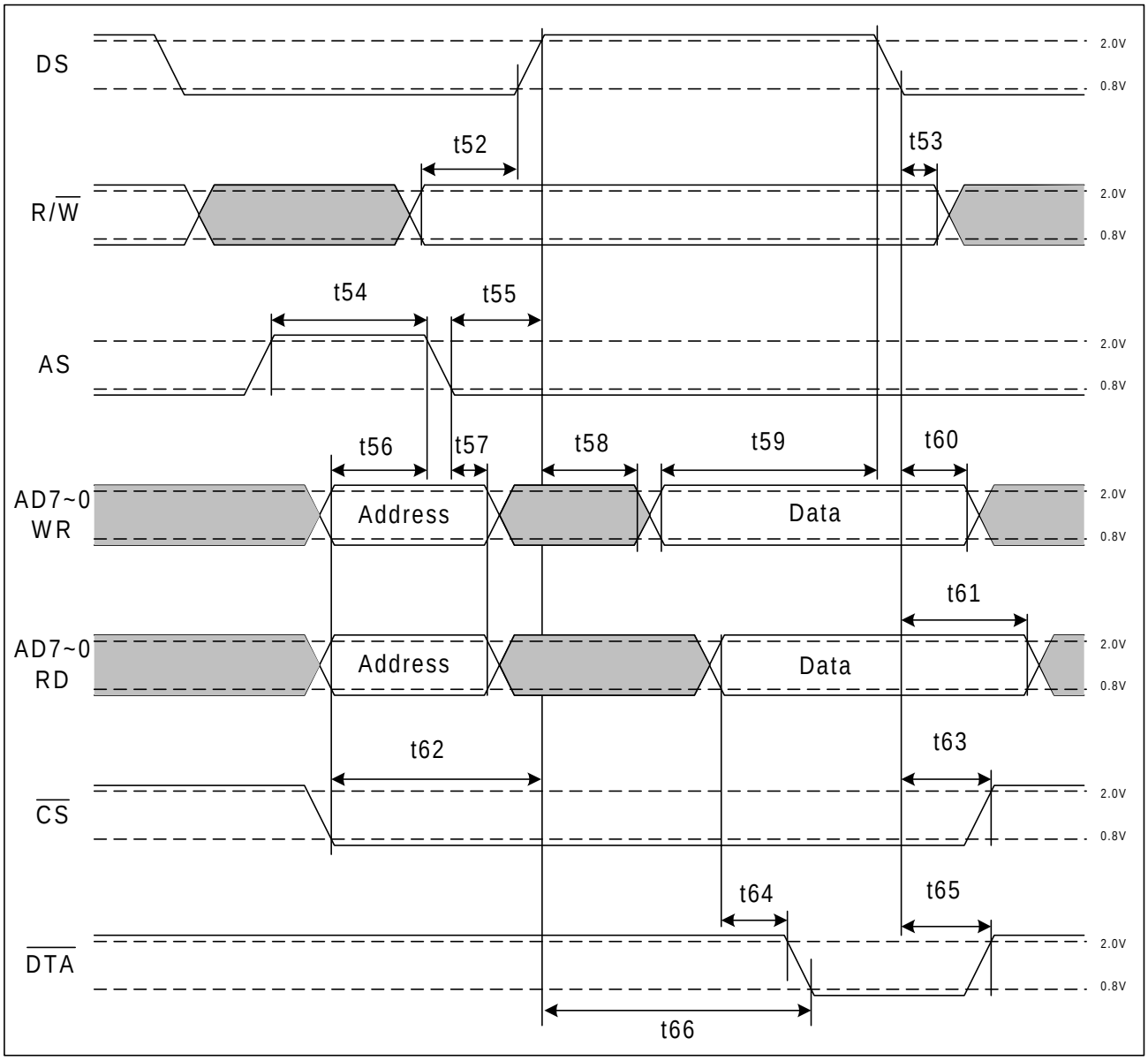


Figure-24. Motorola Multiplexed Bus Timing

AC Electrical Characteristics – Motorola Non-Multiplexed Bus Mode

Par-meter	Description		Min	Typ*	Max	Units	Test Conditions
t67	$\overline{CS}$ Setup from DS Rising		0			ns	
t68	$\overline{CS}$ Hold after DS Falling		0			ns	
t69	R/$\overline{W}$ Setup from DS Rising		30			ns	
t70	R/$\overline{W}$ Hold after DS Falling		5			ns	
t71	Address Setup from DS Rising		5			ns	
t72	Address Hold after DS Falling		5			ns	
t73	Data Hold on Read		10	50	90	ns	R_L=1KΩ**, C_L=150pF
t74	Valid Data Delay on Write (slow write)				122	ns	
t75	Data Setup on Write (fast write)		20			ns	
t76	Data Hold on Write		8			ns	
t77	Data Setup from $\overline{DTA}$ Low on Read		10			ns	C_L=150pF
t78	$\overline{DTA}$ Hold Time		10	60	110	ns	R_L=1KΩ**, C_L=150pF
t79	$\overline{DTA}$ Delay	Reading Data Memory		560	1220	ns	C_L=150pF
		Reading Connection Memory		300	730	ns	
		Writing Connection Memory		400	950	ns	
		Writing to Control & Mode Reg.		47	95	ns	
		Reading from Control & Mode Reg.		70	155	ns	

* Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

** High impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

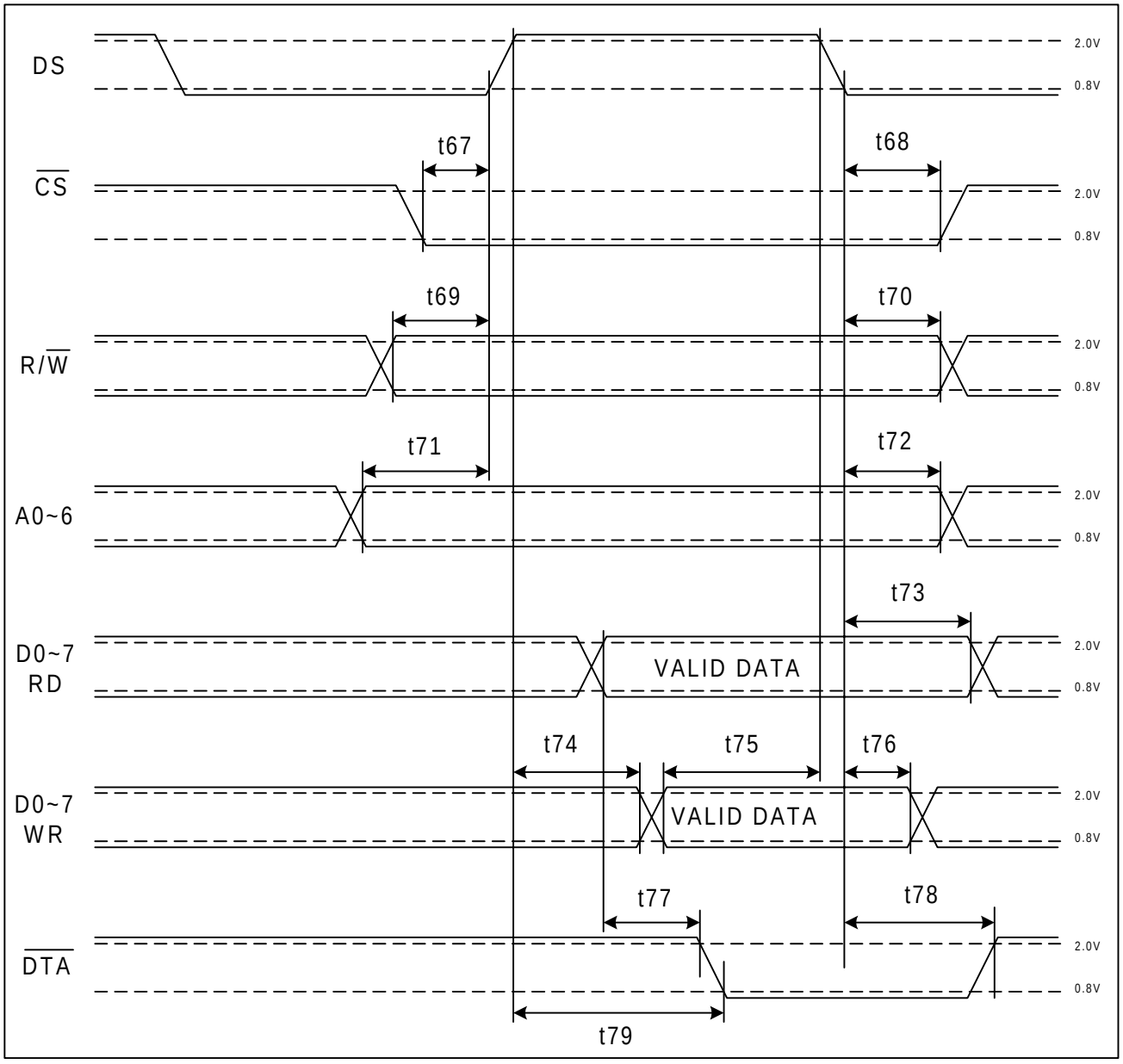


Figure-25. Motorola Non-Multiplexed Bus Timing

Physical Dimensions in Millimeters

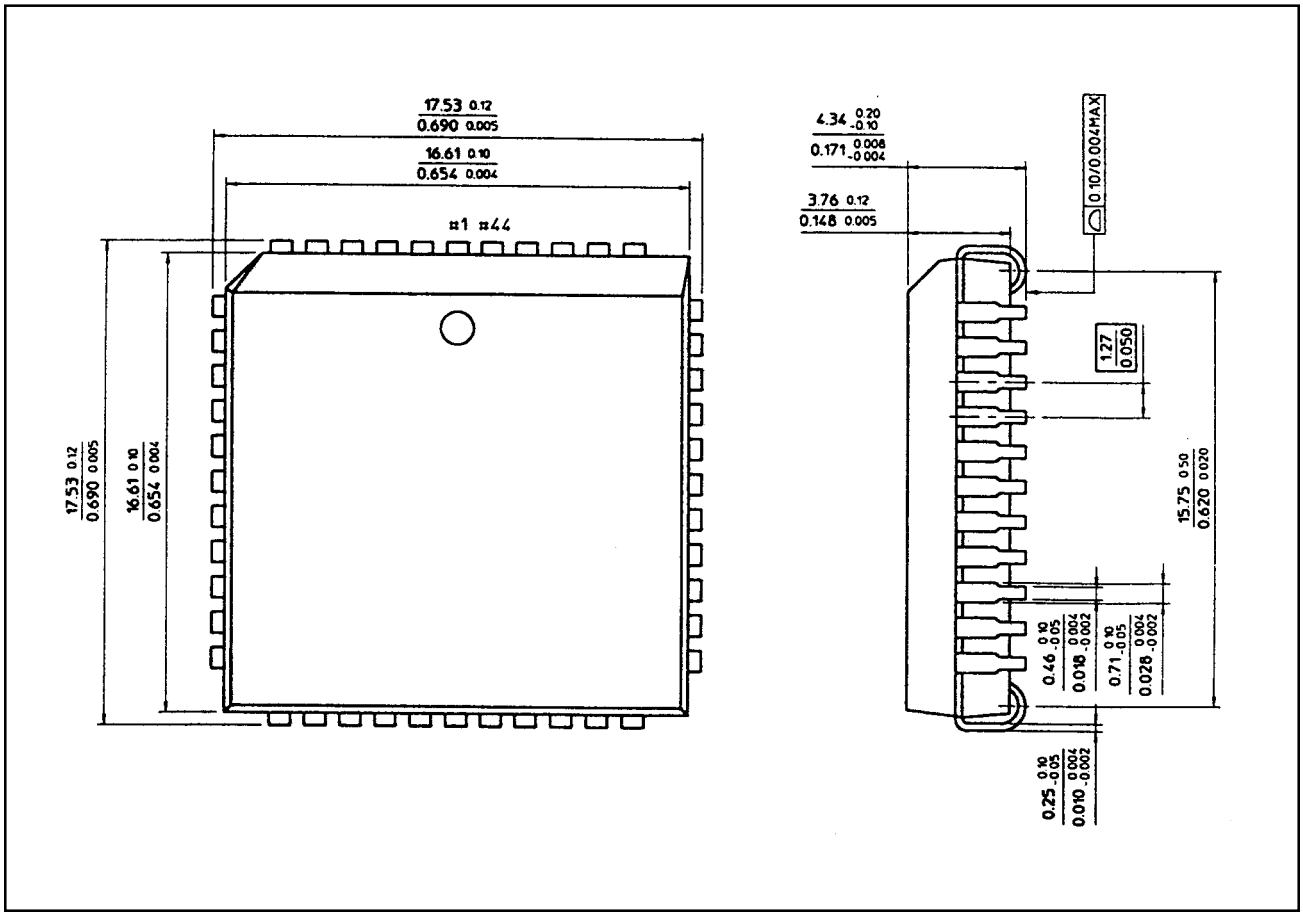


Figure-26. NW1507-XL 44-pin PLCC Package Diagram

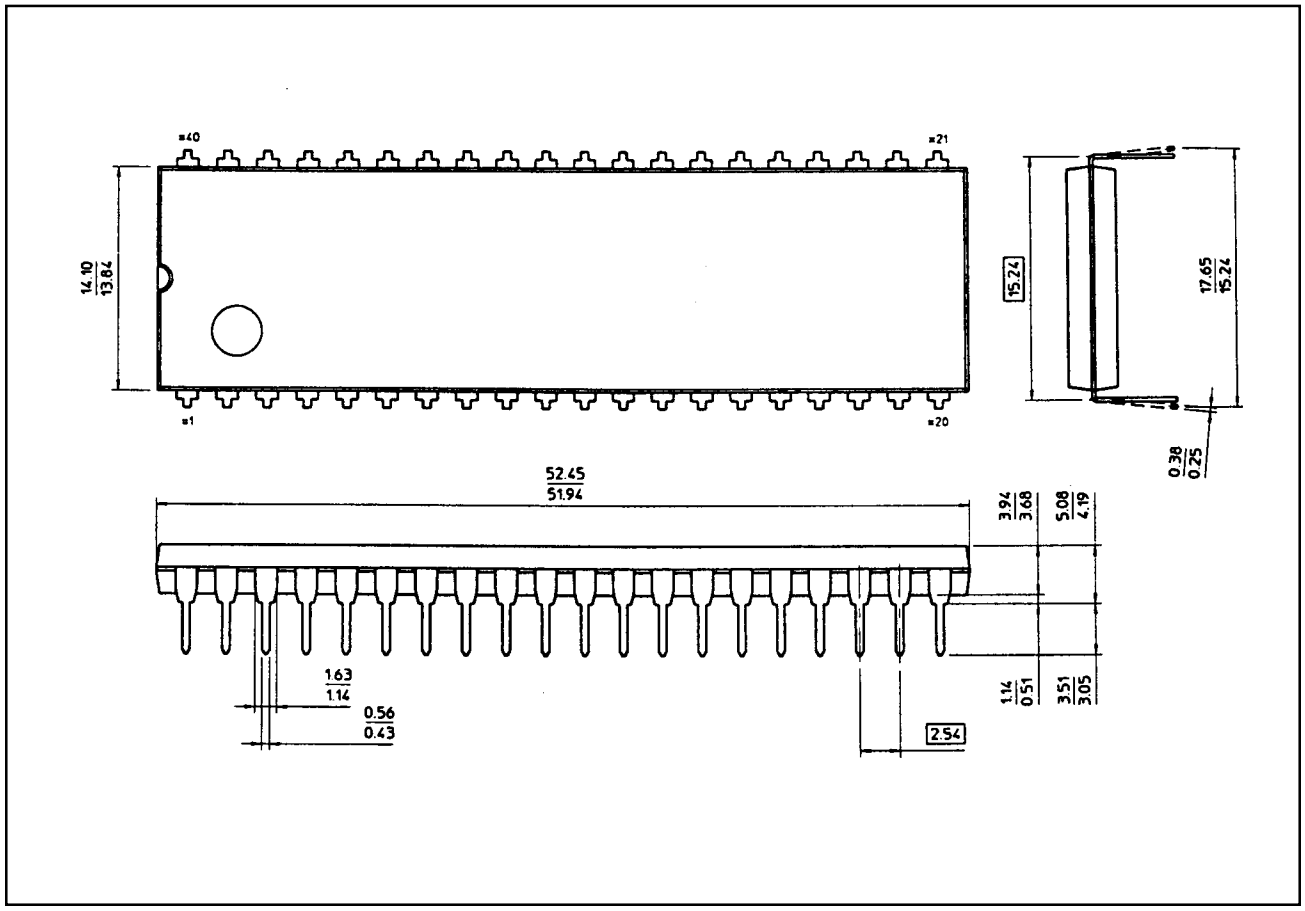


Figure-27. NW1507-XD 40-pin PDIP Package Diagram