NW1501
Time Division Switch Matrix

Data Sheet May 2000 (Ver 2.1)

Features

- 8 line × 32-channel inputs
- 8 line × 32-channel outputs
- 256 non-blocking switch channels
- ST-BUS™ compatible
- Microprocessor control interface
- Tri-state serial outputs
- +5 V single power supply
- Low power consumption (30 mW Typ.)
- Operating temperature range:
  -40 °C to +85 °C
- Packages available:
  NW1501-XL 44-pin PLCC
  NW1501-XD 40-pin PDIP
  (where X is the revision ID)

Note: ST-BUS™ is a trade mark of Mitel Corp.

Description

The NW1501 is a single-chip, 256-channel time division switch matrix. The device has 8 serial inputs and 8 serial outputs, each consisting of 32 channels at 64 kbits/s data rate. Information in any of the 256 ST-BUS™ input channels can be switched to any of the 256 output channels.

The NW1501 can be used for the switching of digitized voice, digitized video and data in telecommunication applications such as Private Branch Exchange (PBX), Central Office Switch and Cellular Base Station.

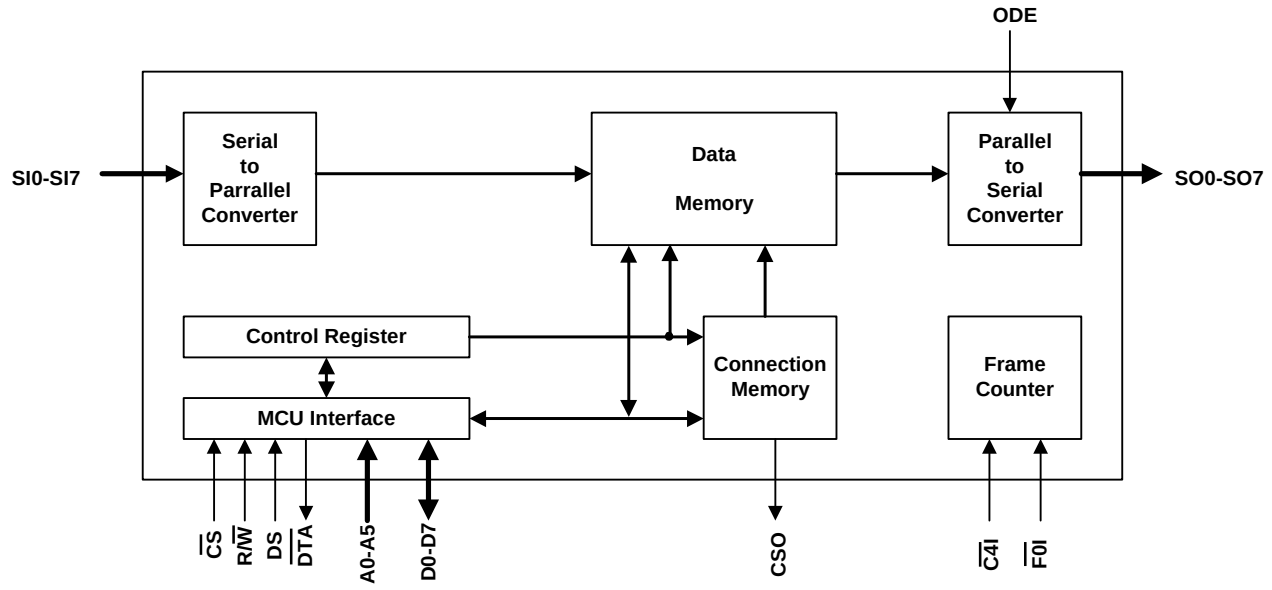

Figure-1. Block Diagram

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Pin Connection

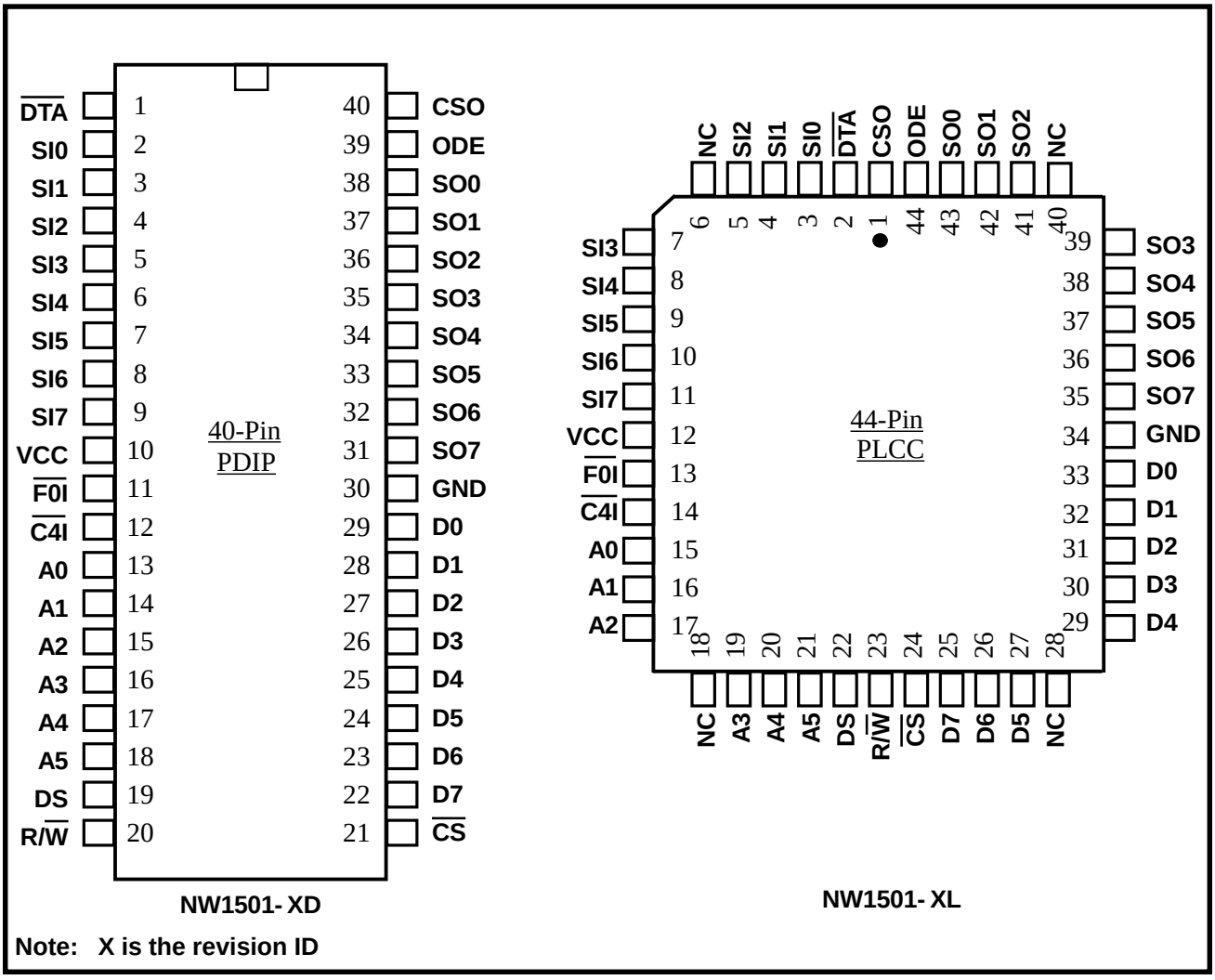


Figure-2. Pin Connection

Pin Description

Name	Type	Pin Number 40 DIP	Pin Number 44 PLCC	Description
$\overline{DTA}$	O	1	2	**Data Acknowledgment (Open Drain Output).** This is a pin on the microprocessor interface. When this pin is pulled low, it means that the chip has processed the data. An external 1 kΩ pull-up resistor is recommended.
SI0	I	2	3	**Serial ST-BUS™ Input.** These are inputs for the 2.048Mbit/s ST-BUS™ input streams.
SI1		3	4	
SI2		4	5	
SI3		5	7	
SI4		6	8	

Name	Type	Pin Number 40 DIP	Pin Number 44 PLCC	Description
SI5	I	7	9	**Serial ST-BUS™ Input.**
SI6		8	10	These are inputs for the 2.048Mbit/s ST-BUS™ data streams.
SI7		9	11	
VCC	--	10	12	**Power Supply of +5V.**
$\overline{F0I}$	I	11	13	**Framing 0-Type Input.** This is a frame synchronization input pulse for the serial input or output streams. Low level of this pin causes internal counter to reset at the next falling edge of $\overline{C4I}$ input.
$\overline{C4I}$	I	12	14	**4.096 MHz Clock Input.**
A0	I	13	15	**Address Bus Inputs.**
A1		14	16	These are inputs for the address lines on the microprocessor interface.
A2		15	17	
A3		16	19	
A4		17	20	
A5		18	21	
DS	I	19	22	**Data Strobe Input.** Active high data strobe on the microprocessor interface.
R/$\overline{W}$	I	20	23	**Read/Write Select.** Signal on the microprocessor interface, high for read, low for write.
$\overline{CS}$	I	21	24	**Chip Select.** Active low chip select on the microprocessor interface.
D7	I/O	22	25	**Data Bus of Tri-state I/O.**
D6		23	26	These are microprocessor interface I/O.
D5		24	27	
D4		25	29	
D3		26	30	
D2		27	31	
D1		28	32	
D0		29	33	
GND	--	30	34	**Ground.**
SO7	O	31	35	**Serial ST-BUS™ output.** .
SO6		32	36	These are outputs for the 2.048Mbit/s ST-BUS™ data streams.
SO5		33	37	
SO4		34	38	
SO3		35	39	
SO2		36	41	
SO1		37	42	
SO0		38	43	
ODE	I	39	44	**Output Drive Enable.** This is the control input which enables the output data bus. If high, SO7-0 output drivers function normally. If low, output drivers go into high impedance state. (See Operation Control Section on page 5 for reference)
CSO	O	40	1	**Control ST-BUS™ Output.** The 2.048 Mbit/s output contains 256 bits per frame. Each frame contains the values of bit 1 of Connection Memory High Section in the 256 locations.
NC			6	**No Connection.**
			18	
			28	
			40	

Functional Description

ST-BUS™ architecture is designed for software controlled digital switch and interprocessor communications. ST-BUS™ operates at the rate of 2.048 Mbit/s. The serial data stream contains 32 channels at 64 kbit/s rate. Since there are 8 bits in each PCM sample, the resulting frame rate is 8 kHz, i.e. the width of each frame is 125 µs.

The NW1501 has the ability to switch data from any input ST-BUS™ channels to any output ST-BUS™ channels. Meanwhile, it allows the controlling microprocessor to read from channels on ST-BUS™ inputs .

Hardware Description

The NW1501 consists of the following major blocks:

1. Data Memory is used to store byte-wide data converted from input serial data stream. Each location in Data Memory is associated with a specific input stream and channel address. Data Memory can also be read by the controlling microprocessor via MCU Interface.

2. Connection Memory is used to store the switching configuration originated from the microprocessor. Each location of the Connection Memory is associated with a specific output stream and channel, and is divided into low and high sections: **Connection Memory Low section (CML)** and **Connection Memory High section (CMH)**. The CML stores the Data Memory address of output data for switching. CMH can control if an individual output channel is placed into the high-impedance state. This is useful if NW1501 arrays are used to construct a larger switch matrix.

3**. MCU Interface and Control Register** are connected with both Data Memory and Connection Memory. The MCU Interface receives the control data, while the Control Register performs the control function. The MCU Interface consists of a bidirectional data bus (D7-D0), an address bus (A5-A0) and four control signals : $\overline{CS}$ (Chip Select), R/$\overline{W}$ (Read/Write Select), DS (Data Strobe) and $\overline{DTA}$ (Data Acknowledgment). The Control Register can be written to or read from via the MCU Interface. It enables the device to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low.

4. **Frame Counter** derives all ST-BUS™ timing from the two input signals $\overline{C4I}$ and $\overline{F0I}$.

Microprocessor can write to the device or read from the device. By writing, it can establish switching connections between input and output channels. By reading, it can receive information from input channels or check which switching connections have already been established.

Software Control Description

Data from a particular input channel is switched to the chosen output channel in a non-blocking fashion. Until rewritten by the microprocessor, the same information is output onto the channel once every frame. Data on the input channels can be read by microprocessor.

Input channel information is first converted from serial form into parallel form. After the conversion, the byte wide data is stored in the corresponding memory location in a fixed sequence. Data Memory of the NW1501 has a capacity of 256 bytes (one byte of Data Memory per input channel). It can load information automatically only from inputs, and can not be written to via the microprocessor port.

Information stored in Data Memory can be read in two ways:

a). Through the microprocessor port. In this case, the address of a location in Data Memory is formed by Control register bits CR2-CR0 and external address bits A4-A0;

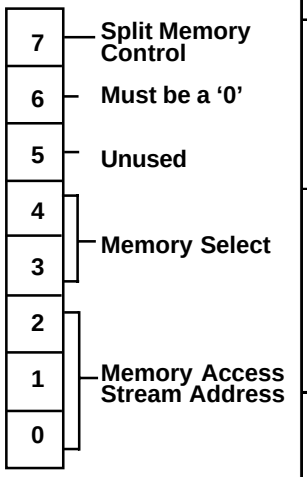
b). By a sequence that places Data Memory contents into an ST-BUS™ output channel. The address for Data Memory is formed by the contents of the CML bytes associated with the output channel.

The address lines A5-A0 on the MCU Interface access the Control Register directly, or access memory locations in Data Memory, CMH or CML of the device. If A5 is high, then the address line A4-A0 select the memory location corresponding to channel 0-31 of the memory and stream selected in the Control Register. If A5 is low, then the Control Register is addressed regardless of the rest address lines.

Control Register (see Fig. 3) can be read or written by the microprocessor port. It is accessed only when A5 is low. CR4 and CR3 determine which of the memory blocks is being accessed. CR2 - CR0 determine which portion of the memory block is selected for subsequent operation. Each memory block portion selected is 32 bytes deep, corresponding to the 32 channels in one stream. A4-A0 determine which byte in the 32 byte segment is accessed by the microprocessor at any one time. All switch operation is determined by CMH. CR7 can split the memory. When it is a '1', the device is in split mode. In this mode, all microprocessor reads are from

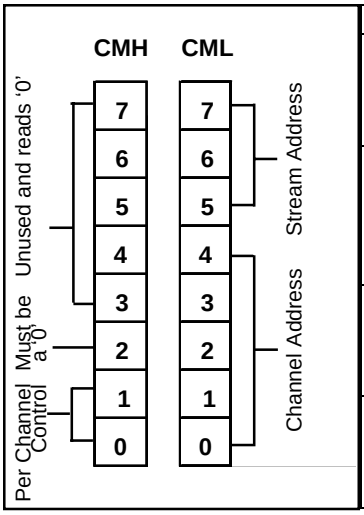
Data Memory, while all microprocessor writes are to the CML. If CR7 is set to a '0', then memory block selection is determined by CR4 and CR3. CR5 is unused and CR6 must be set to '0'. It's noted that CR4 and CR3 should never be set to '00'.

Connection Memory Low section (see Fig. 4) has a capacity of 256 bytes. Each byte in CML is associated with an output channel. CML can be written only from microprocessor port, but can be read out as switch address:



BIT	Name and Description
CR7	**Split Memory Control** When '1', until Control Register is accessed again, all subsequent reads are from the Data Memory, while writes are to the CML. When '0', Memory Select bit specifies the memory for subsequent operation.
CR4-3	**Memory Select** "00" - Not to be used "01" - For selection of Data Memory (Read only via the microprocessor port) "10" - For selection of Connection Memory Low "11" - For selection of Connection Memory High
CR2-0	**Memory Access Stream Address** These bits expressed in binary notation indicate the input or output streams corresponding to the subsection of memory made accessible for subsequent operations.

Figure-3. Control Register Bits



BIT	Description
CMH1	**CSO Bit** This bit outputs on CSO pin a channel earlier. CSO bit of stream 0 is output first.
CMH0	**Channel Output Enable** When '0', the individual channel on individual stream is made high-impedance. When '1', if ODE pin is high, the output driver of the location's channel and stream is enabled.
CML7-5	**Stream Address** The contents of these bits mean the number of ST-BUS™ stream for the source of connection. Bit 7 is the most significant bit.
CML4-0	**Channel Address** The contents of these bits mean the number of varies of channels source from channel 0 to channel 31. Bit 4 is the most significant bit.

Figure-4. Connection Memory Bits

When the microprocessor is writing to or reading from CML, the address of the location is formed by CR2-CR0, and A4-A0. The contents of the CML are used once every frame.

Connection Memory High (see Fig. 4) section has the same address range, method of addressing as CML. CMH can be read from and written to by the microprocessor. Each byte in CMH is associated with the same output channel as the related byte in the CML.

CMH1 controls the state of the bit on the CSO output that is associated with that particular CMH location and channel. It outputs on CSO pin once every frame. This output pin contains 8 bits (CMH1 of stream 0-7, stream 0 is output first), corresponding to the channel position every 16 clock cycles (one channel time). Considering delay in external control circuitry, CMH1 outputs appear one channel time before the corresponding channel on the ST-BUS™ streams (see Fig.8)

CMH1 can be used in synchronization of the microprocessor with the device. CMH0 is the output enable bit. When it is '0', the output channel location is placed into a high impedance state. When it is a '1', the output channel driver is turned on.

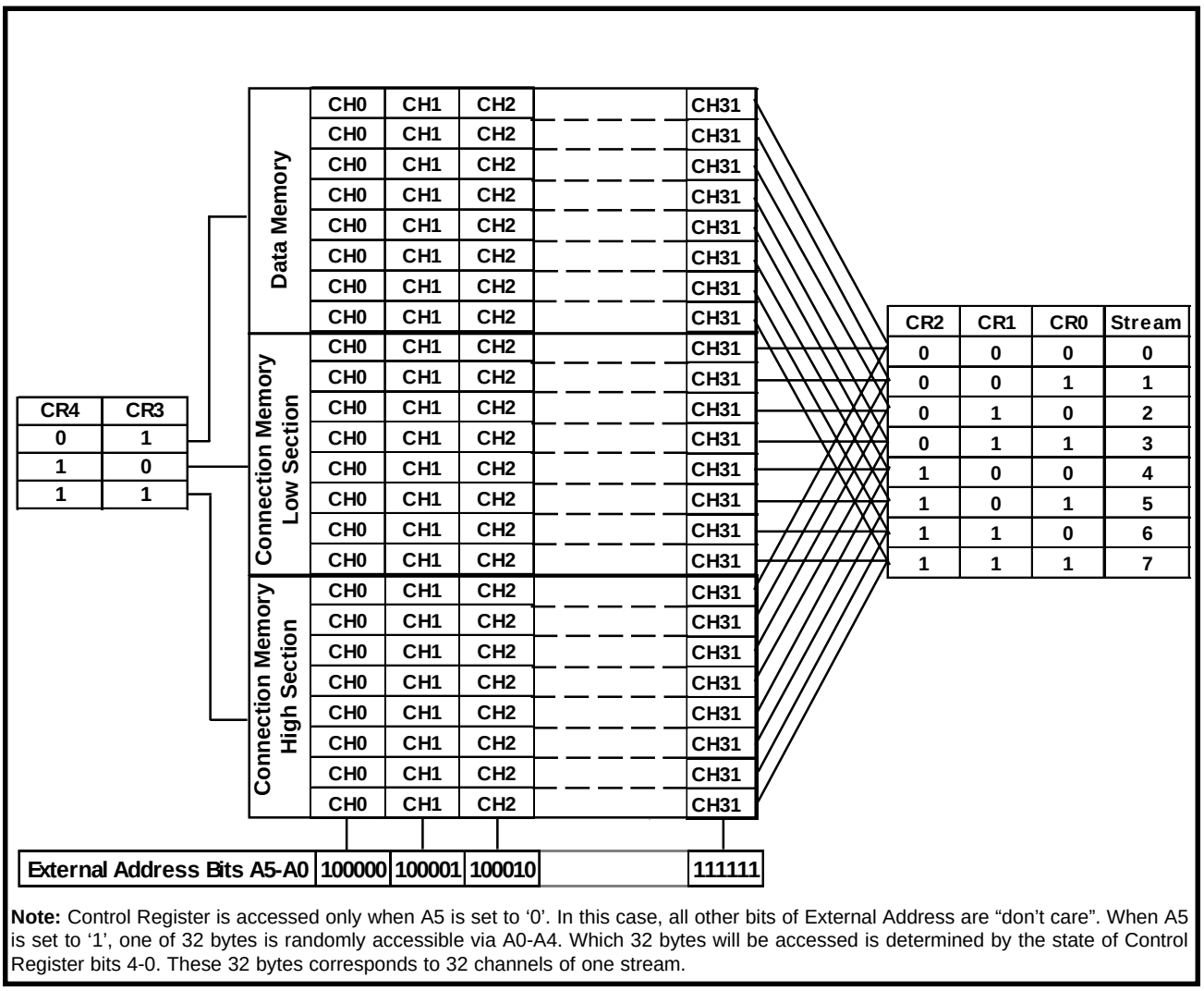
An input pin named ODE plays a key role in the operation of NW1501. If it is high, then a '1' of CMH0 enables the output driver of the corresponding output stream
and channel. If ODE pin is low, all the serial ST-BUS™ outputs go to high-impedance state.

We will clarify how the Control Register, memory blocks and the external address bits work together (see Fig. 5) with the following example.

In this example, Channel 24 on Input Stream 2 (SI2) should be switched to Channel 3 on Output Stream 7 (SO7). First, the two Connection Memory locations corresponding to Channel 3 on SO7 have to be accessed. CML must contain the Data Memory address of the source channel - Channel 24 on SI2. CMH specifies the mode of Channel 3 on SO7 and whether it is in a high impedance state. To access CML, CR4 and CR3 must be set to '10'. To access the 32 byte segments corresponding to SO7, CR2-CR0 must be set to '111'. CR7 can be either a '1' or a '0' for writes (if a '0',then CR4 and CR3 must be set properly). For reads, CR7 must be a '0'. Note that if it were an '1', then CR4 and CR3 would have been inconsequential and the read would have been from Data Memory. Finally to access channel 3, A4-A0 must be set to '00011'.

The source of the information for Channel 3 on SO7 is Channel 24 on SI2. To indicate this, CML bytes must be written as '01011000'. The three most significant bits of this byte select the input stream, and the five least significant bits select the input channel on that stream.

To access CMH for the target output channel, CR4 and CR3 must be set to '11' and CR7 must be set to '0'. CR2, CR1 and CR0 need not be changed, and the same setting of A4-A0 must be used. CMH0 must be set to a '1' to ensure that the output channel is not in a high impedance state.



Note: Control Register is accessed only when A5 is set to '0'. In this case, all other bits of External Address are "don't care". When A5 is set to '1', one of 32 bytes is randomly accessible via A0-A4. Which 32 bytes will be accessed is determined by the state of Control Register bits 4-0. These 32 bytes corresponds to 32 channels of one stream.

Figure-5. Control Register, Data Memory, CMH,CML Operation Method

Application Information

The principal application of the NW1501 is:

Switching. The NW1501 provides non-blocking switching of 256 information channels. Each channel has a capacity of 64 kbit/s, and may carry data, digitized voice or video. The device can provide a communication path between any input channel and output channel of the NW1501 through ST-BUS™. Furthermore, it can construct larger switching matrices by putting its ST-BUS™ outputs into a high impedance state on a per channel basis.

Maximum Rating

Supply Voltage: -0.3 V to 7 V
Digital Input Voltage: -0.3 V to 7 V
Digital Output Voltage: -0.3 V to 7 V
Digital Output Current: ≤ 40 mA
Package Power Dissipation: ≤ 2 W
Storage Temperature: -65 °C to +150 °C

Recommended Operating Conditions

Operating Temperature: -40 ° C to +85 ° C
Power Supply: 4.75 V to 5.25 V
Input Voltage: 0 V to VCC

DC Electrical Characteristics

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -10 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 5 mA
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.6	V	
I_{OH}	Output High Current	-10	-15		mA	V_{OH} = 2.4 V
I_{OL}	Output Low Current	5	10		mA	V_{OL} = 0.4 V
I_{I1}	Input Leakage	-10		10	µ A	V_I between V_{CC} and GND
I_{I2}	Input Leakage 2*		250	320	µ A	V_I between V_{CC} and GND
I_{OZ}	High Impedance Leakage	-10		10	µ A	V_O between V_{CC} and GND
I_{CC}	Supply Current		6	14	mA	All outputs unloaded
C_O	Output Pin Capacitance		8		pF	
C_I	Input Pin Capacitance		8		pF	

Note *: *This input leakage is for STI4-7, with pull-down resistors.*

AC Electrical Characteristics - Clock Timing

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t1	Clock Period	220	244	300	ns	
t2	Clock Width High	95	122	150	ns	
t3	Clock Width Low	110	122	150	ns	
t4	Clock Rise/Fall Time		20		ns	
t5	Frame Signal Width	60	244	50000	ns	
t6	Frame Signal Setup Time	20		200	ns	
t7	Frame Signal Hold Time	0.02		50	µ s	

Note: *Test can be in the conditions showed as Max. or Min., use appropriate value specified under Electrical Charateristics for the applicable device type. Contents of Connection Memory will not be lost if the clock stops. However, ST-BUS™ outputs go into the high impedance state.*

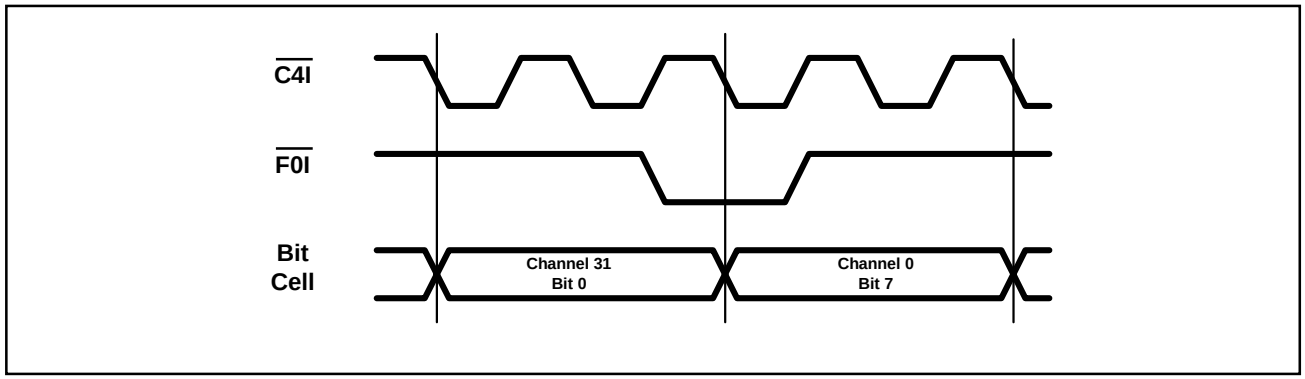


Figure-6. Frame Alignment

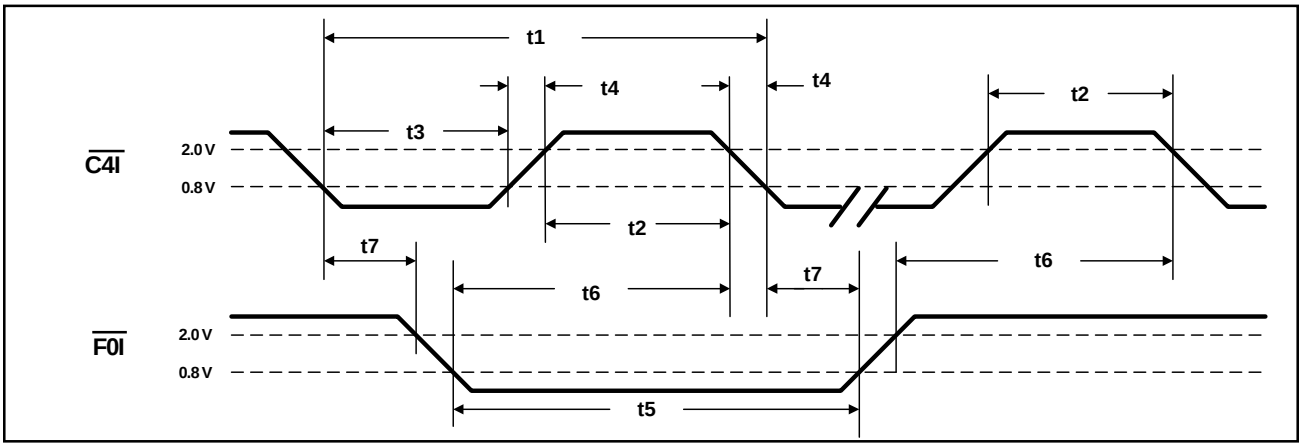


Figure-7. Clock Timing

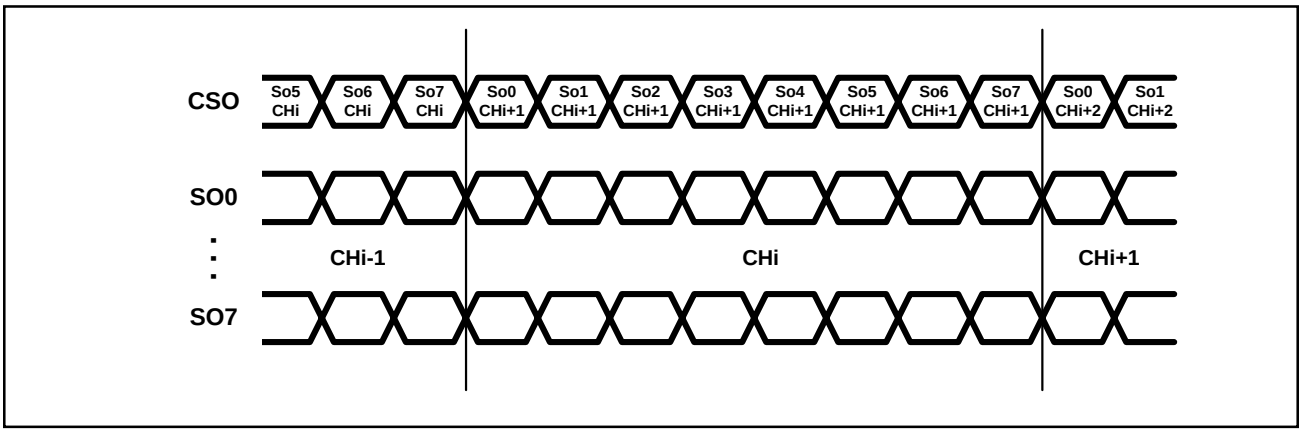


Figure-8. CSo Output Timing

AC Electrical Characteristics - Serial Streams

Parameter	Description	Min	Typ	Max	Units	Test Condition
t11	SO0-7 Delay-Active to High Z		50	80	ns	R_L = 1kΩ, C_L = 150 pF
t12	SO0-7 Delay-High Z to Active		60	125	ns	C_L = 150 pF
t13	SO0-7 Delay-Active to Active		65	125	ns	C_L = 150 pF
t14	SO0-7 Hold Time		45		ns	C_L = 150 pF
t15	Output Driver Enable Delay		45	125	ns	R_L = 1kΩ, C_L = 150 pF
t16	External Control Hold Time	0	50		ns	C_L = 150 pF
t17	External Control Delay		75	110	ns	C_L = 150 pF
t18	SI0-7 Setup Time		-40	-20	ns	
t19	SI0-7 Hold Time	90			ns	

** High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.*

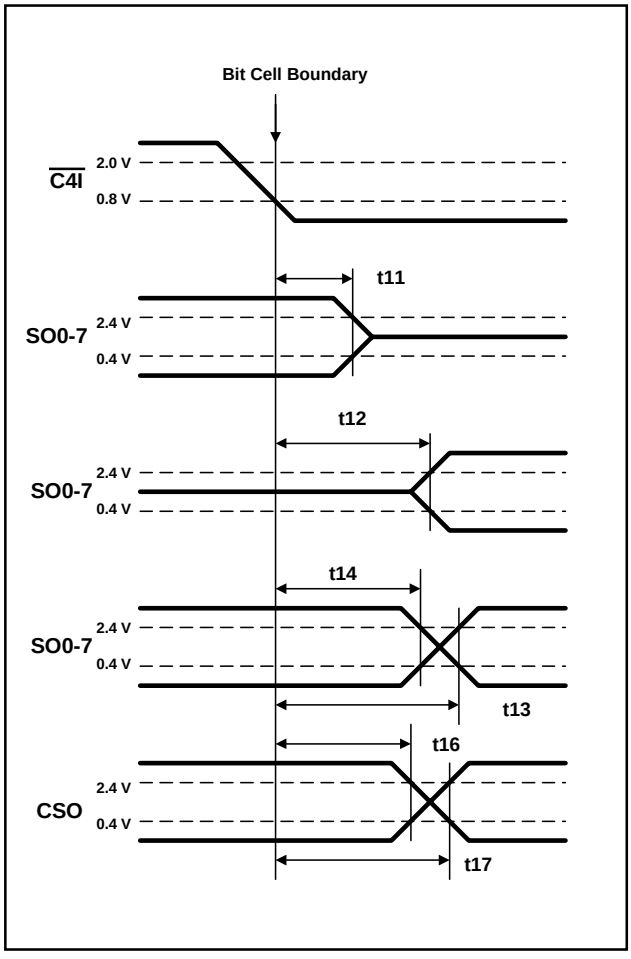


Figure-9. Serial Outputs and External Control

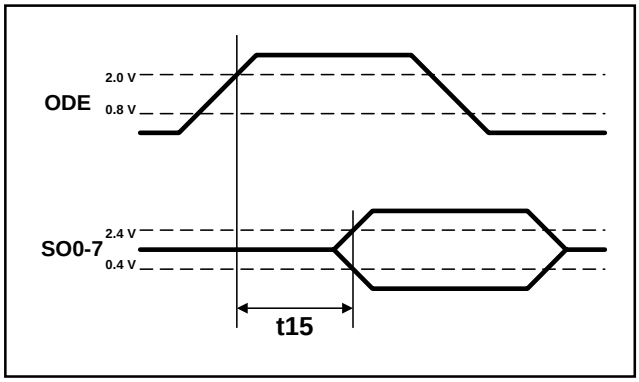


Figure-10. Output Driver Enable

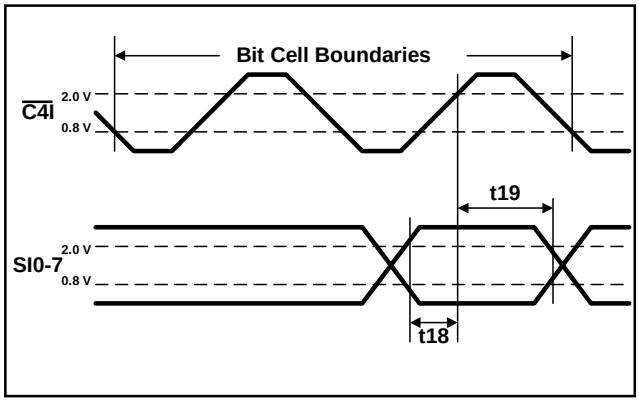


Figure-11. Serial Inputs of SI0-7

AC Electrical Characteristics - Processor Bus

Parameter	Description		Min	Typ	Max	Units	Test Condition
t21	Chip Select Setup Time		20	0		ns	
t22	Chip Select Hold Time		0			ns	
t23	Read/Write Setup Time		25	5		ns	
t24	Read/Write Hold Time		0			ns	
t25	Address Setup Time		25	5		ns	
t26	Address Hold Time		0			ns	
t27	Read Data Setup Time				1.2	cycles	$\overline{C4I}$ cycles#, C_L= 150 pF
t28	Read Data to High Z Delay			50	90	ns	R_L = 1kΩ, C_L = 150 pF
t29	Fast Write Data Setup Time**		20			ns	
t30	Slow Write Data Delay**				1.5	cycles	$\overline{C4I}$ cycles#, C_L= 150 pF
t31	Data Hold Time	Read	20			ns	R_L = 1kΩ, C_L = 150 pF
		Write	20	10		ns	
t32	Acknowledgement Delay	Fast**		40	100	ns	C_L = 150 pF
		Slow**	2.2		7.2	cycles	$\overline{C4I}$ cycles#, C_L= 150 pF
t33	Read Data to Active Delay		20		88	ns	
t34	Acknowledgement Hold Time		10	60	80	ns	R_L = 1kΩ, C_L = 150 pF

** High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.*
#Processor accesses are dependent on the $\overline{C4I}$ clock, so some timings are expressed as multiples of the $\overline{C4I}$ clock period.
*** Fast indicates only write for the control register, slow indicates read/write for the connection and data memory.*

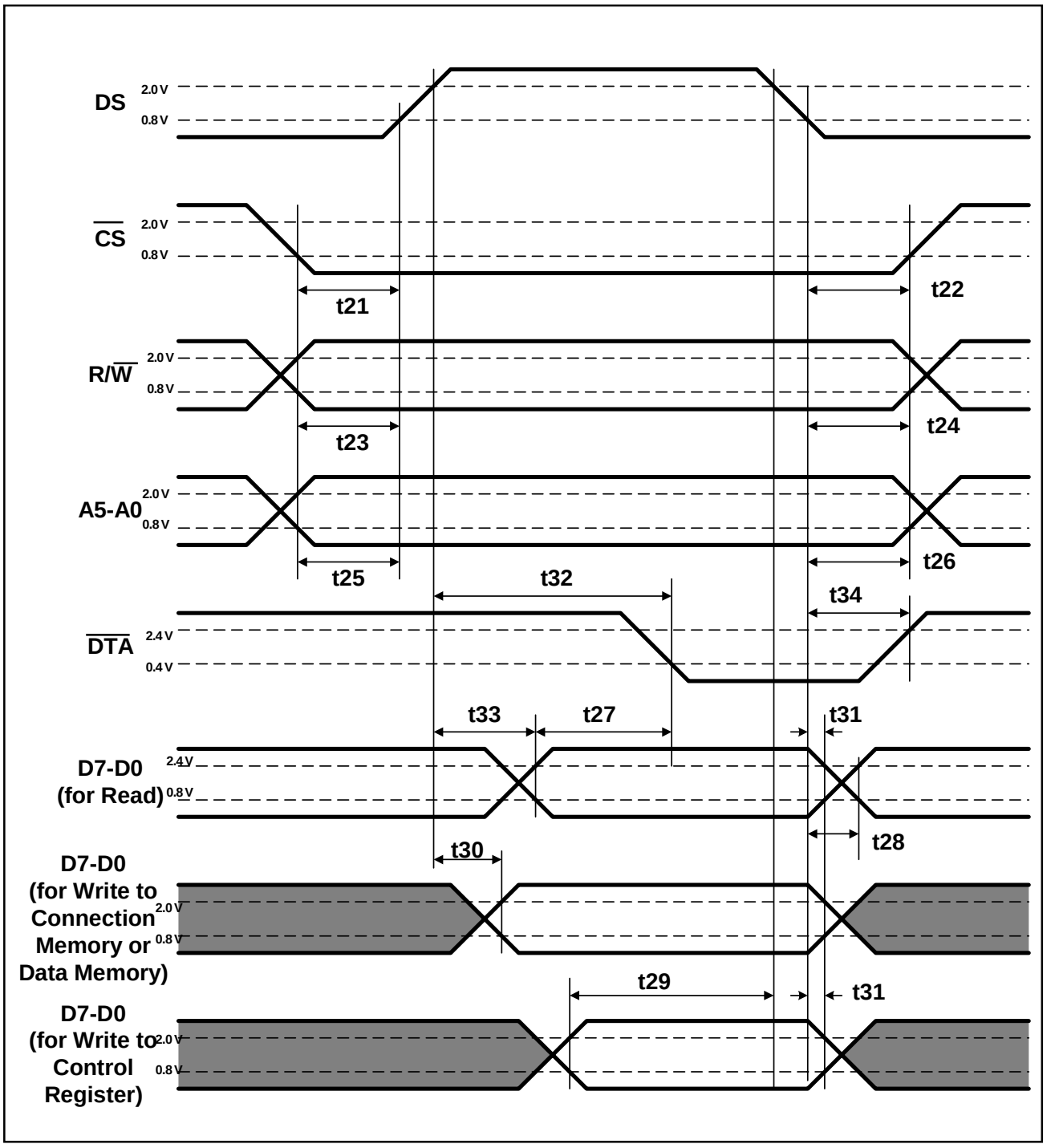


Figure-12. Processor Access Bus

Physical Dimensions in Millimeters

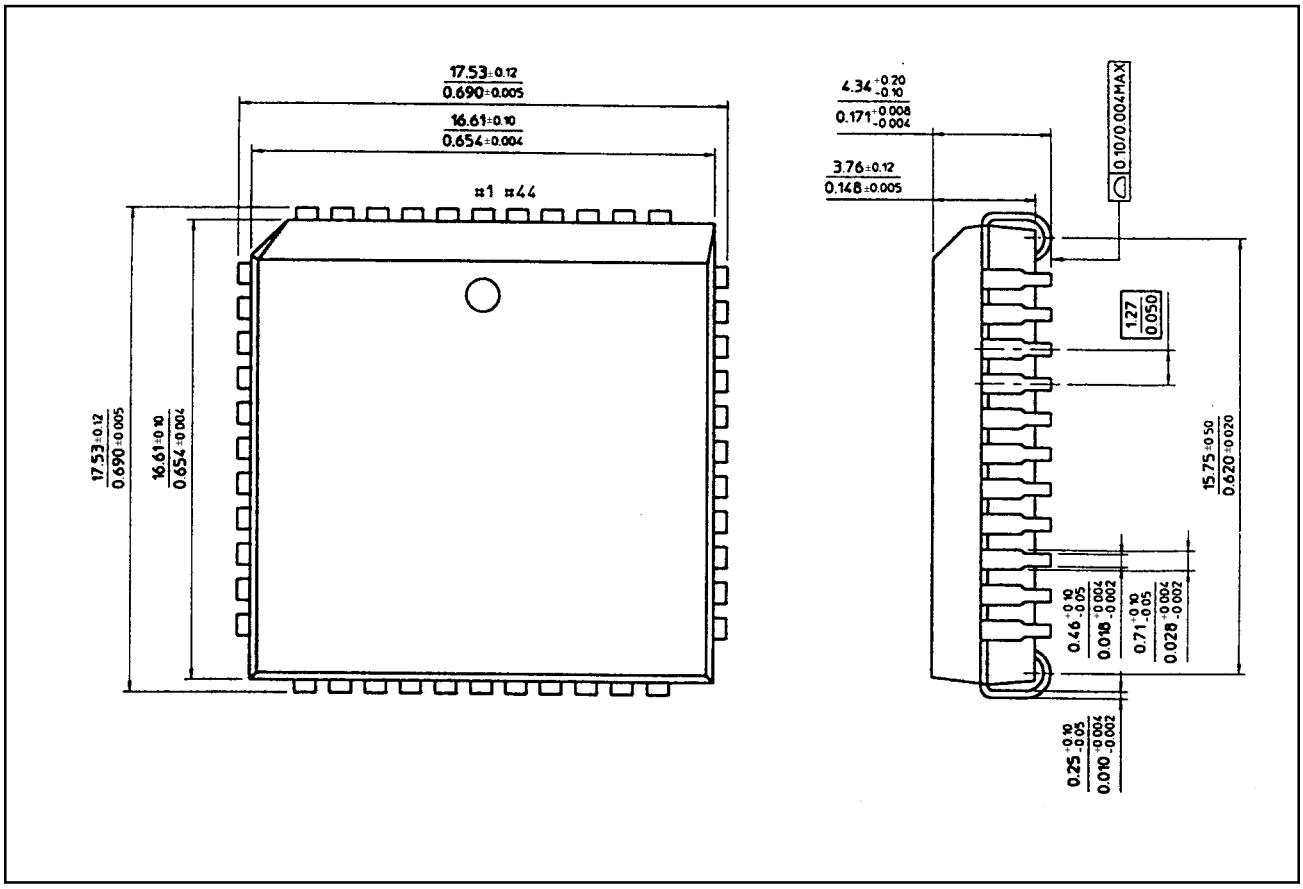


Figure-13. NW1501-XL 44-pin PLCC Package Diagram

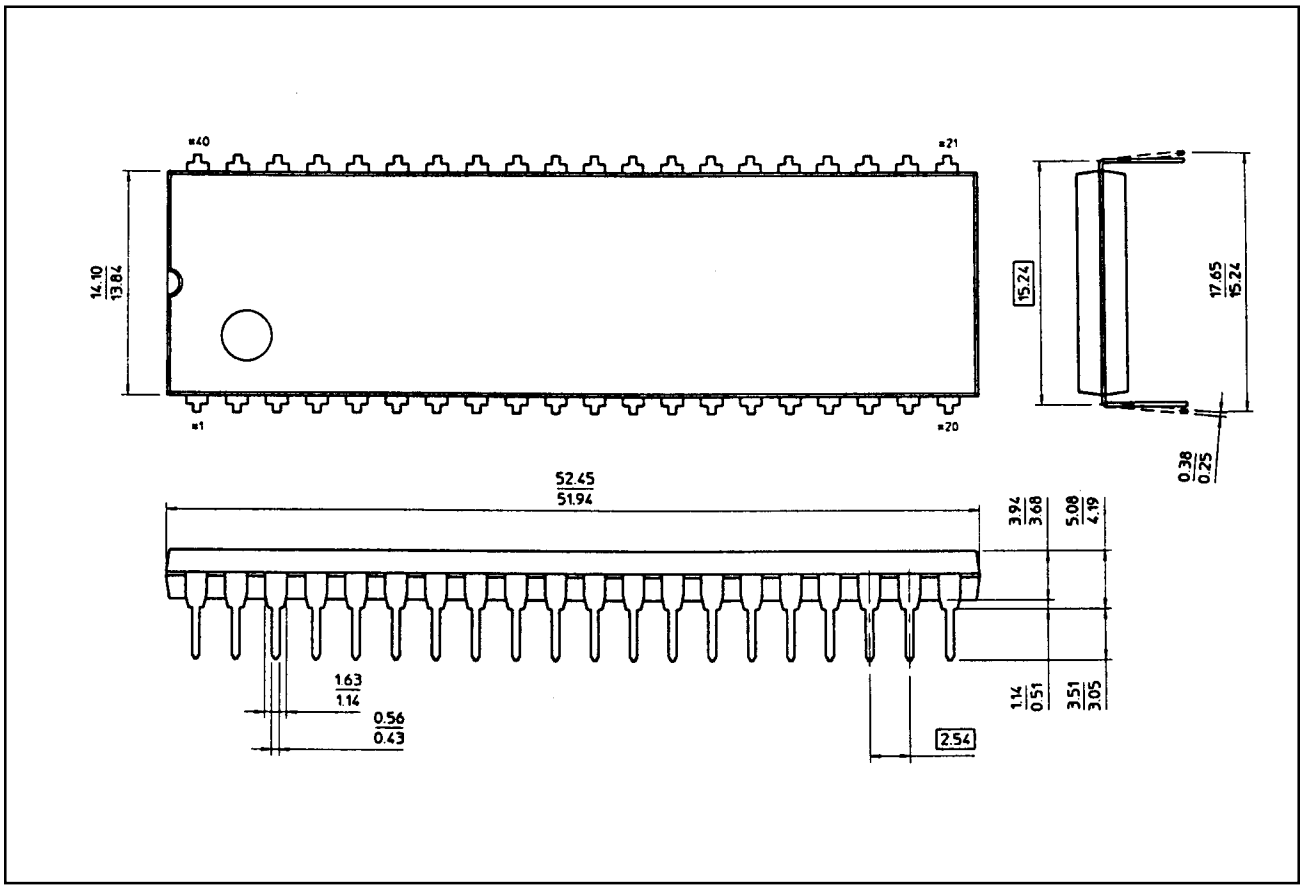


Figure-14. NW1501-XD 40-pin PDIP Package Diagram