NW1068
Programmable Octal PCM CODEC

Preliminary Data Sheet October, 2000 Ver 2.0

Features

- 8 channel CODEC with on-chip digital filters
- Software Selectable A/μ-law conversion
- Meets ITU-T G.711 - G.714 requirements
- Programmable digital filter adapting to system demands:
  - AC impedance matching
  - Echo cancellation
  - Frequency response correction
  - Gain Setting
- Support two programmable PCM buses
- Flexible PCM interface with up to 128 programmable time slots, data rate from 512 kbits/s to 8.192 Mbits/s
- Selectable MPI/GCI(IOM) interface
- Supports both Compressed and Linear data format
- Broadcast mode for coefficient setting
- 7 SLIC signaling pins (including 2 debounced pins) per channel
- Fast hardware ring trip mechanism
- Two programmable tone generators for test and DTMF
- Teletax signal generation (12 kHz or 16 kHz)
- Integrated programmable teletax signal and knotch filtering
- Programmable ring generator
- FSK generator
- Two programmable chopper clocks
- Master clock frequency selectable: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz
- Advanced test capabilities
  - 3 analog loop back tests
  - 5 digital loop back tests
  - Level metering function
- High analog driving capability (300 Ω)
- TTL and CMOS compatible digital I/O
- CODEC identification
- +5 V single power supply
- Low power consumption
- Operating temperature range: -40 °C to +85 °C
- Package available:
  NW1068-XQ 128 pin PQFP

Description

The NW1068 is a feature rich, single-chip, programmable 8 channel PCM CODEC with on-chip filters. Besides the μ-Law/A-Law companding analog-to-digital and digital-to-analog conversions based on ITU-T G.711 - G.714 specifications, NW1068 also provides 1 FSK generator, 2 programmable Tone generators (which can also generate ring signals), 1 programmable Teletax Signal generator together with 2 programmable chopper clocks for SLIC.

The digital filters in NW1068 provide the necessary transmit and receive filtering for voice telephone circuit to interface with time-division multiplexed systems. An integrated programmable DSP realizes AC Impedance Matching, Echo Cancellation, Frequency Response Correction and Gain Setting functions. The NW1068 supports 2 PCM buses with programmable sampling edge, which allows an extra delay of up to 7 clocks. Once the delay is determined, it is effective to all eight channels of NW1068. The device also provides 7 signaling pins to SLIC on per channel basis.

The NW1068 provides 2 programming interfaces: Microprocessor Interface (MPI) and General Communications Interface (GCI), which is also known as ISDN Oriented Module (IOM). For both MPI and GCI programming, the device supports both Compressed and Linear data format.

The device also offers strong test capability with several analog/digital loop-backs and level metering function. It brings convenience to system maintenance and diagnosis.

A unique feature of 'Hardware Ring Trip' is implemented in NW1068. When off-hook signal is detected, NW1068 can reverse an output pin to stop ringing immediately.

The NW1068 can be used in digital telecommunication applications such as Central Office Switch, PBX, DLC and Integrated Access Unit (IAD), i.e. VoIP and VoDSL.

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Block Diagram

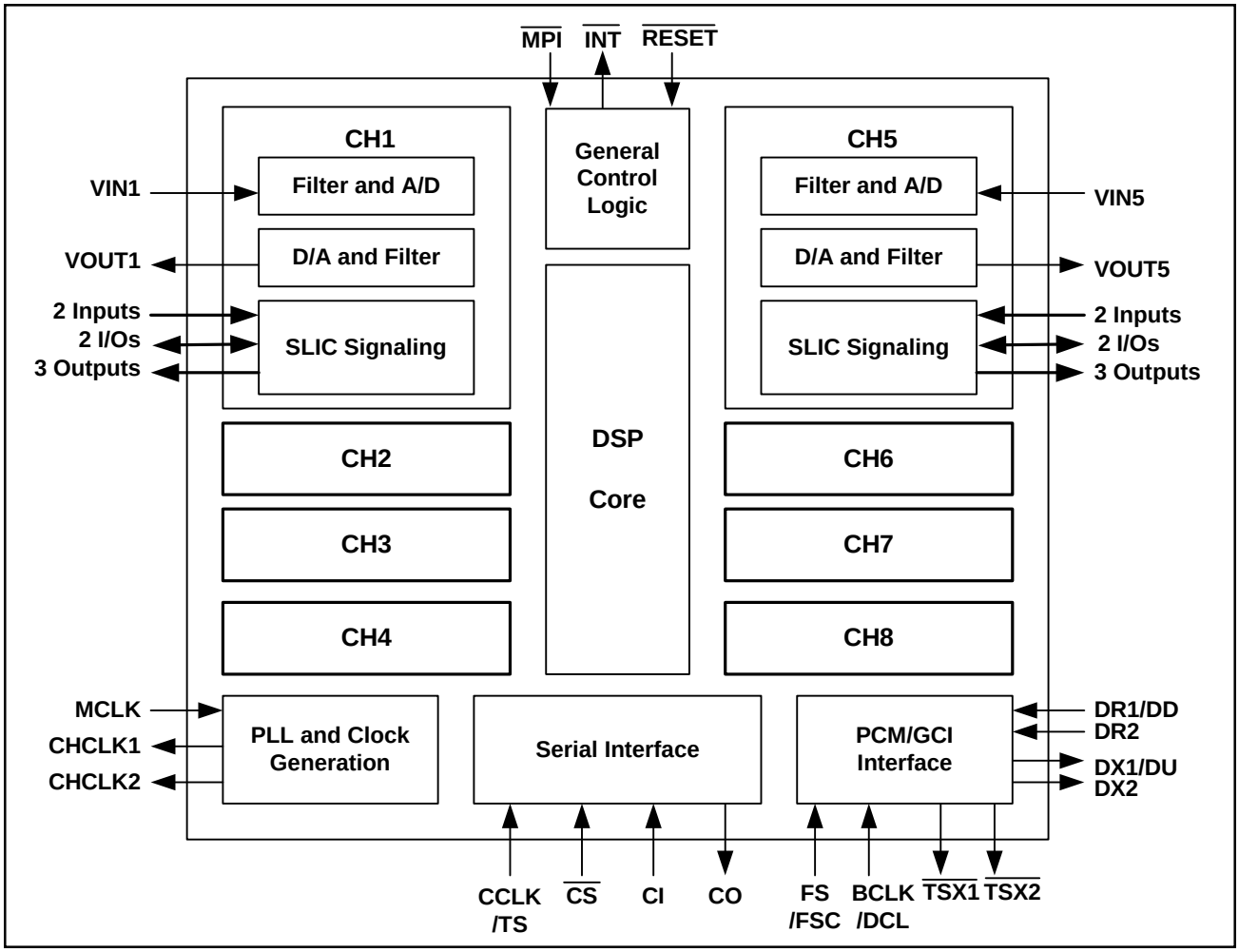


Figure-1. Block Diagram

Pin Connection

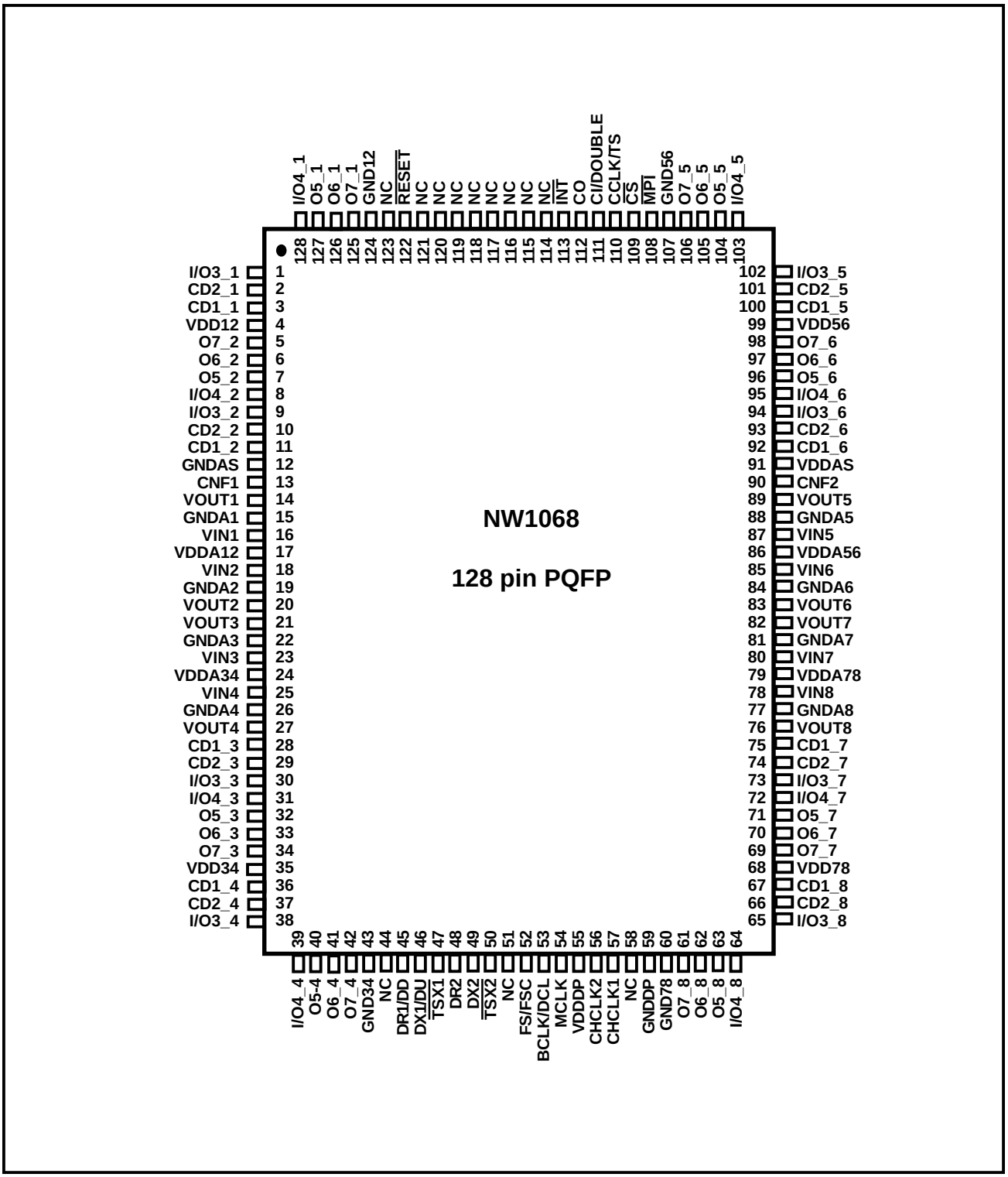


Figure-2. Pin Assignment

Pin Description

Name	Type	Pin Number	Description
GNDA1 GNDA2 GNDA3 GNDA4 GNDA5 GNDA6 GNDA7 GNDA8	-	15 19 22 26 88 84 81 77	**Analog Ground.** All ground pins should be connected together.
GNDAS	-	12	**Analog Ground For Bias.** All ground pins should be connected together.
GND12 GND34 GND56 GND78	-	124 43 107 60	**Digital Ground.** All ground pins should be connected together.
GNDDP	-	59	**Digital Ground For PLL.** All ground pins should be connected together.
VDDA12 VDDA34 VDDA56 VDDA78	-	17 24 86 79	**+5V Analog Power Supply.** These pins should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDAS	-	91	**+5V Analog Power Supply For Bias.** This pin should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDD12 VDD34 VDD56 VDD78	-	4 35 99 68	**+5V Digital Power Supply.** These pins should be connected to ground via a 0.1μF capacitor. All power supply pins should be connected together.
VDDDP	-	55	**+5V Digital Power Supply For PLL.** This pin should be connected to ground via a 0.1μF capacitance. All power supply pins should be connected together.
VIN1-8	I	16, 18, 23, 25 87, 85, 80, 78	**Analog Voice Inputs.** These pins should be connected with the SLIC via a capacitor (0.22 μF).
VOUT1-8	O	14, 20, 21, 27 89, 83, 82, 76	**Voice Frequency Receiver Outputs.** These pins can drive 300 Ω AC load. It allows the direct driving of transformer.
CD1_(1-8) CD2_(1-8)	I	3, 11, 28, 36 100, 92, 75 67 2, 10, 29, 37 101, 93, 74 66	**Debounced SLIC Signalling Inputs for Channel 1-8.**
I/O3_(1-8) I/O4_(1-8)	I/O	1, 9, 30, 38 102, 94, 73 65 128, 8, 31 39, 103, 95 72, 64	**SLIC Signalling I/Os for Channel 1-8.**
O5_(1-8) O6_(1-8) O7_(1-8)	O	127, 7, 32 40, 104, 96 71, 63 126, 6, 33 41, 105, 97 70, 62 125, 5, 34 42, 106, 98 69, 61	**SLIC Signalling Outputs for Channel 1-8.**

Name	Type	Pin Number	Description
DX1/DU	**O**	**46**	**Transmit PCM Data Output (For MPI)/GCI Data Upstream (For GCI).** In MPI mode, this pin remains high-impedance until a pulse appears on FS input. PCM data can output from DX1 or DX2 as selected by serial port. In GCI mode, GCI data is serially transmitted on this pin for all 8 channels of NW1068. Which part of the GCI data will be occupied is determined by CCLK/TS pin.
DX2	**O**	**49**	**Transmit PCM Data Output (For MPI).** This pin remains high-impedance until a pulse appears on FS input. PCM data can output from DX1 or DX2 as selected by serial port. This pin is not used in GCI mode.
DR1/DD	**I**	**45**	**Receive PCM Data Input (For MPI)/GCI Data Downstream (For GCI).** In MPI mode, PCM data is shifted into DR1 or DR2 following the BCLK. PCM data can input from DR1 and DR2 as selected by serial port. In GCI mode, GCI data is received serially on this pin for all 8 channels of NW1068. Which part of the GCI data will be transmitted is determined by CCLK/TS pin.
DR2	**I**	**48**	**Receive PCM Data Input (For MPI).** PCM data is shifted into DR1 or DR2 following the BCLK. PCM data can input from DR1 and DR2 as selected by serial port. This pin is not used in GCI mode
FS/FSC	**I**	**52**	**Frame Synchronisation (For MPI)/Frame Sync (For GCI).** In MPI mode, FS is an 8 kHz synchronisation clock that identifies the beginning of the PCM frame. In GCI mode, FSC is an 8 kHz signal that identifies the beginning of Timeslot 0 in the GCI frame.
BCLK/DCL	**I**	**53**	**Bit Clock (For MPI)/Data Clock (For GCI).** In MPI mode, this pin clocks out the PCM data on DX1 or DX2 pin. It may vary from 512kHz to 8.192 MHz, and is required to be synchronous with FS. In GCI mode, this pin is either 2.048 MHz or 4.096 MHz. The frequency is selected by CI/DOUBLE pin.
$\overline{\text{TSX1}}$ **$\overline{\text{TSX2}}$**	**O**	**47** **50**	**Time Slot Indicator Output (For MPI).** This pin pulses low during the receive time slot. A low on this pin indicates DX1/DX2 output. These two open-drain pins are not used in GCI mode.
$\overline{\text{CS}}$	**I**	**109**	**Chip Select.** In MPI mode, a low level on this pin enables the Serial Control Interface. In GCI mode, a low level on this pin configures a Compressed GCI operation; while a high level on this pin configures a Linear GCI operation.
CI/DOUBLE	**I**	**111**	**Serial Control Interface Data Input (For MPI)/Double DCL (For GCI).** In MPI mode, data input on this pin can control both CODEC and SLIC. In GCI mode, this pin is used to determine the frequency of DCL. When low, DCL will be 2.048 MHz; when high, DCL will be 4.096 MHz.
CO	**O**	**112**	**Serial Control Interface Data Tri-State Output (For MPI).** This pin is used to monitor SLIC working status. It is in high impedance state when $\overline{\text{CS}}$ is high. This pin is not used in GCI mode.
CCLK/TS	**I**	**110**	**Serial Control Interface Clock (For MPI)/Time Slot Select (For GCI).** In MPI mode, this is the clock for Serial Control Interface. It can be up to 8.192 MHz. In Compressed GCI mode, this pin indicates which half of 8 continuous GCI time slots is used. When this pin is low, time slots 0-3 are selected; when this pin is high, time slots 4-7 are selected. In Linear GCI mode, this pin indicates which half of 8 continuous GCI time slots is used for voice signal. When this pin is low, time slots 0-3 are used as Monitor channel and C/I octet, time slots 4-7 are used for linear voice; when this pin is high, time slots 4-7 are used for linear voice, time slots 0-3 are used as Monitor channel and C/I octet.
$\overline{\text{MPI}}$	**I**	**108**	**MPI/GCI Select.** This pin is used to determine which operation mode the NW1068 works in. When this pin is low, MPI/PCM mode is selected; When this pin is high, GCI mode is selected.

Pin Description (continued)

Name	Type	Pin Number	Description
$\overline{\text{RESET}}$	I	122	**Reset Input.** Forces the device to default mode. Active low.
$\overline{\text{INT}}$	O	113	**Interrupt Output Pin.** Active low interrupt signal for ch1-ch8, open-drain. It reflects the changes on SLIC pins.
MCLK	I	54	**Master Clock.** Master clock provides the clock for DSP. It can be 1.536 MHz, 1.544 MHz, 2.048 MHz, 4.096 MHz, or 8.192 MHz.
CHCLK1	O	57	**Chopper Clock Output.** Provides a programmable (2 -28 ms) output signal synchronous to MCLK.
CHCLK2	O	56	**Chopper Clock Output.** Provides a programmable 256 kHz, or 512 kHz or 16.384 MHz output signal synchronous to MCLK.
CNF1 CNF2	-	13 90	**Capacitor Noise Filter.**
NC	-	44 58 114 115 116 117 118 119 120 121 123	**No Connection.**

General Description of Programming

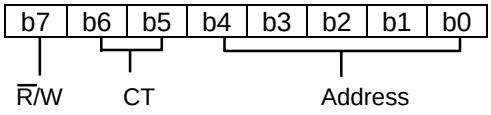
MPI and GCI Control Mode

NW1068 can be controlled in two modes: MPI mode and GCI mode. Which mode will be effective is determined by the state of $\overline{MPI}$ pin and $\overline{CS}$ pin (see Page-14 MPI and GCI Operation Selection) .

Programming Command

In both MPI mode and GCI mode, the programming is realized by writing command to Registers or RAM in the chip. In MPI mode, command is written to the chip through CI pin, whereas in GCI mode, command is written to the chip through DR1/DD pin.

For both MPI mode and GCI mode, the format of command is as the following:



$\overline{R}$/W: Read/Write Command bit.

b7 = 0: Read Command
b7 = 1: Write Command

CT: Command Type

b6 b5 = 00: LC - Local Command
b6 b5 = 01: GC - Global Command
b6 b5 = 10: NOT ALLOWED
b6 b5 = 11: RC - RAM Command

Address: Specify which register or which block of RAM will be read or write.

For both Local Command and Global Command, b[4:0] are used to address the Local Registers or Global Registers.

For RAM Command, b4 is used to distinguish the Coe-RAM and the FSK RAM:
b4 = 0: The RAM Command is for Coe-RAM
b4 = 1: The RAM Command is for FSK-RAM

When the RAM Command is for Coe-RAM, b[3:0] are used to address the blocks in the Coe-RAM.

When the RAM Command is for FSK-RAM, b3 is always '0' and b[2:0] are used to address the blocks in the FSK-RAM.

Command Type

There are 3 types of Command in NW1068 distinguished by different combination of b6b5.

Local Command is used to configure each channel, and Global Command is used to configure all 8 channels. When using Local Command, Global Command 7 (Channel Enable Command) must be used first to specify which channel will be configured by the followed Local Command. If Global Command 7 enabled more than one channel, then all of the enabled channels will be configured by the followed Local Command at one time.

RAM Command is used to Read/Write RAM. When a RC is executed, a RAM block which consists of 8 words (14 or 16 bits/word) will be accessed .

Register and RAM

NW1068 provides 2 different groups of registers and 2 different groups of RAM, they are:

- 12 Local Registers per channel (Totally 96 Registers)
- 26 Global Registers
- 40 * 14 bits Coe-RAM per channel (Devided into 5 blocks)
- 32 * 16 bits FSK-RAM (Devided into 4 blocks)

Local Command is used to Read/Write Local Registers, Global Command is used to Read/Write Global Registers and RAM Command is used to Read/Write either Coe-RAM or FSK-RAM.

Addressing of Register and RAM

- Addressing of Local Register

In MPI mode, when addressing Local Registers, Global Command 7 (Channel Enable) must be used first to specify the channel(s), then the address (b[4:0]) in the followed Local Command indicates which one of the 12 Local Registers for that channel(s) will be addressed.

In GCI mode, the position (Time Slot) of Local Command and b4 in Program Start Byte (see Page-10) would indicate which channel to be addressed.

The b[3:0] of a Local Command address the 12 Local Registers for each channel.

NW1068 provides a Consecutive Adjacent Addressing for Read/Write Local Registers. If the address of the one Local Register is specified in a Local Command, the next (Address Countdown) 1 to 4 adjacent registers will be Read/Write automatically. If the address of the register specified by the Local Command is end with '11' (b1b0='11'), 4 adjacent registers will be Read/Write by this Command. If b1b0 ='10', then 3 adjacent registers will be Read/Write. If b1b0 = '01', then only 2 adjacent registers will be Read/Write. If b1b0 = '00', then only this specified register will be Read/Write. The details of the Consecutive Adjacent Addressing is shown as below:

Address Specified by Local Command	In/Out Data	Registers being R/W
b4 b3 b2 b1 b0		
X X X 1 1	Byte 1	X X X 11
(b1b0 = 11, 4 bytes **DATA**)	Byte 2	X X X 10
	Byte 3	X X X 01
	Byte 4	X X X 00
X X X 1 0	Byte 1	X X X 10
(b1b0 = 10, 3 bytes **DATA**)	Byte 2	X X X 01
	Byte 3	X X X 00
X X X 0 1	Byte 1	X X X 01
(b1b0 = 01, 2 bytes **DATA**)	Byte 2	X X X 00
X X X 0 0	Byte 1	X X X 00
(b1b0 = 00, 1 byte **DATA**)		

In MPI mode, when $\overline{CS}$ becomes low, NW1068 treats the first byte on CI pin as command, and the rest byte(s) as data. To write another command, the $\overline{CS}$ must change from low to high to finish the previous command and then change from high to low to indicate the start of the next command. When a Read/Write is completed, $\overline{CS}$ must be pulled to high in 8-bit time.

In MPI mode, the procedure of Consecutive Adjacent Addressing can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ change from low to high, the operation of the current Register and the next adjacent registers will be aborted. But for previous operation, the results are still effective.

IN GCI mode, the Consecutive Adjacent Addressing can not be stopped once a command is initiated. For write command, the number of bytes following the command must be the same as the number of registers being written.

- Addressing of Global Register

The address of the 26 Global Registers is from:

00000 - 11000 (25 adjacent Global Registers) and
11100 (the 26th. Global Register)

The address of the 26th. Global Register is 11100, because the address of Global Registers from 11001 to 11011 are reserved.

For the adjacent 25 Global Registers, NW1068 also provides a Consecutive Adjacent Addressing for Read/Write, which is exactly the same as the Local Registers. In MPI mode, the procedure of Consecutive Adjacent Addressing also can be stopped by $\overline{CS}$ signal at any time as it does for Local Registers. In GCI mode, the situation is also the same as in Local Registers. But for the 26th Global Register (address is 11100), once a Read/Write procedure is completed, $\overline{CS}$ must be pulled high.

- Addressing of Coe-RAM

The Coe-RAM (Coefficient RAM) is consisted of 5 blocks for per channel and totally 40 words. Each block contains 8 words. The 5 blocks are:
- IMF RAM (Word0 - Word7), for Impedance Matching Filter coefficient;
- ECF RAM (Word8 - Word15), for Echo Cancellation Filter coefficent;
- GIS RAM (Word16 - Word23), for Gain for Impedance Scaling;
- FRX RAM (Word24 - Word30) and GTX RAM (Word31), for Frequency Response Correction in Transmit Path coefficient and Gain in Transmit Path;
- FRR RAM (Word32 - Word 38) and GRX RAM (Word39), for Frequency Response Correction in Receive Path coefficient and Gain in Receive Path.
See APPENDIX II: Coe-RAM Mapping.

Each word in Coe-RAM is 14 bit wide. To write a Coe-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill one word with MSB first**,** but the last two bits (LSB) will be neglected. When being read, each Coe-RAM word will output 16 bits with MSB first, but the last two bits are meaningless.

In MPI mode, when addressing Coe-RAM, Global Command 7 (Channel Enable) must be used first to specify the channel(s), then the Address (b[4:0]) in the followed RAM Command indicates which block in the Coe-RAM for that channel(s) will be addressed. In GCI mode, the position (Time Slot) of RAM Command and b4 in Program Start byte would indicate the channel to be addressed.

Only b[3:0] of a Coe-RAM Command can be used to address the 5 blocks in Coe-RAM, as b4 is used to distinguish the Coe-RAM and FSK-RAM:

B4 = 0: b[3:0] is used to address Coe-RAM
B4 = 1: b[3:0] is used to address FSK-RAM

When the address of a Coe-RAM block is specified in a RAM Command, the all 8 words in this block will be Read/ Write automatically, with the highest order word first.

In MPI mode, when read/write a Coe-RAM block, the procedure of addressing words can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ change from low to high, the operation of the current word and the next adjacent words will be aborted. But for previous operation, the results are still effective.

- Addressing of FSK-RAM

The FSK-RAM is consisted of 4 blocks, each block has eight 16-bit words.

To write a FSK-RAM word, 16 bits (or, two 8-bit bytes) are needed to fulfill one word with MSB first**.** When being read, each FSK-RAM word in FSK-RAM will output 16 bits with MSB first.

Only b[2:0] of a FSK-RAM Command are needed to address the 4 blocks in FSK-RAM, b3 should be always '0', and b4 is always '1' to indicate the address is for FSK-RAM.

When the address of a FSK-RAM block is specified in a RAM Command, the all 8 words in this block will be Read/ Write automatically, with the highest order word first.

In MPI mode, when read/write a FSK-RAM block, the procedure of addressing words can be stopped by $\overline{CS}$ signal at any time. When $\overline{CS}$ change from low to high, the operation of the current word and the next adjacent words will be aborted. But for previous operation, the results are still effective.

Commands In GCI Operation

I. General Description

In GCI operation, the NW1068 uses the monitor channel for the exchange of status or mode information with high level processors. The messages transmitted in the monitor channel have different data structures. For a complete command operation, the first byte of monitor channel data indicates the address of the device either sending or receiving the data. All monitor channel messages to/from NW1068 begin with the following Program Start (PS) byte:

b7	b6	b5	b4	b3	b2	b1	b0
1	0	0	$\overline{A}$/B	0	0	0	1

Where, $\overline{A}$/B identifies Channel A or Channel B:
$\overline{A}$/B = 0: Channel A is the source (upstream) or destination (downstream) -81H;
$\overline{A}$/B = 1: Channel B is the source (upstream) or destination (downstream) -91H.

The Program Start byte is followed by a command byte. For global command, the $\overline{A}$/B bit in the PS byte can be ignored. If the command byte specifies a write, then from 1 to 16 additional data bytes may follow (1-4 for registers, 1-16 for RAM). If the command byte specifies a read, additional data bytes may follow. NW1068 responds to the read command by sending up to 16 data bytes upstream containing the information requested by the upstream controller. Each byte on monitor channel must be transferred at least twice and in two consecutive frames.

II. Identification Command

In order to distinguish different devices by software, a two byte identification command (8000H) is defined for NW1068:

1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NW1068 will reply with identification code 8082H:

1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0

III. LC/GC Read or Write Commands
An example of Local Command write one byte (Local Register 00H) and read back:

DD	b7	b6	b5	b4	b3	b2	b1	b0	DU	b7	b6	b5	b4	b3	b2	b1	b0
PS	1	0	0	0	0	0	0	1	IDLE	1	1	1	1	1	1	1	1
Write 1 byte	1	0	0	0	0	0	0	0	IDLE	1	1	1	1	1	1	1	1
Byte 1	DATA								IDLE	1	1	1	1	1	1	1	1
PS	1	0	0	0	0	0	0	1	IDLE	1	1	1	1	1	1	1	1
Read 1 byte	0	0	0	0	0	0	0	0	IDLE	1	1	1	1	1	1	1	1
IDLE	1	1	1	1	1	1	1	1	PS	1	0	0	0	0	0	0	1
IDLE	1	1	1	1	1	1	1	1	Byte 1	DATA							

IV. RC (Coe-RAM) Read/Write Commands
An example of RC write one word (Coe-RAM 00H) and read back

DD	b7	b6	b5	b4	b3	b2	b1	b0	DU	b7	b6	b5	b4	b3	b2	b1	b0
PS	1	0	0	0	0	0	0	1	IDLE	1	1	1	1	1	1	1	1
Write 1 word	1	1	1	0	0	0	0	0	IDLE	1	1	1	1	1	1	1	1
Byte 1	DATA_H								IDLE	1	1	1	1	1	1	1	1
Byte 2	DATA_L						X	X	IDLE	1	1	1	1	1	1	1	1
PS	1	0	0	0	0	0	0	1	IDLE	1	1	1	1	1	1	1	1
Read 1 word	0	1	1	0	0	0	0	0	IDLE	1	1	1	1	1	1	1	1
IDLE	1	1	1	1	1	1	1	1	PS	1	0	0	0	0	0	0	1
IDLE	1	1	1	1	1	1	1	1	Byte 1	DATA_H							
IDLE	1	1	1	1	1	1	1	1	Byte 2	DATA_L						X	X

Note: In Coe-RAM, the data word is 14 bit wide. The lowest 2 bits in the DATA_L are don't_care.

V. RC (FSK-RAM) Read/Write Commands
An example of RC write one word (FSK-RAM 00H) and read back:

DD	b7	b6	b5	b4	b3	b2	b1	b0	DU	b7	b6	b5	b4	b3	b2	b1	b0
PS	1	0	0	0	0	0	0	1	IDLE	1	1	1	1	1	1	1	1
Write 1 word	1	1	1	1	0	0	0	0	IDLE	1	1	1	1	1	1	1	1
Byte 1	DATA_H								IDLE	1	1	1	1	1	1	1	1
Byte 2	DATA_L								IDLE	1	1	1	1	1	1	1	1
PS	1	0	0	0	0	0	0	1	IDLE	1	1	1	1	1	1	1	1
Read 1 word	0	1	1	1	0	0	0	0	IDLE	1	1	1	1	1	1	1	1
IDLE	1	1	1	1	1	1	1	1	PS	1	0	0	0	0	0	0	1
IDLE	1	1	1	1	1	1	1	1	Byte 1	DATA_H							
IDLE	1	1	1	1	1	1	1	1	Byte 2	DATA_L							

Commands In MPI Operation

I. General Description

In MPI operation, the NW1068 is programmed by microprocessor via a serial interface which consists of 4 pins: $\overline{CS}$, CCLK, CI and CO. All the commands and data transmitted or received serially are aligned with byte (8 bits). The data transfer is synchronized by the CCLK input. The contents of CI is latched at the rising edges of CCLK, while CO changes with the falling edges of CCLK. During the implementation of commands which followed by output data (read commands), the device will not accept any new command from CI. The data transfer sequence can be interrupted by setting $\overline{CS}$ high. A broadcast mode is provided in MPI write operation by enabling all 8 channels using Global Command 7. In this mode, data can be written to all 8 channels by one command.

When read, NW1068 outputs an Idendification Code of 81H before data bytes. The Identification Code are used to indicate the following data is from NW1068

CCLK is the only reference of CI and CO pins. Its duty and frequency may not necessarily be standard.

II. LC/GC Read or Write Commands

An example of LC write one byte (Local Register 00H) and read back:

CI	b7	b6	b5	b4	b3	b2	b1	b0	CO	b7	b6	b5	b4	b3	b2	b1	b0
Write 1 byte	1	0	0	0	0	0	0	0	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Byte 1	DATA								IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Read 1 byte	0	0	0	0	0	0	0	0	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	ID	1	0	0	0	0	0	0	1
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	Byte 1	DATA							

Note: 'Z' means High Impedance. In this case, CI and CO can be connected together.
When CI and CO are not connected, the input from CI will be neglected.

III. RC (Coe-RAM) Read/Write Commands

An example of RC write one word (Coe-RAM 00H) and read back:

CI	b7	b6	b5	b4	b3	b2	b1	b0	CO	b7	b6	b5	b4	b3	b2	b1	b0
Write 1 word	1	1	1	0	0	0	0	0	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Byte 1	DATA_H								IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Byte 2	DATA_L						X	X	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Read 1 word	0	1	1	0	0	0	0	0	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	ID	1	0	0	0	0	0	0	1
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	Byte 1	DATA_H							
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	Byte 2	DATA_L						X	X

Note: In Coe-RAM, the data word is 14 bit wide. The lowest 2 bits in the DATA_L are don't_care.

IV. RC (FSK-RAM) Read/Write Commands

An example of RC write one word (FSK-RAM 00H) and read back:

CI	b7	b6	b5	b4	b3	b2	b1	b0	CO	b7	b6	b5	b4	b3	b2	b1	b0
Write 1 word	1	1	1	1	0	0	0	0	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Byte 1	DATA_H								IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Byte 2	DATA_L								IDLE	Z	Z	Z	Z	Z	Z	Z	Z
Read 1 word	0	1	1	1	0	0	0	0	IDLE	Z	Z	Z	Z	Z	Z	Z	Z
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	ID	1	0	0	0	0	0	0	1
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	Byte 1	DATA_H							
IDLE	Z	Z	Z	Z	Z	Z	Z	Z	Byte 2	DATA_L							

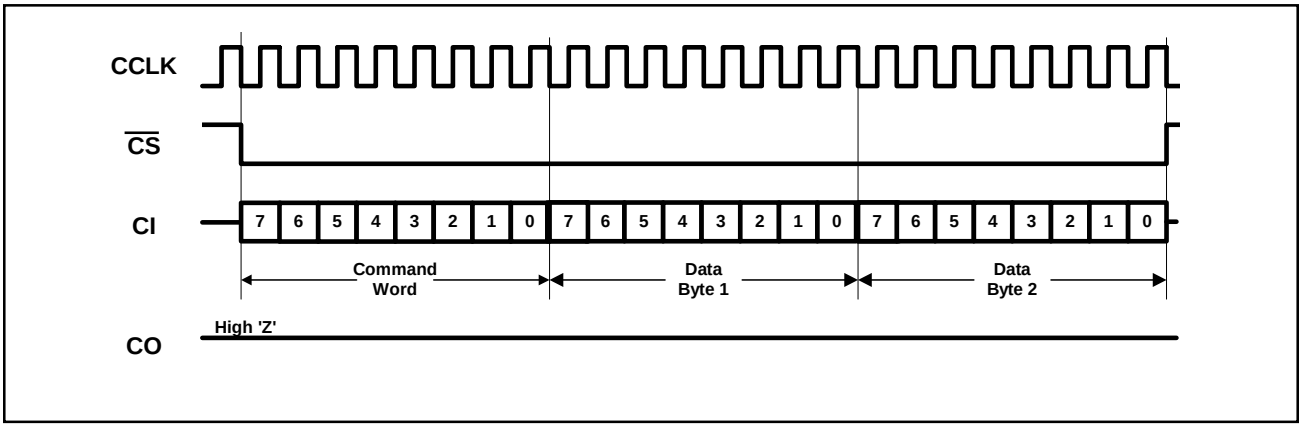


Figure 3. An Example of Serial Interface Write Mode

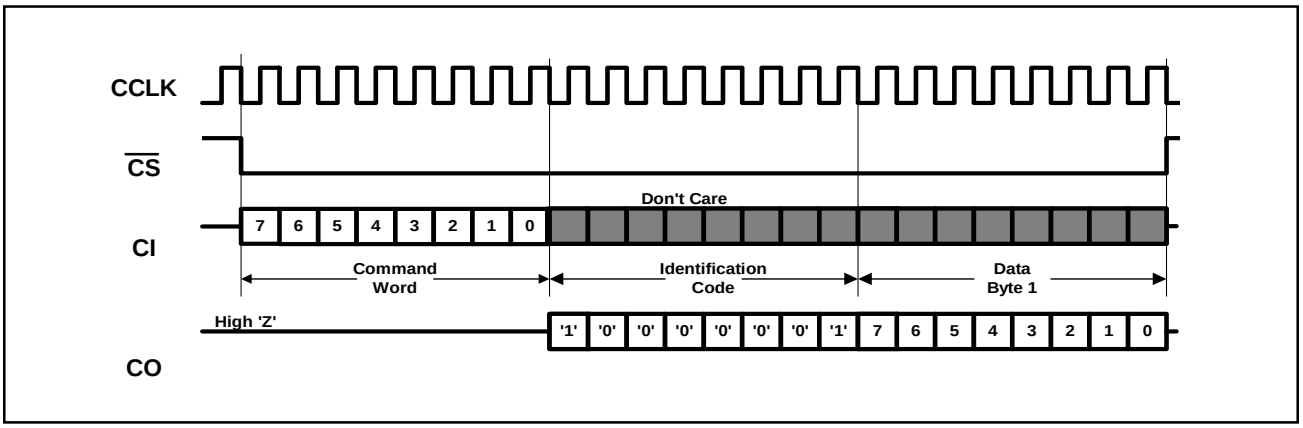


Figure 4. An Example of Serial Interface Read Mode (ID = 81h)

Functional Description

Power-on Sequence and Master Clock Configuration

To power on NW1068, users should follow this sequence:
1. Apply ground first;
2. Apply VCC, finish signal connections and set $\overline{\text{RESET}}$ low, thus the device goes into default state;
3. Set $\overline{\text{RESET}}$ high;
4. Select master clock frequency;
5. Program filter coefficients and other parameters as required;

The master clock frequency of NW1068 can be configured as 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz by setting MCLK Select Register (Global Command 6).

In MPI operation, the master clock is derived from MCLK pin. The master clock is used by DSP core. The source for the master clock can be asynchronous to BCLK.

In GCI operation, the master clock is obtained from MCLK pin. It is recommended to connect MCLK and DCL pins together. DCL can be only 2.048 MHz or 4.096 MHz.

Default State After Reset

When the NW1068 is powered on, or reset either by $\overline{\text{RESET}}$ pin or GCI/MPI Command, the device defaults to the following operation:
1. All eight channels are powered down and in standby mode;
2. All loop-backs and cut-off are disabled;
3. DX1/DU pin is selected for all channels for transmission, DR1/DD pin is selected for all channels to receive data;
4. The master clock frequency is 2.048 MHz;
5. For MPI operation, transmit and receive time slots are set to 0-7 respectively for channel 1-8. The PCM data rate is the same as clock frequency. Data is transmitted on rising edges while is received on falling edges;
   For GCI operation, time slots to be used is determined by TS pin, and data rate is determined by DOUBLE pin. DD, DU clocks data on rising edges of DCL;
6. A-Law is selected;
7. Default values for FRX, FRR, GTX and GTR are selected. The analog gains are set to 0 dB. IMF, GIS and ECF are disabled, while HPF is enabled (See Figure 8: Signal Flow of Each Channel);
8. I/O3 and I/O4 are configured as input;
9. CD1 and CD2 are configured with no debounce;
10. All interrupts are disabled, and all pending interrupts are cleared;
11. All feature function blocks including FSK, Dual Tone, Teletax, Ring Trip and Level Metering are turned off;
12. CHCLK1 and CHCLK2 are set to high.

The data stored in RAM will not be changed by any kind of reset. In this way, the RAM data programmed before reset will not be lost until the device powered down physically.

MPI and GCI Operation Selection

The NW1068 allows both MPI and GCI programming interfaces, it supports three operations: MPI, Compressed GCI and Linear GCI. The operation selection is executed by $\overline{\text{MPI}}$ and $\overline{\text{CS}}$ pins.

$\overline{\text{MPI}}$	$\overline{\text{CS}}$	Chip Mode
0	1/0	MPI
1	0	Compressed GCI
1	1	Linear GCI

In MPI operation, each channel of NW1068 can be assigned to any time slot of the PCM highway.

In GCI operation, the data clock frequency can be selected as 2.048 MHz or 4.096 MHz by DOUBLE pin. The data rate will remain 2.048 Mbit/s in both clock frequencies. In Compressed GCI operation, the 8 channels of NW1068 can be assigned to one of the 2 groups of time slots by setting TS pin. In Linear GCI operation, the linear voice signal of the eight channels occupies 4 GCI time slots, and the rest 4 GCI time slots are used for Monitor and C/I octet. Which half of the 8 GCI time slots are used for linear voice is determined by TS pin.

Operation mode can be changed in working states by setting $\overline{\text{MPI}}$ and $\overline{\text{CS}}$ pins accordingly. After the change, a hardware reset will be required to set the chip into default state. Or, users can reprogram the device by commands and accessing RAMs.

Channel Program Enable

In MPI operation, NW1068 offers a Channel Program Enable command (Global Command 7) to facilitate the addressing of individual or multiple channels. Each bit of this command is assigned to one specific channel. The channel or channels are enabled when their corresponding bits are set high. In this way, multiple channel addressing is accomplished without increasing the number of I/O pins on the device. When all channels are enabled by setting all channel enable bits high, the NW1068 enters a broadcast state simply and efficiently. In read operation, multiple channel addressing is not allowed.

In GCI operation, the individual channels are controlled by their respective Monitor and C/I channels embedded in the GCI time slots selected by TS pin.

A-Law/μ-Law Select

The NW1068 supports both A-Law and μ-Law companding A/D and D/A conversions. The law selection is done by the LS bit in Global Command 8.

Gain Adjustment

The analog gain and digital gain of each channel can be adjusted separately in NW1068.

For each individual channel, in transmit path, analog gain can be selected as 0 dB or 6 dB. The selection is done by A/D Gain (GAD) bit in Local Command 10. The default analog gain for both transmit path and receive path is 0 dB.

Digital gain of transmit path can be programmed from 0 to 12 dB with minimum 0.1 dB step. If CS[5] is '0' in Local Command 1, the Digital Transmit Gain will be set to the default value, which is 0 dB. If CS[5] bit is '1' in Local Command 1, the Digital Transmit Gain will be decided by the coefficient in Coe-RAM.

For each individual channel, in receive path, analog gain can be selected as 0 dB or -6 dB. The selection is done by D/A Gain (DAG) bit in Local Command 10. The default analog gain for receive path is 0 dB.

Digital gain of receive path can be programmed from 0 to -12 dB with minimum 0.1 dB step. If CS[7] bit is '0' in Local Command 1, the digital gain in receive path is set to be the default value, which is 0 dB. If CS[7] bit is '1' in Local Command 1, the digital gain in receive path will be decided by the coefficient in Coe-RAM.

Gain coefficient are GTX (for transmit) and GRX (for receive). GTX and GRX can be calculated automatically by software (Newave provide) according to the specified dB figure. The address of GTX/GRX in Coe-RAM is shown APPENDIX II <<Coefficient Memory Address Mapping>>.

Impedance Matching

There is a programmable feedback path on each channel from VIN to VOUT in the NW1068. It synthesizes the two-wire impedance of the SLIC. The coefficients for Impedance Matching are GIS and IMF, the address of GIS and IMF is shown in APPENDIX II.

Echo Cancellation

Transhybrid balancing filter is used to adjust transhybrid balance to ensure the echo cancellation meets the ITU-T specifications. The coefficient for Echo Cancellation is ECF, the address of ECF is shown in APPENDIX II.

Frequency Response Correction

The FRX filter in the transmit path and the FRR filter in the receive path can be programmed to correct any frequency distortion caused by the impedance matching filters. The coefficients of Frequency Response Correction are FRX for transmit path and FRR for receive path. The address of FRX/FRR is listed in APPENDIX II.

Coefficient Calculation

All the coefficients, including IMF, ECF, GIS, FRX, FRR, GTX, GRX can be calculated automatically by a software provided by Newave. The user just input the SLIC model and the desired gain (dB), the software will automatically calculate all the above coefficients. When these coefficients are written to the Coe-RAM, the final AC characters of the line card (consists of SLIC and CODEC) will meet the ITU-T specifications.

PCM Interface, Highway Selection and Dynamic Time-slot Assignment (For MPI Operation)

In MPI operation, NW1068 provides a flexible PCM interface for all 8 channels with programmable data rate, sampling edge, data format selection and up to 7 clocks data delay. All the controls are implemented by Global Command 8. Once the PCM interface is configured by Global Command 8, it's effective for all 8 channels.

The PCM data rate can be configured as the same as BCLK or half of it. NW1068 can transmit or receive data either on BCLK rising edges or falling edges. See Figure 5. The PCM data transmit and receive timeslot can be offset from FS for 0 BCLK period to 7 BCLK periods. The PCM interface of NW1068 also allows both Compressed voice data format and Linear voice data format. The Compressed voice data is 8 bit wide, and the Linear voice data is 16 bit wide with 2's complement.

Each channel of NW1068 can be assigned to any time-slot of the PCM highway. The number of available time-slots is determined by BCLK frequency. When BCLK is 512 kHz, time-slot 0-7 are available; when BCLK is 1.024 MHz, time slot 0-15 are available; when BCLK is 8.192 MHz, time-slot 0-127 are selectable.

When Compressed format is selected, the voice data of one channel occupies one time-slot. Local Command 7 selects the transmit time-slot for each channel, while Local Command 8 selects the receive time-slot for each channel.

When Linear format is selected, the voice data of one channel occupies a time-slot group, which is consisted of 2 adjacent time-slots. The TT[6:1] bits in Local Command 7 select the transmit time-slot group for each channel, and the TT0 bit is ignored. The RT[6:1] bits in Local Command 8 select the receive time-slot group for each channel, and the TR0 bit is ignored.

PCM data for each individual channel can be clocked out of DX1 or DX2 pin on the programmed edges of BCLK according to time slot assignment. The transmit highway (DX1/2) is selected by Local Command 7. The frame sync (FS) pulse identifies the beginning of a transmit frame, or time-slot0.The PCM data is transmitted serially on DX1 or DX2 with MSB (Bit1) first.

PCM data for each channel can be clocked into DR1 or DR2 pin on the programmed edges of BCLK according to time slot assignment. The receive highway (DR1/2) is selected by Local Command 8. The frame sync (FS) pulse identifies the beginning of a receive frame, or time-slot0. The PCM data is transmitted serially on DX1 or DX2 with MSB (Bit1) first.

The NW1068 allows any BCLK frequency between 512 kHz and 8.192 MHz at increment of 64 kHz in a system.

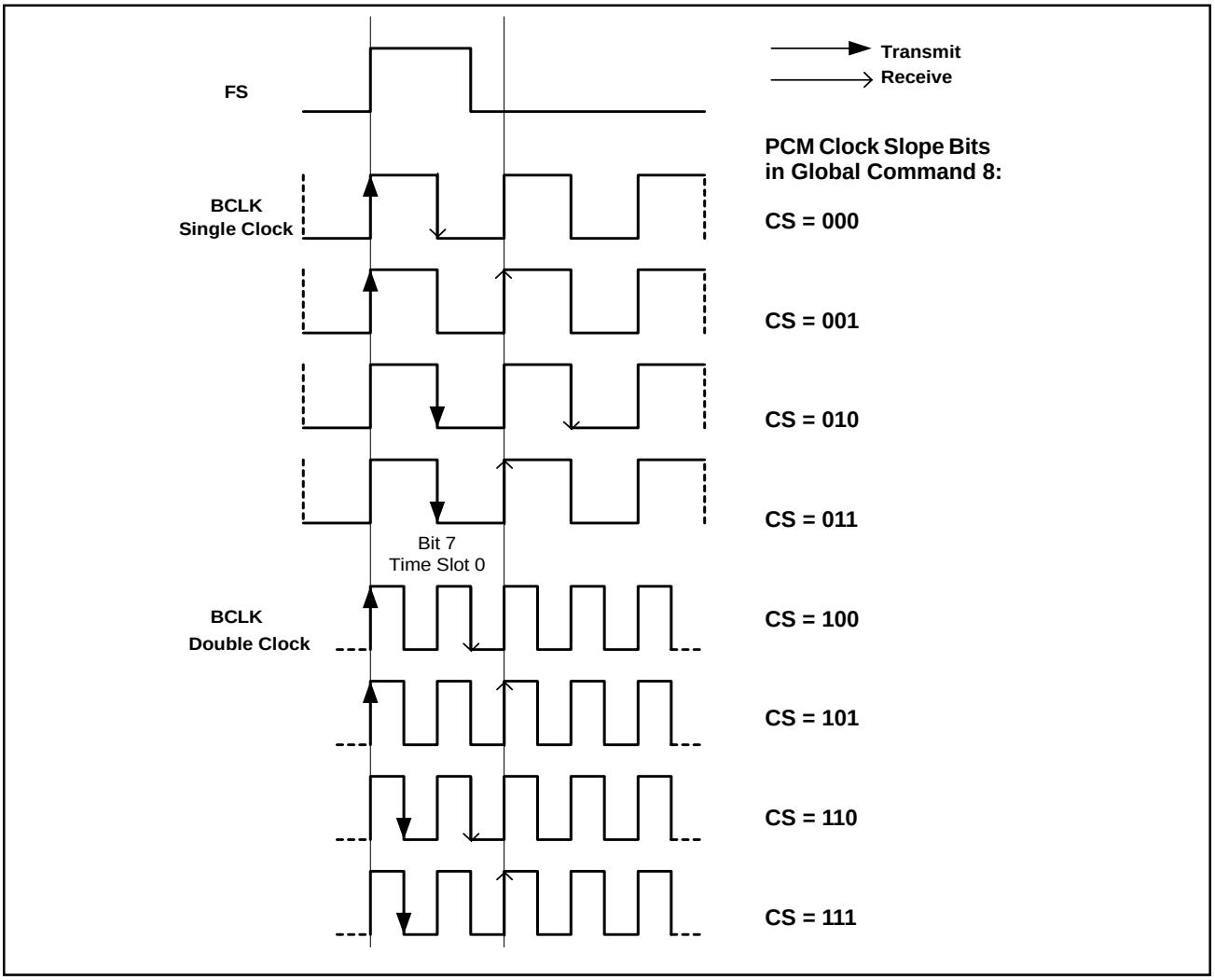


Figure 5. Sampling Edge Select Waveform

SLIC Control

The SLIC interface of NW1068 for each channel consists of 7 pins: inputs CD1 and CD2, 2 I/O pins I/O3 and I/O4, together with 3 outputs O5, O6 and O7.

1. CD1 and CD2

SLIC inputs CD1 and CD2 can be read in 2 ways - globally for all 8 channels, or locally for each individual channel.

For global read, NW1068 provides 2 registers for CD1 and CD2 data of all eight channels. They can be accessed by Global Command 10 and 11 at any time regardless of the channel program enable state. In this way, informations on CD1 or CD2 for eight channels can be derived from NW1068 with single read operation. The 2 data registers allow the microprocessor a more efficient way of obtaining time-critical data such as on/off-hook and ring trip information. They are available in both MPI and GCI operations.

The eight CDA bits of Global Command 10 represents the debounced CD1 signal on corresponding channels, while the eight CDB bits of Global Command 11 represents the debounced CD2 signal on corresponding channels. Both CD1 and CD2 can be assigned to off-hook, ring trip, ground key signals or other signals.

In MPI operation, CD1 and CD2 can also be accessed on a per channel basis and be read by Local Command 9.

In GCI operation, CD1 and CD2 data for each channel can be obtained in the field of upstream C/I octet. Refer to GCI Interface Description in Appendix.

2. I/O3 and I/O4

SLIC I/O pin I/O3 for each channel can be configured as input or output seperately, by Global Command 14. Each bit in this command corresponds to one channel's I/O3. When a bit in this command is set to '0', the I/O3 pin of its corresponding channel is configured as an input; when the bit is set to '1', the I/O3 pin of its corresponding channel is configured as an output.

Global Command 15 determines the I/O direction of the I/O4 pins for each channel in the same way.

When I/O3 and I/O4 are selected as inputs, they can be read in two ways: globally for all 8 channels, or locally for each individual channel.

For global read, NW1068 provides 2 registers for I3 and I4 data of all eight channels. They can be accessed by Global Command 12 and 13 at any time regardless of the channel program enable state. They are available in both MPI and GCI operations.

The eight I3 bits of Global Command 12 represents the I3 signal on corresponding channels, while the eight I4 bits of Global Command 13 represents the I4 signal on corresponding channels.

I3 and I4 can also be read on a per channel basis and be read by Local Command 9.

In GCI operation, I3 data for each channel can be read in the field of upstream C/I octet. Refer to GCI Interface Description in Appendix. But I4 data can only be read by Global Command 13.

When I/O3 and I/O4 are configured as outputs, they are written in different ways in MPI operation and GCI operation.

In MPI operation, only Global Command 12 and 13 can write data into O3 and O4 pins for all 8 channels. NW1068 provides 2 registers for O3 and O4 data of all eight channels. They can be accessed by Global Command 12 and 13 at any time regardless of the channel program enable state.

The eight O3 bits of Global Command 12 represents the O3 data for corresponding channels, while the eight O4 bits of Global Command 13 represents the O4 data for corresponding channels.

In GCI operation, O3 and O4 can only be written on a per-channel basis through the downstream C/I octet. Refer to GCI Interface Description in Appendix.

3. O5, O6 and O7

Signals on O5, O6 and O7 pins can only be written on a per-channel basis.

In MPI operation, Local Command 9 writes the 3 output pins for each channel.

In GCI operation, O5, O6 and O7 data are written through downstream C/I octet. Refer to GCI Interface Description in Appendix.

When Local Command 9 reads a channel's SLIC pins, the O5-O7 bits will be read out as the data entered in last write operation.

Debounce Filters

For each channel, NW1068 provides two debounce filter circuits: Debounced Switch Hook (DSH) Filter for CD1 and Ground Key (GK) Filter for CD2 as shown in Figure 4. They are used to buffer the input signals on CD1 and CD2 pins before changing the state of the SLIC Debounced Input CD1/ CD2 Registers (Global Command 10 and 11), or, before changing the state of the GCI upstream C/I octet. Frame Sync (FS) is necessary for both DSH filter and GK filter.

DSH Debounce bits in Local Command 4 can program the debounce time of CD1 input from SLIC on individual channel. The DSH filter is initially clocked at the frame sync rate of 125 µs, and any data changing at this sample rate resets a programmable counter. The counter clocks at the rate of 1 ms, and the count value can be varied from 1 to 16 which is determined by Local Command 4. The corresponding CDA bit in the SLIC Debounced Input CD1 Register (accessed by Global Command 10), and the corresponding channel's CD1 bit in GCI upstream C/I octet would not be updated with the CD1 input state until the count value is reached. CD1 bit usually contains SLIC switch hook status.

GK Debounce bits in Local Command 4 can program the debounce time of CD2 input from SLIC on corresponding channel. The debounced signal will be output to CDB of SLIC Debounced Input CD2 Register (accessed by Global Command 11) and the corresponding channel's CD2 bit in GCI upstream C/I octet. The GK debounce filter consists of an up/down counter that ranges between 0 and 6. This six-state counter is clocked by the GK timer at the sampling period of 0-15 ms, as programmed by Local Command 4. When the sampled value is low, the counter is decremented by each clock pulse. When the sampled value is high, the counter is incremented by each clock pulse. When the counter increments to 6, it sets a latch whose output is routed to the corresponding CDB bit and GCI upstream C/I octet CD2 bit. If the counter decrements to 0, this latch is cleared and the output bit is set to 0. In other cases, the latch, the CDB status and the CD2 bit in GCI upstream C/I octet remain in their previous state without being changed. In this way, at least six consecutive GK clocks with the debounce input remaining at the same state to effect an output change.

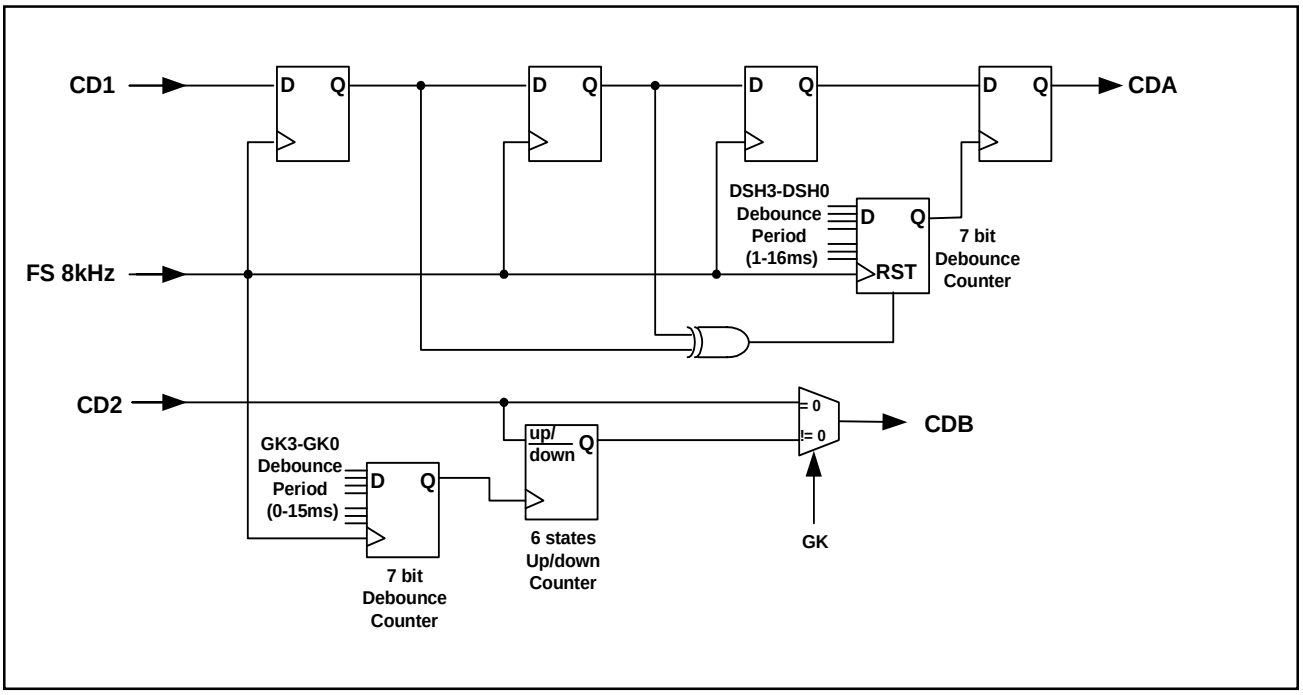


Figure 6. Debounce Filters

Dual Tone and Ring Generation

Each channel of NW1068 has two tone generators, Tone0 generator and Tone1 generator, which can produce a gain-adjustable dual tone signal and output it on VOUT pin. The dual tone signal can be used for the signal generations such as test, DTMF, dial tone, busy tone, congestion tone and Caller-ID Alerting Tone etc.

The Tone0 generator and Tone1 generator of each channel can be enabled or disabled independently by setting the T0E and T1E bits in Local Command 6. The frequency of the tones generated can be programmed from 1 Hz to 4.095 kHz with 4095 steps. Local Command 5 provides 12 bits for each tone generator to set the frequency.

The gain of the Tone0 and Tone1 signal of each channel is programmed by the TG[5:0] bits in Local Command 6, in the range of -3 dB to -39 dB. The gain of each tone can calculated by the formula below:

$$G = 20 \times \lg (Tg \times 2/256) + 3.14$$

where, Tg is the decimal value of TG[5:0].

The Dual Tone Output Invert bit (TOI) of Global Command 20 can invert the output tone signal. When it's '0', it means no inversion; when it's '1', the output tone signal will be inverted.

Ring signal is a special signal generated by the dual tone generators. When only one tone generator is enabled or both tone generators produce the same tone, and frequency of the tone is set as ring signal required (10 Hz to 100 Hz), the VOUT pin will output the Ring signal.

FSK Signal Generation

The NW1068 provides a FSK signal generator for Caller ID. This function block will be enabled when FSK On/Off bit (FO) is set '1' in Global Command 25. The FSK signal of NW1068 follows the BELL 202 and CCITT V.23 specifications. The FSK Mode Select bit (FMS) in Global Command 25 makes the selection.

Item	BT	Bellcore
Mark(1) frequency	1300 Hz ± 1.5%	1200Hz ± 1.1%
Space (0) frequency	2100 Hz ± 1.1%	2200 Hz ± 1.1%
Transmission rate	1200 baud ± 1%	1200 baud ± 1 %
Word format	1 start bit which is '0', 8 word bits (with least significant bit LSB first), 1 stop bit which is '1'	1 start bit which is '0' 8 word bits (with least significant bit LSB first) 1 stop bit which is '1'

The structure of FSK signal is determined by Flag Length, Data Length, Seizure Length and Mark Length (Global Command 21-24), while the operation of FSK signal generator is controlled by Global Command 25.

To transmit a single frame FSK signal, please follow the sequence below:
1. Check FSK Start bit (FS in Global Command 25) to see if the FSK function block is busy or idle. If this bit is '0' which means that the FSK block is idle, user can go on with the operation. If this bit is '1' which means the function block is busy, user should wait until the FSK Start bit turns to '0';
2. Set FSK Channel Sel bits (FCS[2:0] in Global Command 25) to determine which channel the FSK signal will output;
3. Set Data Length (Global Command 22), Seizure Length (Global Command 23), Mark Length (Global Command 24) and Flag Length (Global Command 21);
4. Write the FSK-RAM (see Programming Description) with the message need to be transmitted;
5. Set Mark After Send bit (MAS in Glabal Command 25) to '0';
6. Select Bellcore or BT specification by setting BT/Bellcore Sel bit (FMS bit in Global Command 25);
7. Set FSK Start bit (FS in Global Command 25) to '1'.

The FSK signal generator transmits the FSK signal in following steps:
1. Keep FSK Start bit (FS in Global Command 25) as '1';
2. Send seizure signal according to Seizure Length set by Global Command 23;
3. Send mark signal according to Mark Length set by Global Command 24;
4. Transmit one byte word in FSK RAM, add 1 to the internal transmitted counter;

5. Transmit flag signal according to Flag Length Set by Global Command 21;
6. Transmit next byte word in FSK RAM, and add 1 to transmitted counter.Transmit flag signal according to Flag Length;
7. The FSK generator will return to the 6th step until the value in the transmitted counter equals to the Data Length. When the value reaches the Data Length, the FSK generator will reset FSK Start bit to '0';
8. If Mark After Send = '1', then send mark signal. Otherwise, mute the FSK output.

To transmit a multiple frame FSK signal, please follow the sequence below:
1. Check FSK Start bit (FS in Global Command 25) to see if the FSK function block is busy or idle. If this bit is '0' which means that the FSK block is idle, user can go on with the operation. If this bit is '1' which means the function block is busy, user should wait until the FSK Start bit turns to '0';
2. Set FSK Channel Sel bits (FCS in Global Command 25) to determine which channel the FSK signal will output;
3. Set Data Length (Global Command 22), Seizure Length (Global Command 23), Mark Length (Global Command 24) and Flag Length (Global Command 21);
4. Write the FSK-RAM (see Programming Description) with the message need to be transmitted;
5. Set Mark After Send bit (MAS in Global Command 25) to '1';
6. Select Bellcore or BT specification by setting BT/Bellcore Sel bit (FMS in Global Command 25);
7. Set FSK Start bit (FS in Global Command 25) to '1';
8. Transmit the FSK signal;
9. Check FSK Start bit, if it's '0', then continue. If it's '1', then wait;
10. Fill the FSK-RAM with the message need to be transmitted;
11. Set Data Length. Set Mark length and Seizure Length to '0';
12. Set FSK Start bit to '1';
13. If the FSK signal input is finished, set Mark After Send to '0'. Otherwise, go back to step 8.

Teletax

When a '1' appears on Teletax Ramp Start bit (RS) of Local Command 10, the teletax signal will be output from the VOUT pin on the corresponding channel with a 16 ms ±10% rising time. This teletax signal will last until a '0' on the RS bit for the same channel. It has a falling time of 16 ms ±10%, as shown in Figure 7. Teletax signal is used to sum the telephone fee according to the calling time and tariff. The frequency of teletax signal carrier can be selected as 12 kHz or 16 kHz (± 50 Hz) by Global Command 20, while the amplitude of the teletax signal on specific channel can be programmed by Teletax Gain Setting bits (TGS[7:0]) in Local Command 3.

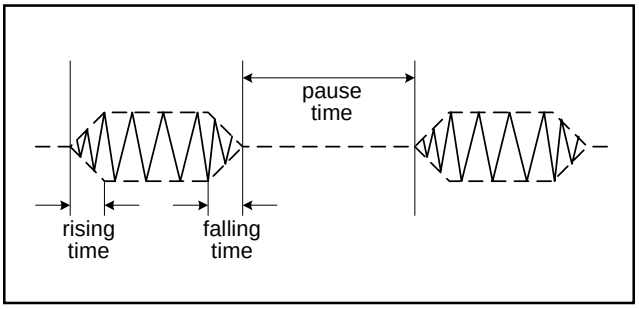


Figure 7. Teletax Signal

Level Metering

The NW1068 has a level meter which can be shared by all 8 signal channels. The level meter is designed to emulate the off-chip PCM test equipment so as to facilitate the line-card, subscriber line and user telephone set monitoring. The level metering tests the returned signal and report the measurement result via MPI/GCI interface. When combined with Tone Generation and Loop-back modes, this allows the microprocessor to test channel integrity. CS bits in Global Command 20 select the channel, signal on which will be level metered.

Level Metering function is enabled by setting LMO bit to '1' in Global Command 20. There is a Level Meter Counter register for this function. It can be accessed by Global Command 19. This register is used to configure the number of time cycles for sampling PCM data (8 kHz sampling rate). The output of Level Metering will be sent to Level Meter Result Low and Level Meter Result High registers (Global Command 17 and 18). The LMRL register contains the lower 7 bits of the output and a data-ready bit (DRLV), while the LMRH register contains the higher 8 bits of the output. An internal accummulator sums the rectified samples until the number configured by Level Meter Counter register is reached. By then, the DRLV bit is set to '1' and accumulation result is latched into the LMRL and LMRH registers simultaneously.

Once the LMRH register is read, the DRLV bit will be cleared. The DRLV bit will be set high again by a new data available. The contents in LMRL and LMRH will be overwritten by later metering result if they are not read out yet. In Level Metering result read operation, it is highly recommended to read LMRL first.

L/C bit in Global Command 20 determines the mode of Level Meter operation. When L/C bit is '1', the Level Meter will measure the Linear PCM data, and if DRLV bit is '1' , the measure result will be output to LMRL and LMRH. When L/C bit is '0', compressed PCM will be output transparantly to LMRH.

The detail calculation and method of level metering will be described in Application Note, which will be published later.

Hardware Ring-Trip

In order to protect the ring circuit from the impact of long-period large current on the line, the NW1068 offers a hardware ring-trip function to respond to the off-hook signal as fast as possible. This function can be enabled by setting RTE bit to '1' in Global Command 16.

The off-hook signal can be input via any of CD1 or CD2, while the ring control signal can be output via any of O7, O6, O5, I/O4 (when it's configured as output) and I/O3 (when it's configured as output). In Global Command 16, IS bit determines which input is used and OS bits determine which output is used.

When a valid off-hook signal arrives on CD1 or CD2, the NW1068 will turn off the ring signal by inverting the selected output, in spite of the corresponding value for this output stored in register. This function provides a much faster response to off-hook signal than the software ring-trip which turns off the ring signal by changing the value of selected output in the corresponding register.

The IPI bit in Global Command 16 is used to indicate the valid polarity of input. If the off-hook signal is low active, the IPI should be set to '0'; if the off-hook signal is high active, the IPI should be set to '1'.

The OPI bit in Global Command 16 is used to indicate the valid polarity of output. If the ring control signal is required to be low in normal status and be high to activate a ring, the OPI should be set to '1'; if it is required to be high in normal status and be low to activate a ring, the OPI should be set to '0'.

For example, in a system where the off-hook signal is low active and ring control signal is normally low and high active, the IPI in Global Command 16 should be set to '0' and the OPI bit should be set to '1'. In normal status, the selected input is high and the selected output is low. When the output is turned to high and the ring is activated, a low pulse appearing on the input (off-hook signal) will inform the device to invert the output to low and cut off the ring signal.

Chopper Clock

NW1068 offers two programmable chopper clock outputs: CHCLK1 and CHCLK2. Both CHCLK1 and CHCLK2 are synchronous to MCLK. CHCLK1 outputs signal with programmable 2-28 ms clock cycle, while the frequency of CHCLK2 can be any of 256 kHz, 512 kHz and 16.384 MHz. The frequency selection of chopper clocks can be implemented by Global Command 9. The chopper clocks can be used to drive the power supply switching regulators on SLICs.

Interrupt and Interrupt Mask

An interrupt mechanism is offered in NW1068 for reading the SLIC input status. Each SLIC input generates interrupt respectively when it changes state. An interrupt mask is selectable for each interrupt source to disable its interrupt ability. The interrupt signal can be cleared by Global Command 3 Interrupt Clear.

Any of CD1, CD2, I/O3 and I/O4 (when they are configured as inputs) can be interrupt source. As CD1 and CD2 are debounced signals while I/O3 and I/O4 are not, more attention is needed when I/O3 and I/O4 are selected as interrupt sources.

There is a four bit Interrupt Mask Register for each channel in NW1068. The register can be programmed by Local Command 2. Each bit of the register corresponds to one interrupt source on the specific channel. The device will ignore the interrupt signal on an input when its corresponding bit in Interrupt Mask Register is set to '1'.

Multiple interrupt sources can be enabled at the same time, while all of them can be cleared by applying an Interrupt Clear Command (Global Command 3).

Channel Power Down/Standby Mode (MPI,GCI Only)

Each individual channel of NW1068 can be powered down independently by Local Command 10. When the channel is powered down (enters into standby mode), PCM data transmission and reception, D/A and A/D are disabled. In this way, power consumption of the device can be reduced. When NW1068 is powered up or reset, all eight channels will be powered down. All circuits that contain programmed information retain their data when powered down. In MPI operation, MPI (Microprocessor Interface) is always active so that new command could be received and executed. In GCI operation, the monitor channel of any timeslot is always on so that new command could be accepted at any time.

Power Down PLL/Suspend Mode

A suspend mode is offered to the whole chip to save power. In this mode, the PLL block is turned off and DSP operation is disabled. This mode saves much more power consumption than standby mode. In this mode, only Global Command and Local Command can be executed. RAM operation is disabled as internal clock has been turned off. Suspend mode can be entered by Global Command 26 which powers down PLL, after all channels have been powered down.

Signal Processing

High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) are used in the NW1068 to provide the required conversion accuracy. The associated decimation and interpolation filters are realized with both dedicated hardware and Digital Signal Processor (DSP). The DSP also handles all other necessary functions such as PCM bandpass filtering, sample rate conversion, impedance matching, echo cancellation and gain adjustment. See Figure 8.

Transmit Signal Processing For MPI Operation

In the transmit path, the analog input signal is converted to PCM code by ADC, DSP and PCM companding circuits. The PCM code is transmitted at the rate of 8,000 samples per second. After conversion, it is available for outputting to PCM highway. Band-limiting functions as specified in ITU-T are implemented by digital filters.

Receive Signal Processing for MPI Operation

In the receive path, the PCM code is received at the rate of 8,000 samples per second. The PCM code is expanded and sent to the DSP for interpolation and receive channel filtering function. The filtered signal is then sent to an oversampling DAC. The DAC output is post-filtered and then delivered at VOUT pin by a power amplifier. The amplifier can drive resistive load higher than 300 Ω.

Data Upstream Interface for GCI Operation

In GCI Compressed operation, the Data Upstream Interface transmits a total of four 8-bit bytes per GCI timeslot. Two bytes are from the A-law or μ-law compressor: one for voice channel A, one for voice channel B; A single Monitor channel byte and a single C/I channel byte. Transmit logic controls the transmission of data onto the GCI bus as determined by the TS pin.

In GCI Linear operation, the Data Upstream Interface transmits a total of four 8-bit bytes per GCI timeslot. Each GCI frame consists of 8 GCI timeslots. 4 timeslots are used for monitor and C/I octet, whereas the rest 4 timeslots are used for GCI Linear data. The timeslot selection is determined by TS pin.

The FS signal identifies GCI Timeslot0 and all GCI timeslots are referenced to it. Upstream Data is always transmitted at a 2.048 MHz data rate.

Refer to GCI Interface Description in appendix.

Data Downstream Interface for GCI Operation

In GCI Compressed operation, the Data Downstream Interface logic controls the reception of data bytes from the GCI highway. The GCI timeslots received by the NW1068 is determined by the TS pin. The two compressed voice channel data bytes of the GCI time slot are transferred to the A-law or μ-law expansion logic circuit. The expanded data is passed to the receive path of the signal processor. The Monitor Channel and C/I Channel bytes are transferred to the GCI control logic for processing.

In GCI Linear operation, the Data Downstream Interface logic controls the reception of data bytes from the GCI highway. The GCI timeslots for GCI Linear data received by the NW1068 is determined by the TS pin. The data is passed to the receive path of the signal processor. The Monitor Channel and C/I Channel bytes are transferred to the GCI control logic for processing.

Refer to GCI Interface Description in appendix.

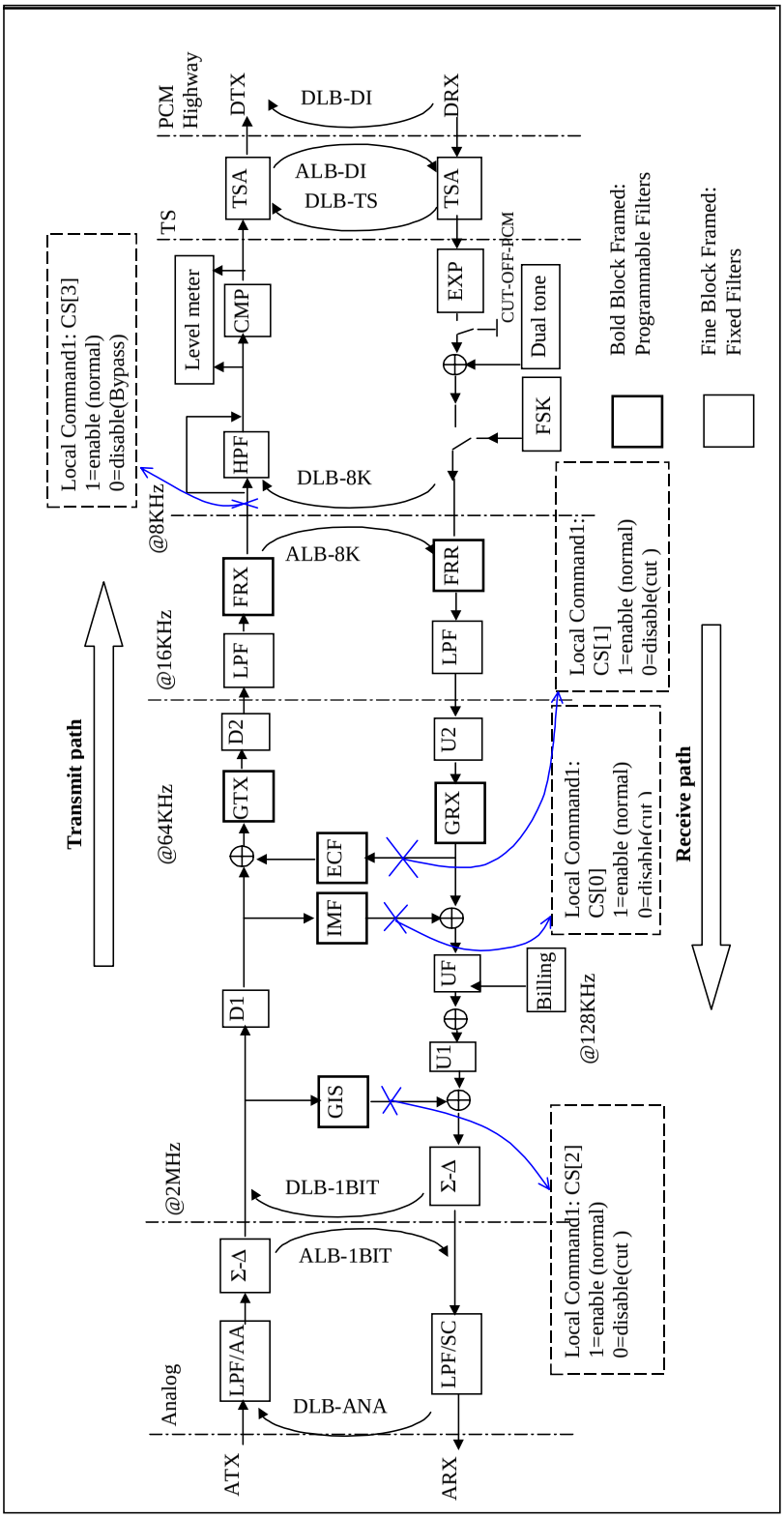


Figure 8. Signal Flow for Each Channel

Abbreviation List

LPF/AA: Anti-Alias Low-pass Filter
LPF/SC: Smoothing Low-pass Filter
LPF: Low-pass Filter
HPF: High-pass Filter
GIS: Gain for Impedance Scaling
D1: 1st Down Sample Stage
D2: 2nd Down Sample Stage
U1: 1st Up Sample Stage
U2: 2nd Up Sample Stage
UF: Up Sampling Filter (64k-128k)

IMF: Impedance Matching Filter
ECF: Echo Cancellation Filter
GTX: Gain for Transmit Path
GRX: Gain for Receive Path
FRX: Frequency Response Correction for Transmit
FRR: Frequency Response Correction for Receive
CMP: Compression
EXP: Expansion

Command and Register List

$\overline{R}$/W = 0: Read $\overline{R}$/W = 1: Write
R means Reserved for future use. Always write as 0, read as don't_care.

When a command is executed, the NW1068 will read or write its corresponding register as shown in this list.

MPI/GCI Global Command and Register List

1. No Operation (A0H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	0	0

2. Version Number (20H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	0	0	0	0

By this command, users can read out the version number of the NW1068.

3. Interrupt Clear (A1H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	0	1

All interrupts on SLIC I/O will be cleared by this command.

4. Software Reset (A2H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	0

This command only resets the Local Registers of those channels selected by Channel Program Enable (Global Command 7).

5. Hardware Reset (A3H), Write Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	1	0	1	0	0	0	1	1

This command is equivalent to pulling $\overline{RESET}$ pin low.

6. MCLK Select (24H/A4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W[NOTE1]	0	1	0	0	1	0	0
I/O data	R[NOTE2]	R	R	R	Sel[3]	Sel[2]	Sel[1]	Sel[0]

This command is used to determine the frequency of Master Clock which is affective to all channels.
Master Clock Frequency:
Sel = 0000: 8.192 MHz
Sel = 0001: 4.096 MHz
Sel = 0010: 2.048 MHz (default)
Sel = 0110: 1.536 MHz
Sel = 1110: 1.544 MHz
Sel = 0101: 3.072 MHz
Sel = 1101: 3.088 MHz
Sel = 0100: 6.144 MHz
Sel = 1100: 6.176 MHz

7. Channel Program Enable (25H/A5H), not availabe in GCI operation, Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	0	1
I/O data	CE[7]	CE[6]	CE[5]	CE[4]	CE[3]	CE[2]	CE[1]	CE[0]

Enable Channel N, default value is 0(d) which means all channel disabled. When Channel N is selected, the subsequent Local Commands will be effective to the selected channel.

CE[N] = 0: Disabled, Channel N can't be programmed by Local Commands

CE[N] = 1: Enabled, Channel N can be programmed by Local Commands

8. PCM Data Offset, PCM Clock Slope, Data Mode Select, not available in GCI operation, and A/μ-Law Select (26H/A6H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	0
I/O data	LS	DMS	CS[2]	CS[1]	CS[0]	DO[2]	DO[1]	DO[0]

PCM Data Offset bits (DO[2:0]) configure the number of clocks that PCM data transmit and receive timeslot is offset from FS.

DO = 000: 0 BCLK period (default);
DO = 001: 1 BCLK period;
DO = 010: 2 BCLK periods;
DO = 011: 3 BCLK periods;
DO = 100: 4 BCLK periods;
DO = 101: 5 BCLK periods;
DO = 110: 6 BCLK periods;
DO = 111: 7 BCLK periods.

PCM Clock Slope (CS[2:0]) bits select transmit and receive clock edge.

CS[2] = 0: single clock (default);
CS[2] = 1: double clock;
CS[1:0] = 00: NW1068 transmits data on rising edges of BCLK, and receives data on falling edges of BCLK (default);
CS[1:0] = 01: NW1068 transmits data on rising edges of BCLK, and receives data on rising edges of BCLK;
CS[1:0] = 10: NW1068 transmits data on falling edges of BCLK, and receives data on falling edges of BCLK;
CS[1:0] = 11: NW1068 transmits data on falling edges of BCLK, and receives data on rising edges of BCLK.

Data Mode Select bit (DMS) defines the coding of the voice data.

DMS = 0: compressed code (default);
DMS = 1: linear code.

A/μ-law Select bit (LS) selects A-law or μ-law.

LS = 0: A-law (default);
LS = 1: μ-law.

9. Chopper Clock Select (27H/A7H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	0	1	1	1
I/O data	R	R	CHCLK2_SEL[1]	CHCLK2_SEL[0]	CHCLK1_SEL[3]	CHCLK1_SEL[2]	CHCLK1_SEL[1]	CHCLK0_SEL[0]

CHCLK1_SEL bits configure the programmable output pin CHCLK1.

CHCLK1_SEL = 0000: CHCLK1 outputs 1 permanently (default);
CHCLK1_SEL = 0001: CHCLK1 outputs digital signal at the frequency of 1000/2 Hz;
CHCLK1_SEL = 0010: CHCLK 1 outputs digital signal at the frequency of 1000/4 Hz;
CHCLK1_SEL = 0011: CHCLK1 outputs digital signal at the frequency of 1000/6 Hz;
CHCLK1_SEL = 0100: CHCLK1 outputs digital signal at the frequency of 1000/8 Hz;
CHCLK1_SEL = 0101: CHCLK 1 outputs digital signal at the frequency of 1000/10 Hz;
CHCLK1_SEL = 0110: CHCLK1 outputs digital signal at the frequency of 1000/12 Hz;
CHCLK1_SEL = 0111: CHCLK1 outputs digital signal at the frequency of 1000/14 Hz;
CHCLK1_SEL = 1000: CHCLK 1 outputs digital signal at the frequency of 1000/16 Hz;
CHCLK1_SEL = 1001: CHCLK1 outputs digital signal at the frequency of 1000/18 Hz;
CHCLK1_SEL = 1010: CHCLK1 outputs digital signal at the frequency of 1000/20 Hz;
CHCLK1_SEL = 1011: CHCLK 1 outputs digital signal at the frequency of 1000/22 Hz;
CHCLK1_SEL = 1100: CHCLK1 outputs digital signal at the frequency of 1000/24 Hz;
CHCLK1_SEL = 1101: CHCLK1 outputs digital signal at the frequency of 1000/26 Hz;
CHCLK1_SEL = 1110: CHCLK 1 outputs digital signal at the frequency of 1000/28 Hz;
CHCLK1_SEL = 1111: CHCLK1 outputs 0 permanently.

CHCLK2_SEL bits configure the programmable output pin CHCLK2.

CHCLK2_SEL = 00: CHCLK2 outputs 1 permanently (default);
CHCLK2_SEL = 01: CHCLK2 outputs digital signal at the frequency of 512 kHz;
CHCLK2_SEL = 10: CHCLK2 outputs digital signal at the frequency of 256 kHz;
CHCLK2_SEL = 11: CHCLK2 outputs digital signal at the frequency of 16.384 MHz.

10. SLIC Debounced Input CD1 (28H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	0
I/O data	CDA[7]	CDA[6]	CDA[5]	CDA[4]	CDA[3]	CDA[2]	CDA[1]	CDA[0]

CDA bits contain SLIC loop-detect status which SLIC Interface Pin CD1 receives. The value of CDA [N] represents the debounced data on Channel N. Default value is 0(d).

11. SLIC Debounced Input CD2 (29H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	0	1	0	0	1
I/O data	CDB[7]	CDB[6]	CDB[5]	CDB[4]	CDB[3]	CDB[2]	CDB[1]	CDB[0]

CDB bits contain SLIC ground key status which SLIC Interface Pin CD2 receives. The value of CDB[N] represents the debounced data bit on Channel N. Default value is 0(d).

12. SLIC Real-time I/O3 (AAH/2AH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	0	1	0
I/O data	I/O3[7]	I/O3[6]	I/O3[5]	I/O3[4]	I/O3[3]	I/O3[2]	I/O3[1]	I/O3[0]

I/O3 bits contain the information of SLIC bidirectional pin I/O3. The value of I/O3[N] represents the I/O3 data bit on Channel N. Default value is 0(d).

MPI/GCI Global Command List (Continued)

13. SLIC Real-time I/O4 (2BH/ABH), Read/Write

	B7	B6	B5	B4	B3	B2	B1	B0
Command	$\overline{R}$/W	0	1	0	1	0	1	1
I/O data	I/O4[7]	I/O4[6]	I/O4[5]	I/O4[4]	I/O4[3]	I/O4[2]	I/O4[1]	I/O4[0]

I/O4 bits contain the information of SLIC bi-direnctional pin I/O4. The value of I/O4[N] represents the I/O4 data bit on Channel N. Default value is 0(d).

14. I/O3 Direction (2CH/ACH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	0	0
I/O data	I/O3C[7]	I/O3C[6]	I/O3C[5]	I/O3C[4]	I/O3C[3]	I/O3C[2]	I/O3C[1]	I/O3C[0]

SLIC I/O3 Direction bits (I/O3C) configure the direction of SLIC interface pin I/O3. Default value is 0(d).
I/O3C[N] = 0: I/O3 pin of Channel N is configured as an input;
I/O3C[N] = 1: I/O3 pin of Channel N is configured as an output.

15. I/O4 Direction (2DH/ADH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	0	1
I/O data	I/O4C[7]	I/O4C[6]	I/O4C[5]	I/O4C[4]	I/O4C[3]	I/O4C[2]	I/O4C[1]	I/O4C[0]

SLIC I/O4 Direction bits (IO4C) configure the direction of SLIC interface pin I/O4. Default value is 0(d).
I/O4C[N] = 0: I/O4 pin of Channel N is configured as an input;
I/O4C[N] = 1: I/O4 pin of Channel N is configured as an output.

16. SLIC Ring Trip Setting (2EH/AEH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	0	1	1	1	0
I/O data	OPI	R	IPI	IS	RTE	OS[2]	OS[1]	OS[0]

Output Selection bits OS[2:0] determine which output will be selected as the ring control signal source.
OS = 000 - 010: not defined;
OS = 011: I/O3 is selected (when it's configured as an output);
OS = 100: I/O4 is selected (when it's configured as an output);
OS = 101: O5 is selected;
OS = 110: O6 is selected;
OS = 111: 07 is selected.
Ring Trip Enable bit RTE enables or disables the ring trip function block:
RTE = 0: the ring trip function block is disabled (default);
RTE = 1: the ring trip function block is enabled.
Input Selection bit IS determines which input will be selected as the off-hook indication signal source.
IS = 0: CD1 is selected (default); IS = 1: CD2 is selected.
Input Polarity Indicator bit IPI indicates the valid polarity of input.
IPI = 0: low active (default); IPI = 1: high active.
Output Polarity Indicator bit OPI indicates the valid polarity of output.
OPI = 0: the selected output pin changes from high to low to activate the ring (default);
OPI = 1: the selected output pin changes from low to hight to activate the ring.

17. Level Meter Result Low Register (30H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	0
I/O data	LMRL[7]	LMRL[6]	LMRL[5]	LMRL[4]	LMRL[3]	LMRL[2]	LMRL[1]	DRLV

This register contains the lower 7 bits of Level Meter output and a data-ready bit with the default value of 0(d). DRLV is the high active data-ready bit. While LMRH is read, this bit is cleared immediately.

18. Level Meter Result High Register (31H), Read Only

	b7	b6	b5	b4	b3	b2	b1	b0
Command	0	0	1	1	0	0	0	1
I/O data	LMRH[7]	LMRH[6]	LMRH[5]	LMRH[4]	LMRH[3]	LMRH[2]	LMRH[1]	LMRH[0]

This register contains the higher 8 bits of Level Metering output with the default value of 0(d).

19. Level Meter Counter (32H/B2H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	1	0
I/O data	CN[7]	CN[6]	CN[5]	CN[4]	CN[3]	CN[2]	CN[1]	CN[0]

Level Meter Counter register is used to configure the number of time cycles for sampling PCM data.

CN = 0 (d): the linear or compressed PCM data is output to LMRH and LMRH directly (default);

CN = N: PCM data is sampled for N * 125 μs (N from 1 to 255).

20. Level Meter Channel Select, Level Meter Mode Select, Level Meter On/off, Teletax Pulse Frequency and Dual Tone Output Invert (33H/B3H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	1	1
I/O data	R	TOI	TF	LMO	L/C	CS[2]	CS[1]	CS[0]

Level Meter Channel Select bits (CS[3:0]) select the channel, data on which will be level metered.

CS = 000: Channel 0 is selected (default);
CS = 001: Channel 1 is selected;
CS = 010: Channel 2 is selected;
CS = 011: Channel 3 is selected;
CS = 100: Channel 4 is selected;
CS = 101: Channel 5 is selected;
CS = 110: Channel 6 is selected;
CS = 111: Channel 7 is selected.

Level Meter Mode Select bit (L/C) determines the mode of level meter operation.

L/C = 0: Message mode is selected. Compressed PCM will be output to LMRH transparently (default);

L/C = 1: Meter mode is selected. Linear PCM data will be metered and output to LMRH and LMRL, when data_ready bit in LMRL register is '1'.

Level Meter On/off bit (LMO) enables the level meter.

LMO = 0: Level meter is disabled (default);
LMO = 1: Level meter is enabled.

Teletax Pulse Frequency bit (TF) selects the frequency of teletax pulse.

TF = 0: Teletax pulse frequency is 16 kHz (default);
TF = 1: Teletax pulse frequency is 12 kHz.

Dual Tone Output Invert bit (TOI) determines whether output tone signal will be inverted or not.

TOI = 0: no inversion (default);
TOI = 1: output signal is inverted.

MPI/GCI Global Command List (Continued)

21. FSK Flag Length (34H/B4H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	0	0
I/O data	FL[7]	FL[6]	FL[5]	FL[4]	FL[3]	FL[2]	FL[1]	FL[0]

Flag Length bits (FL[7:0]) determine the number of flag bits '0' which will be transmitted between the transmission of message bytes. The default value is 0(d).

22. FSK Data Length (35H/B5H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	0	0	1
I/O data	WL[7]	WL[6]	WL[5]	WL[4]	WL[3]	WL[2]	WL[1]	WL[0]

Data Length bits (WL[7:0]) determine the number of all the data bits which will be transmitted except flag. The value is valid from 0 to 64(d). Any value larger than 64(d) will be taken as 64(d) by the CPU.
The default value of this register is 0(d). When 0(d) is selected, none of the word data will be sent out. When Mark After Send (MAS bit in Global Command 25) is set to '1', the mark signal will be sent; while Mark After Send is set to '0', the transmission of mark signal will be terminated.

23. FSK Seizure Length (36H/B6H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	0	1	1	0
I/O data	SL[7]	SL[6]	SL[5]	SL[4]	SL[3]	SL[2]	SL[1]	SL[0]

Seizure Lengh bits (SL[7:0]) determine the number of '01' pairs which represent seizure phase. The default value is 0(d). When 0(d) is selected, no seizure signal will be sent.

24. FSK Mark Length (37H/B7H), Read/Write

	B7	B6	B5	B4	B3	B2	B1	B0
Command	$\overline{R}$/W	0	1	1	0	1	1	1
I/O data	ML[7]	ML[6]	ML[5]	ML[4]	ML[3]	ML[2]	ML[1]	ML[0]

Mark Length bits (ML[7:0]) determine the number of mark bits '1' which will be transmitted in initial flag phase. The default value is 0(d). When 0(d) is selected, no mark signal will be sent.

25. FSK Start, Mark After Send, FSK Mode Select, FSK Channel Select and FSK On/Off (38H/B8H), Read/ Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	0	0	0
I/O data	FO	FCS[2]	FCS[1]	FCS[0]	R	FMS	MAS	FS

FSK Start bit (FS) should be set to '1' when user is going to send out FSK data. It will be cleared TO the default value '0' at the end of word data. When Seizure Length, Mark Length together with Data Length bits are all set to 0(d), the FSK Start bit will be reset to '0' immediately after it is set to '1'.
Mark After Send bit (MAS) determine the FSK block operation after the word data has been sent.

MAS = 0: The output will be muted after sending out word data (default);

MAS = 1: The carrier (seizure signal, data signal or mark signal) will be always valid after a '1' on FSK Start bit until MAS is set back to '0'. After the MAS bit is set to '0', a '1' on MAS will not work until a '1' on FSK Start bit.

FSK Mode Select bit (FMS) determines which specification the NW1068 follow:

FMS = 0: Bellcore specification is selected (default);

FMS = 1: BT specification is selected.

FSK Channel Select bits (FCS[2:0])selects the channel on which FSK operation will be implemented.

FCS = 000: Channel 0 is selected (default);

FCS = 001: Channel 1 is selected;

FCS = 010: Channel 2 is selected;

FCS = 011: Channel 3 is selected;

FCS = 100: Channel 4 is selected;

FCS = 101: Channel 5 is selected;

FCS = 110: Channel 6 is selected;

FCS = 111: Channel 7 is selected.

FSK On/Off (FO) enables or disables the whole FSK function block.

FO = 0: FSK is disabled (default);

FO = 1: FSK is enabled.

26. Loop Control and PLL Power Down (3CH/BCH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	1	1	1	1	0	0
I/O data	R	PLLPD	R	LP[4]	LP[3]	LP[2]	LP[1]	LP[0]

Loop Control bits (LP[4:0]) determine the loopback status. Refer to Figure 5 for detail information.

LP[0] = 0: Analog Loopback via PCM Highway is disabled (default);

LP[0] = 1: Analog Loopback via PCM Highway is enabled;

LP[1] = 0: Digital Loopback via PCM Highway is disabled (default);

LP[1] = 1: Digital Loopback via PCM Highway is enabled;

LP[2] = 0: Digital Loopback via 8 kHz Interface is disabled (default);

LP[2] = 1: Digital Loopback via 8 kHz Interface is enabled;

LP[3] = 0: Analog Loopback via 8 kHz Interface is disabled (default);

LP[3] = 1: Analog Loopback via 8 kHz Interface is enabled;

LP[4] = 0: Digital Loopback via Analog Interface is disabled (default);

LP[4] = 1: Digital Loopback via Analog Interface is enabled.

PLL Power Down Bit (PLLPD) controls the status of Phase Lock Loop.

PLLPD = 0: the device is in normal operation (default);

PLLPD = 1: Phase Lock Loop is powered down. The device works in Power-Saving mode. All clocks stop running.

MPI/GCI Local Command List

1. Coefficient Select (00H/80H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	0	0
I/O data	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]

Coefficient Select bits (CS[7:0]) are used to control digital filters and function blocks on corresponding channel such as Impedance Matching Filter, Echo Cancellation Filter, High-Pass Filter, Gain for Impedance Scaling, Gain in Transmit/Receive Path and Frequency Response Correction in Transmit/Receive Path. See Figure 5 for detail. It should be noted that Impedance Matching Filter and Gain for Impedance Scaling are working together to adjust impedance. That is to say, CS [0] and CS[2] should be set to the same value to ensure the correct operation.

CS [0] = 0: Impedance Matching Filter is disabled (default);
CS [0] = 1: Impedance Matching Filter coefficient is set by IMF RAM;
CS [1] = 0: Echo Cancellation Filter is disabled (default);
CS [1] = 1: Echo Cancellation Filter coefficient is set by ECF RAM;
CS [2] = 0: Gain for Impedance Scaling is disabled (default);
CS [2] = 1: Gain for Impedance Scaling coefficient is set by GIS RAM;
CS [3] = 0: High-Pass Filter is bypassed/disabled;
CS [3] = 1: High-Pass Filter is enabled (default);
CS [4] = 0: Frequency Response Correction in Transmit Path is bypassed (default);
CS [4] = 1: Frequency Response Correction in Transmit Path coefficient is set by FRX RAM;
CS [5] = 0: Gain in Transmit Path is 0 dB (default);
CS [5] = 1: Gain in Transmit Path coefficient is set by GTX RAM;
CS [6] = 0: Frequency Response Correction in Receive Path is bypassed (default);
CS [6] = 1: Frequency Response Correction in Receive Path coefficient is set by FRR RAM;
CS [7] = 0: Gain in Receive Path is 0 dB (default);
CS [7] = 1: Gain in Receive Path coefficient is set by GRX RAM.

Note: The mapping method of RAM can be found in Coefficient Memory Address Mapping (Page 55).

2. Loop Status Control, PCM Receive Path Cut-off and SLIC Input Interrupt Mask (01H/81H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	0	1
I/O data	IM[3]	IM[2]	IM[1]	IM[0]	PCF	LPC[2]	LPC[1]	LPC[0]

Loop Status Control Bits (LPC[2:0]) determine the loopback status on corresponding channel. Refer to Figure 5 for detail information.

LPC[0] = 0: Digital Loopback via Onebit is disabled on the corresponding channel (default);
LPC[0] = 1: Digital loopback via Onebit is enabled on the corresponding channel;
LPC[1] = 0: Analog Loopback via Onebit is disabled on the corresponding channel (default);
LPC[1] = 1: Analog Loopback via Onebit is enabled on the corresponding channel;
LPC[2] = 0: Digital Loopback via Timeslots is disabled on the corresponding channel (default);
LPC[2] = 1: Digital Loopback via Timeslots is enabled on the corresponding channel. In this loopback mode, the digital data received from DR will be switched by the timeslot setting, and then will be transmitted out from DX pin.

PCM Receive Path Cut-off bit (PCF) is used to cut off the PCM receive path, see Figure 5.

PCF = 0: PCM Receive Path in normal operation; PCF = 1: PCM Receive Path is cut off.

SLIC Input Interrupt Mask bits (IM[3:0]) can enable the device to ignore the interrupt signal on corresponding channel.

IM[0] = 0: interrupt signal on I/O4 (when it is selected as an input) will be recognized (default);
IM[0] = 1: interrupt signal on I/O4 (when it is selected as an input) will be ignored;

IM[1] = 0: interrupt signal on I/O3 (when it is selected as an input) will be recognized (default);
IM[1] = 1: interrupt signal on I/O3 (when it is selected as an input) will be ignored;
IM[2] = 0: interrupt signal on CD2 will be recognized (default);
IM[2] = 1: interrupt signal on CD2 will be ignored;
IM[3] = 0: interrupt signal on CD1 will be recognized (default);
IM[3] = 1: interrupt signal on CD1 will be ignored;

3. Teletax Gain Setting (02H/82H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	1	0
I/O data	TGS[7]	TGS[6]	TGS[5]	TGS[4]	TGS[3]	TGS[2]	TGS[1]	TGS[0]

Teletax Gain Setting bits (TGS[7:0]) are used to set the gain of teletax on corresponding channel. The default value is '00H' which means the gain is 0, 'FFH' represents the gain of 1. There are totally 255 steps between gain 0 and 1 corresponding to the value of the command I/O data.

4. DSH Debounce and GK Debounce (03H/83H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	0	1	1
I/O data	GK[3]	GK[2]	GK[1]	GK[0]	DSH[3]	DSH[2]	DSH[1]	DSH[0]

DSH Debounce bits (DSH[3:0]) set the debounce time of CD1 input from SLIC on corresponding channel.
DSH = 0000: 0 ms (default);
DSH = 0001: 1 ms;
DSH = 0010: 2 ms;
DSH = 0011: 3 ms;
DSH = 0100: 4 ms;
DSH = 0101: 5 ms;
DSH = 0110: 6 ms;
DSH = 0111: 7 ms;
DSH = 1000: 8 ms;
DSH = 1001: 9 ms;
DSH = 1010: 10 ms;
DSH = 1011: 11 ms;
DSH = 1100: 12 ms;
DSH = 1101: 13 ms;
DSH = 1110: 14 ms;
DSH = 1111: 15 ms.
GK Debounce bits (GK[3:0]) set the debounce time of CD2 input from SLIC on corresponding channel.
GK = 0000: 0 ms (default);
GK = 0001: 1 ms;
GK = 0010: 2 ms;
GK = 0011: 3 ms;
GK = 0100: 4 ms;
GK = 0101: 5 ms;
GK = 0110: 6 ms;
GK = 0111: 7 ms;
GK = 1000: 8 ms;
GK = 1001: 9 ms;
GK = 1010: 10 ms;
GK = 1011: 11 ms;

MPI/GCI Local Command List (Continued)

GK = 1100: 12 ms;
GK = 1101: 13 ms;
GK = 1110: 14 ms;
GK = 1111: 15 ms.

5. Dual Tone Frequency Setting (04,05,06H/84,85,86H), Read/Write

	B7	B6	B5	B4	B3	B2	B1	B0
Command	$\overline{R}$/W	0	0	0	0	1	0	0
I/O data	T0[7]	T0[6]	T0[5]	T0[4]	T0[3]	T0[2]	T0[1]	T0[0]

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	0	1
I/O data	T1[3]	T1[2]	T1[1]	T1[0]	T0[11]	T0[10]	T0[9]	T0 [8]

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	1	0
I/O data	T1[11]	T1[10]	T1[9]	T1[8]	T1[7]	T1[6]	T1[5]	T1[4]

The decimal value of Dual Tone Frequency Setting bits (T0[11:0]) is the frequency of Tone0 on corresponding channel. The decimal value of T1[11:0] bits is the Tone1 frequency on corresponding channel.

6. Tone Enable and Tone Gain (07H/87H), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	0	1	1	1
I/O data	T1E	T0E	TG[5]	TG[4]	TG[3]	TG[2]	TG[1]	TG[0]

Tone Gain bits (TG[5:0]) are used to determine the gain of dual tone signal on corresponding channel.

$G = 20*\lg(Tg*2/256) + 3.14$

where: G is the calculated result of dual tone gain, and Tg is the decimal value of TG[5:0].
High Tone Enable and Low Tone Enable bits HE and LE are used to activate high tone or low tone on corresponding channels.

T1E = 0: Tone1 is disabled at the peak value in phase 90 degree (default);
T1E = 1: Tone1 is enabled at the crosszero;
T0E = 0: Tone0 is disabled at the peak value in phase 90 degree (default);
T0E = 1: Tone0 is enabled at the crosszero.

7. Transmit Time-slot and Transmit Highway Selection (08H/88H), <u>not available in GCI mode</u>, Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	0	0
I/O data	THS	TT[6]	TT[5]	TT[4]	TT[3]	TT[2]	TT[1]	TT[0]

Transmit Time-slot Bits (TT[6:0]) determine which time-slot will be used to transmit data for corresponding channel. The valid value is 0d - 127d corresponding to Time-slot0 to Time-slot127. The default value is 0d.
Transmit Highway Selection bit (THS) selects the PCM highway on corresponding channel to transmit voice data.

THS = 0: DX1 is selected (default);
THS = 1: DX2 is selected.

8. Receive Time-slot and Highway Selection (09H/89H), not available in GCI mode, Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	0	1
I/O data	RHS	RT[6]	RT[5]	RT[4]	RT[3]	RT[2]	RT[1]	RT[0]

Receive Time-slot Bits RT[6:0] determine which time-slot will be used to receive data for corresponding channel. The valid value is 0d - 127d corresponding to Time-slot0 to Time-slot127. The default value is 0d.
Receive Highway Selection bit RHS selects the PCM highway on corresponding channel to receive voice data.

RHS = 0: DR1 is selected (default);
RHS = 1: DR2 is selected.

9. Channel I/O Data (0AH/8AH), not available in GCI mode, Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	0	1	0
I/O data	R	O7	O6	O5	CD1	CD2	I/O3	I/O4

Channel I/O Data bits contain the information of SLIC I/O pins CD1, CD2, I/O3, I/O4, O5, O6 and O7 on corresponding channel. Default value is '0d'. It should be noted that both I/O3 and I/O4 are read only in this command.

10. Teletax Ramp Start, D/A Gain, A/D Gain and Channel Power Down (0CH/8CH), Read/Write

	b7	b6	b5	b4	b3	b2	b1	b0
Command	$\overline{R}$/W	0	0	0	1	1	0	0
I/O data	PD	GAD	GDA	RS	R	R	R	R

Teletax Ramp Start bit (RS) starts or stops the teletax on corresponding channel.

RS = 0: Teletax is stopped (default);
RS = 1: Teletax is started.

D/A Gain bit (GDA) sets the gain of analog D/A for corresponding channel.

GDA = 0: 0 dB (default);
GDA = 1: -6 dB.

A/D Gain bit (GAD) sets the gain of analog A/D for corresponding channel.

GAD = 0: 0 dB (default);
GAD = 1: +6 dB.

Channel Power Down bit (PD) disables or enables the corresponding channel.

PD = 0: the corresponding channel is in normal operation (default);
PD = 1: the corresponding channel is powered down.

Maximum Rating - Exceeding the following listed values may cause permanent damage, functional operation not implied.

Power Supply Voltage: ≤ 6.5 V
Voltage on Any Pin with Respect to Ground: -0.5 V to VDD + 0.5 V
Package Power Dissipation: ≤ 800 mW
Storage Temperature: -65 °C to +150 °C

Recommended Operating Conditions

Operating Temperature: -40 °C to +85 °C
Power Supply Voltage: 4.75 V to 5.25 V
MCLK: 1.536 MHz, 1.544 MHz, 2.048 MHz, 3.072 MHz, 3.088 MHz, 4.096 MHz, 6.144 MHz, 6.176 MHz or 8.192 MHz with tolerance of ± 50 ppm

Electrical Characteristics

Digital Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{IL}	Input Low Voltage			0.8	V	All digital inputs
V_{IH}	Input High Voltage	2.0			V	All digital inputs
V_{OL}	Output Low Voltage			0.8 0.2	V V	DX, I_L = 8 mA All other digital outputs, I_L = 4 mA. All digital pins, I_L = 1 mA.
V_{OH}	Output High Voltage	VDD - 0.6 VDD - 0.2			V V	DX, I_L = -8 mA All other digital outputs, I_L = -4 mA. All digital pins, I_L = -1 mA
I_I	Input Current	-10		10	µA	All digital inputs, GND<V_{IN}<V_{DD}
I_{OZ}	Output Current in High-impedance State	-10		10	µA	DX
C_I	Input Capacitance			5	pF	

Power Dissipation

Parameter	Description	Min	Typ	Max	Units	Test Conditions
I_{DD1}	Operating Current		50	80	mA	All channels are active.
I_{DD0}	Standby Current		4	6	mA	All channels are powered down, with MCLK present.

Note: Power measurements are made at MCLK = 4.096 MHz, outputs unloaded

Analog Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
V_{OUT1}	Output Voltage, VOUT	2.25	2.4	2.6	V	Alternating ±zero μ-law PCM code applied to DR
V_{OUT2}	Output Voltage Swing, VOUT	3.25			Vp-p	RL = 300 Ω
R_I	Input Resistance, VIN	160	270		kΩ	0.25 V < VIN < 4.75 V
R_O	Output Resistance VOUT			20	Ω	0 dBm0, 1020 Hz PCM code applied to DR.
R_L	Load Resistance, VOUT	300			Ω	External loading
I_I	Input Leakage Current, VIN	-1.0		1.0	μA	0.25 V < VIN < VDD - 0.25 V
I_Z	Output Leakage Current, VOUT	-10		10	μA	Power down
C_L	Load Capacitance, VOUT			100	pF	External loading

Transmission Characteristics

0 dBm0 is defined as 0.775 Vrms for A-law and 0.769 Vrms for μ-law, both for 600 Ω load. Unless otherwise noted, the analog input is a 0 dBm0, 1020 Hz sine wave; the input amplifier is set for unity gain. The digital input is a PCM bit stream equivalent to that obtained by passing a 0 dBm0, 1020 Hz sine wave through an ideal encoder. The output level is sin(x)/x-corrected.

Gain

Absolute Gain

Parameter	Description	Min	Typ	Max	Units	Test Conditions
G_{XA}	Transmit Gain, Absolute	-0.25		0.25	dB	Signal input of 0 dBm0, μ-law or A-law
G_{RA}	Receive Gain, Absolute	-0.25		0.25	dB	Measured relative to 0 dBm0, μ-law or A-law, PCM input of 0 dBm0 1020 Hz , RL = 10 kΩ

Gain Tracking

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GT_X	Transmit Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	
GT_R	Receive Gain Tracking					Tested by Sinusoidal Method, μ-law/A-law
	+3 dBm0 to - 40 dBm0	-0.10		0.10	dB	
	-40 dBm0 to -50 dBm0	-0.25		0.50	dB	
	-50 dBm0 to -55 dBm0	-0.50		0.50	dB	

Transmission Characteristics (continued)

Frequency Response

Parameter	Description	Min	Typ	Max	Units	Test Conditions
GXR	Transmit Gain, Relative to GXA					
	f = 50 Hz			-40	dB	
	f = 60 Hz			-40	dB	
	f = 300 Hz to 3400 Hz	-0.15		0.15	dB	
	f = 3600 Hz			-0.1	dB	
	f = 4600 Hz and above			-35	dB	
GRR	Receive Gain, Relative to GRA					
	f below 300 Hz			0	dB	
	f = 300 Hz to 3400 Hz	-0.15		0.15	dB	
	f = 3600 Hz			-0.2	dB	
	f = 4600 Hz and above			-35	dB	

Group Delay

Parameter	Description	Min	Typ	Max	Units	Test Conditions
DXR	Transmit Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			280	µs	
	f = 600 Hz –1000 Hz			150	µs	
	f = 1000 Hz – 2600 Hz			80	µs	
	f = 2600 Hz – 2800 Hz			280	µs	
DRR	Receive Delay, Relative to 1800 Hz					
	f = 500 Hz – 600 Hz			50	µs	
	f = 600 Hz –1000 Hz			80	µs	
	f = 1000 Hz – 2600 Hz			120	µs	
	f = 2600 Hz – 2800 Hz			150	µs	
DR	Round-trip Delay*			678	µs	

Note*: Round-trip Delay is the sum of the transmit and receive group delays (measured using same time slot)

Distortion

Parameter	Description	Min	Typ*	Max	Units	Test Conditions
STDX	Transmit Signal to Total Distortion Ratio					Noise method
	Input level = -3 dBm0 to -6 dBm0	30			dB	ITU-T O.131
	Input level = -6 dBm0 to -27 dBm0	36.5			dB	
	Input level = -27 dBm0 to -34 dBm0	33.5			dB	
	Input level = -34 dBm0 to -40 dBm0	29			dB	
	Input level = -40 dBm0 to -55 dBm0	14			dB	
STDR	Receive Signal to Total Distortion Ratio					Noise method
	Input level = -3 dBm0 to -6 dBm0	30			dB	ITU-T O.131
	Input level = -6 dBm0 to -27 dBm0	36			dB	
	Input level = -27 dBm0 to -34 dBm0	34			dB	
	Input level = -34 dBm0 to -40 dBm0	29.7			dB	
	Input level = -40 dBm0 to -55 dBm0	14			dB	
SFDX	Single Frequency Distortion, Transmit			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
SFDR	Single Frequency Distortion, Receive			-42	dBm0	200 Hz - 3400 Hz, 0 dBm0 input, output any other single frequency ≤ 3400 Hz
IMD	Intermodulation Distortion			-50	dBm0	Four Tone Method

Noise

Parameter	Description	Min	Typ	Max	Units	Test Conditions
NXC	Transmit Noise, C Message Weighted for μ-law			18	dBrnC0	
NXP	Transmit Noise, P Message Weighted for A-law			-68	dBm0p	
NRC	Receive Noise, C Message Weighted for μ-law			12	dBrnC0	
NRP	Receive Noise, P Message Weighted for A-law			-78	dBm0p	
NRS	Noise, Single Frequency f = 0 kHz – 100 kHz			-53	dBm0	VIN = 0 Vrms, tested at VFRO
PSRX	Power Supply Rejection Transmit					VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
PSRR	Power Supply Rejection Receive					PCM code is positive one LSB, VDD = 5.0 VDC + 100 mVrms
	f = 300 Hz – 3.4 kHz	40			dB	
	f = 3.4 kHz – 20 kHz	25			dB	
SOS	Spurious Out-of-Band Signals at VOUT Relative to Input PCM code applied:					0 dBm0, 300 Hz – 3400 Hz input
	4600 Hz – 20 kHz			-40	dB	
	20 kHz – 50 kHz			-30	dB	

Transmission Characteristics (continued)

Interchannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XTX-R	Transmit to Receive Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN of interfering channel. Idle PCM code into channel under test.
XTR-X	Receive to Transmit Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. VIN = 0 Vrms for channel under test.
XTX-X	Transmit to Transmit Crosstalk		-85	-78	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. VIN = 0 Vrms for channel under test.
XTR-R	Receive to Receive Crosstalk		-85	-80	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into interfering channel. Idle PCM code into channel under test.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling from VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

Intrachannel Crosstalk

Parameter	Description	Min	Typ	Max	Units	Test Conditions
XTX-R	Transmit to Receive Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 signal into VIN. Idle PCM code into DR.
XTR-X	Receive to Transmit Crosstalk		-80	-70	dB	300 Hz – 3400 Hz, 0 dBm0 PCM code into DR. VIN = 0 Vrms.

Note: Crosstalk into the transmit channels (VIN) can be significantly affected by parasitic capacitive coupling VOUT outputs. PCB layouts should be arranged to minimize these parasitics.

Timing Characteristics

Clock

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t1	CCLK period	244		100k	ns	
t2	CCLK pulse width	97			ns	
t3	CCLK Rise and Fall Time			25	ns	
t4	BCLK period	122			ns	
t5	BCLK pulse width	48			ns	
t6	BCLK Rise and Fall time			15	ns	
t7	MCLK pulse width	48			ns	
t8	MCLK Rise and Fall time			15	ns	
t9	DCL period F = 2.048 kHz F = 4.096 kHz		488 244		ns	
t10	DCL Rise and Fall Time			60	ns	
t11	DCL pulse width	90			ns	

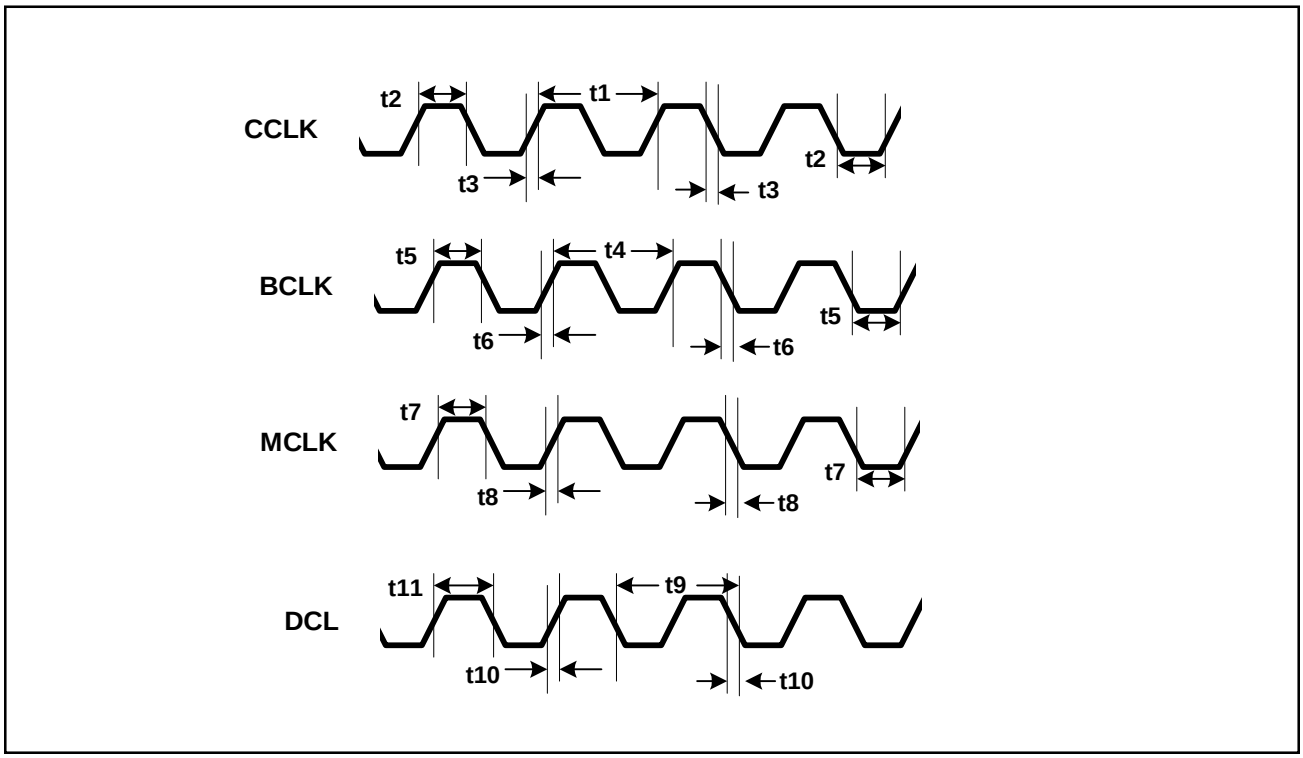


Figure 9. Clock Timing

Microprocessor Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t11	$\overline{CS}$ setup time	70		t3 - 10	ns	
t13	$\overline{CS}$ pulse width		8n*t1 (n>=2)		ns	
t14	$\overline{CS}$ off time	250			ns	
t15	Input data setup time	30			ns	
t16	Input data hold time	30			ns	
t17	SLIC output latch valid			1000	ns	
t21	Output data turn on delay			50	ns	
t22	Output data hold time	0			ns	
t23	Output data turn off delay			50	ns	
t24	Output data valid	0		50	ns	
t25	Reset pulse width	50			µs	

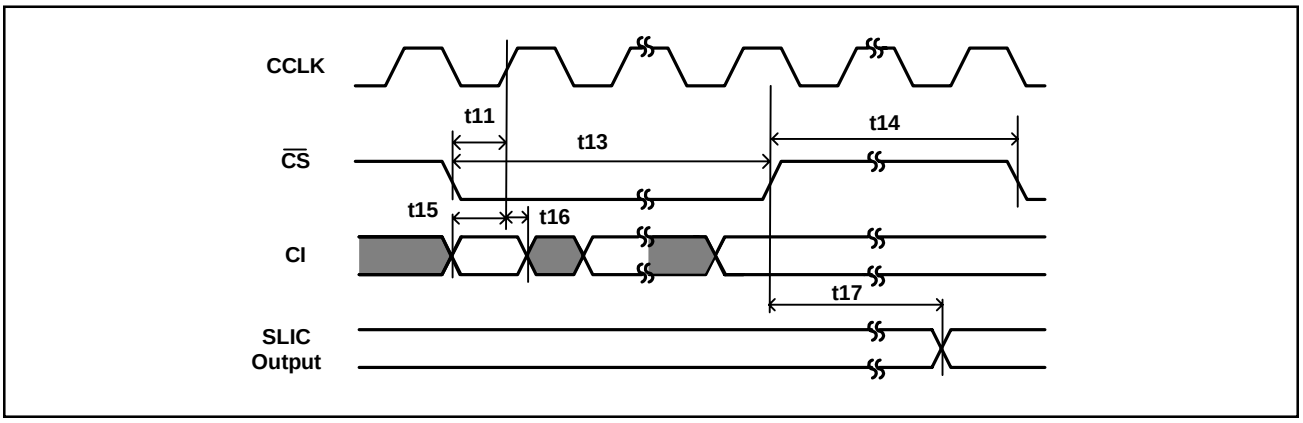


Figure 10. MPI Input Timing

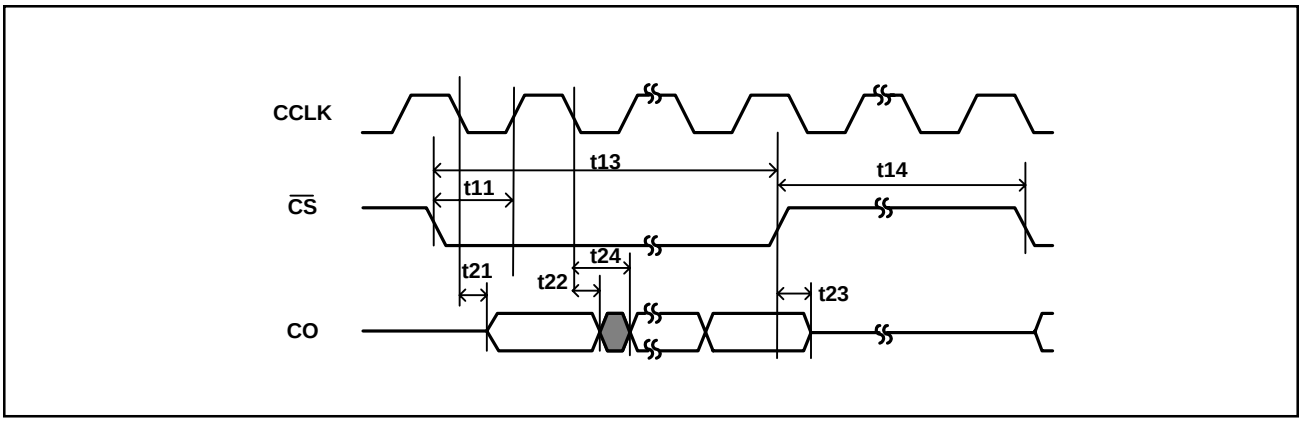


Figure 11. MPI Output Timing

Timing Characteristics (continued)

PCM Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t51	Data enable delay time	5		70	ns	
t52	Data delay time from BCLK	5		70	ns	
t53	Data float delay time	5		70	ns	
t54	Frame sync setup time	25		t4 - 50	ns	
t55	Frame sync hold time	50		t2 - 20	ns	
t56	$\overline{\text{TSX}}$ enable delay time	5		80	ns	
t57	$\overline{\text{TSX}}$ disable delay time	5		80	ns	
t61	Receive data setup time	25			ns	
t62	Receive data hold time	5			ns	

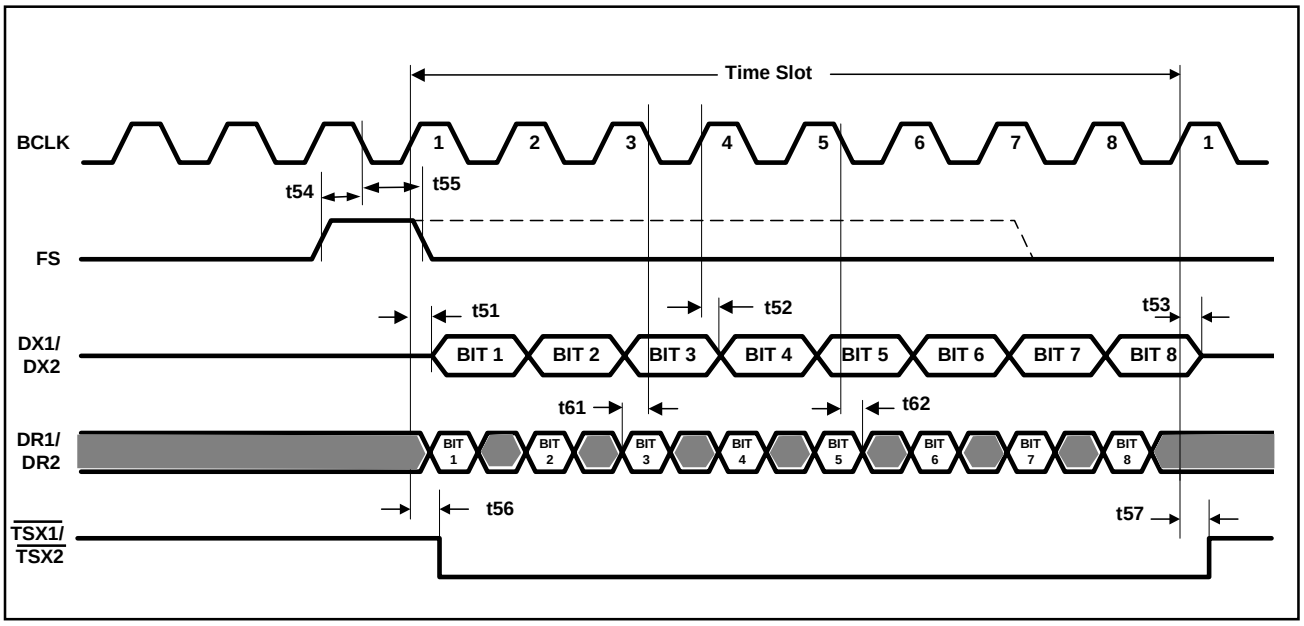


Figure 13. Transmit and Receive Timing When PCM Offset Delays One Clock*

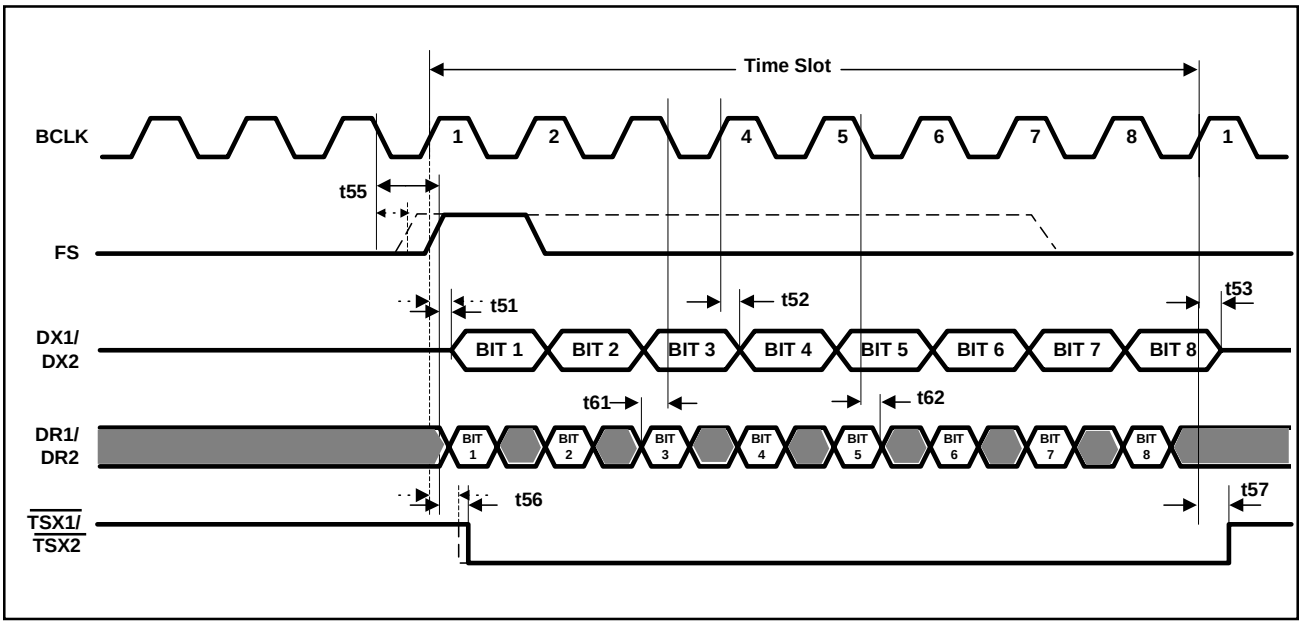


Figure 14. Transmit and Receive Timing *

Note*: These timing diagram only apply to the situation when data clock in on falling edges and clock out on rising edges.

Timing Characteristics (continued)

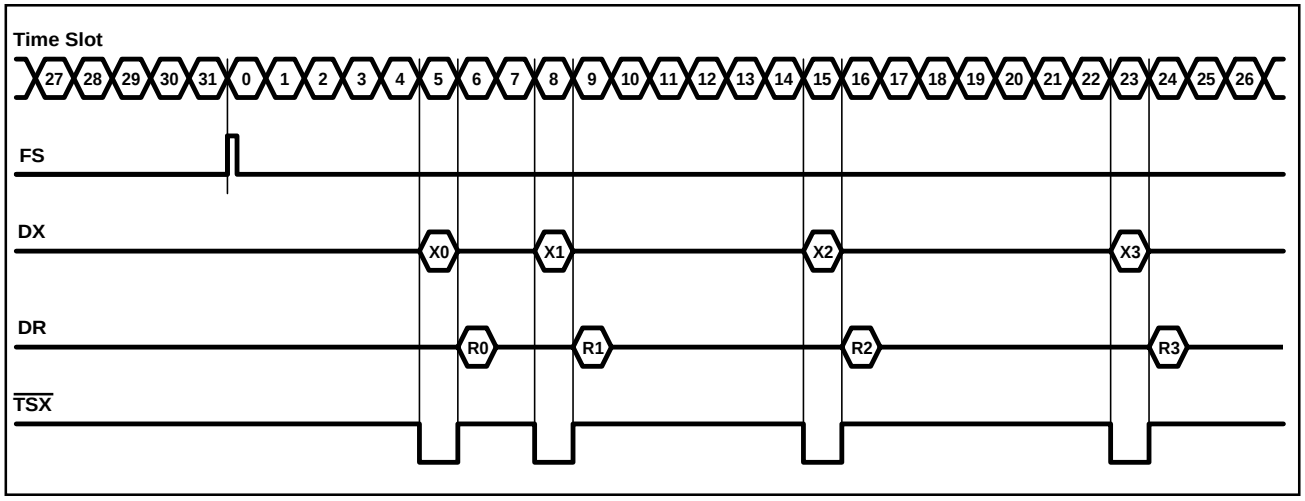


Figure 15. Typical Frame Sync Timing (2 MHz Operation)

GCI Interface

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t71	FSC rise and fall time			60	ns	
t72	FSC setup time	70		t9 - 50	ns	
t73	FSC hold time	50			ns	
t74	FSC high pulse width	130			ns	
t75	DU delay from DCL			100	ns	
t76	DU delay from FSC			150	ns	
t77	DD data setup	t11 + 20				
t78						

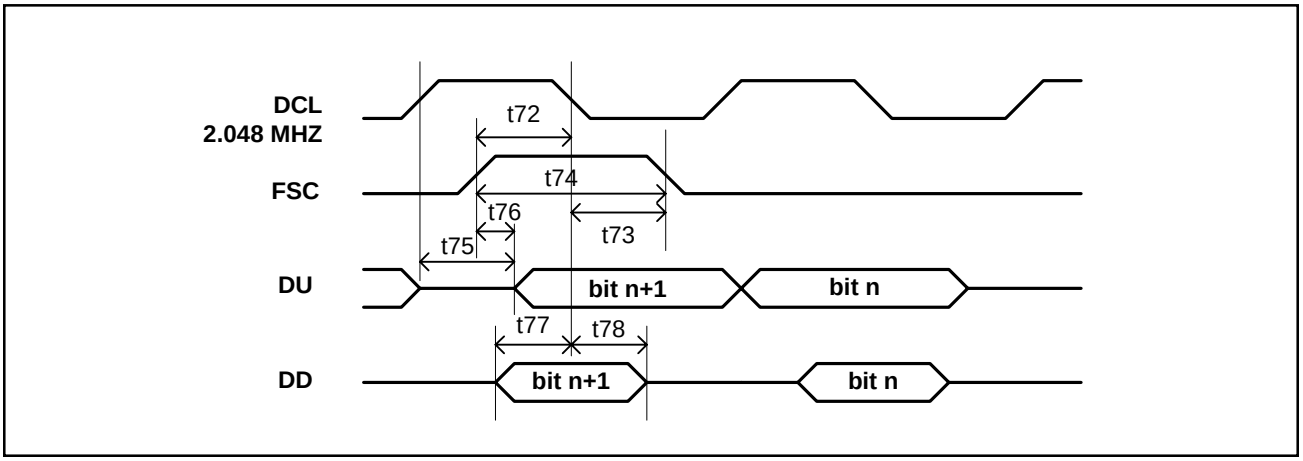


Figure 16. DCL Operation at 2.048 MHz

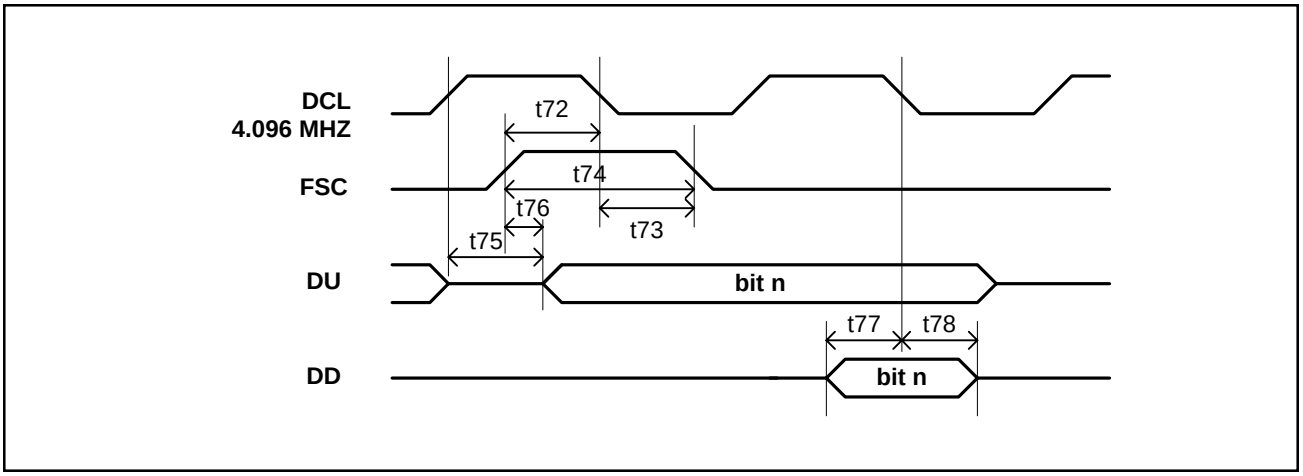
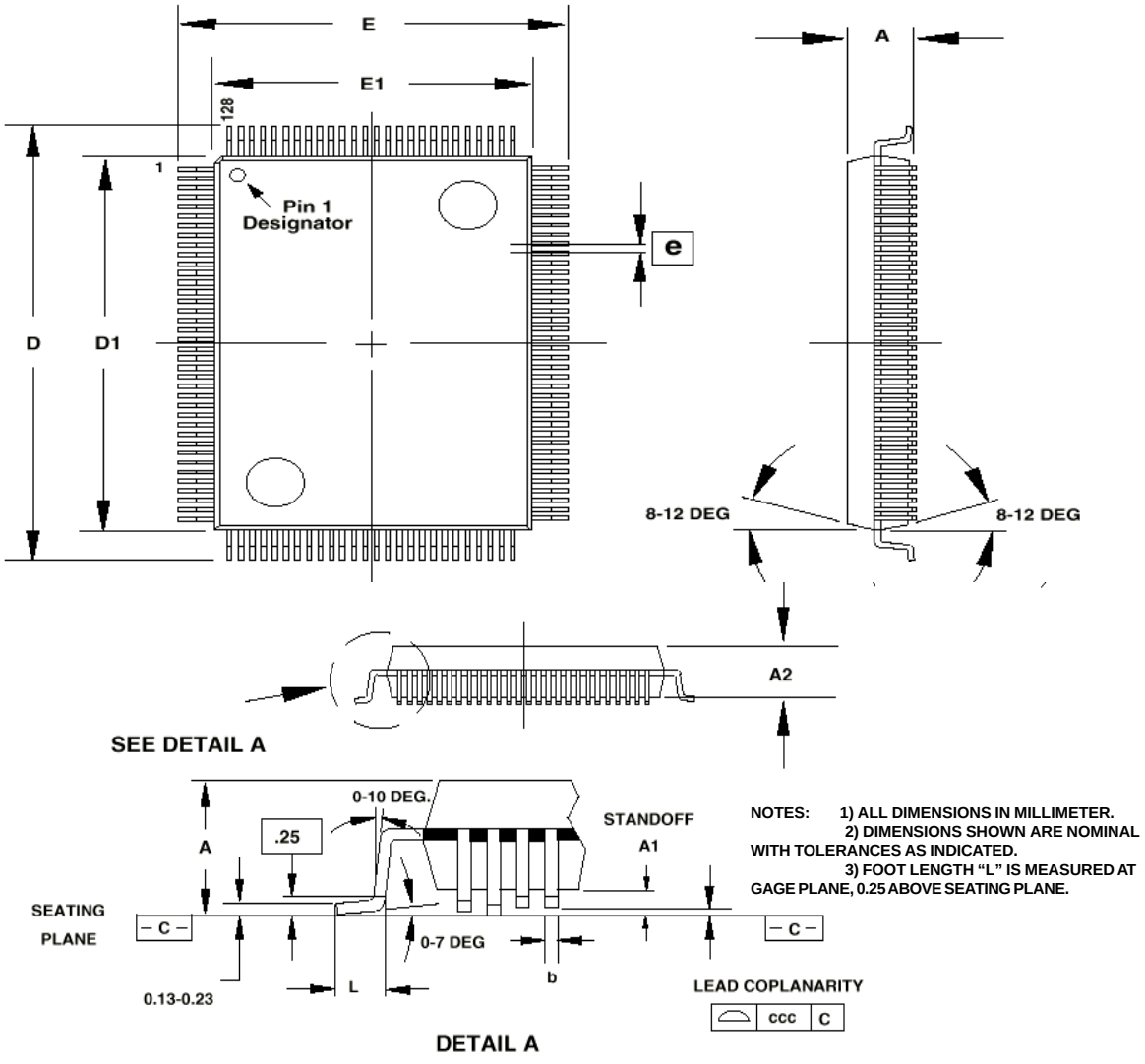


Figure 17. DCL Operation at 4.096 MHz

Physical Dimensions in Millimeters



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

Figure-18. NW1068-XQ 128 Pin PQFP Package Diagram

APPENDIX I: GCI Interface

GCI Interface Description for GCI Operation

GCI interface consists of two data lines (DU and DD) and two clock lines (FSC and DCL). It provides communication of both control and voice data between the GCI highway and SLIC. A complete GCI frame is sent upstream on DU pin and received downstream on DD pin every 125 µs.

Compressed GCI:

Each Compressed GCI frame consists of eight GCI timeslots. Each timeslot consists of four 8 bit bytes, they are:
- 2 Voice Channel bytes, which contain the voice data of channel A and B.
- A Monitor Channel byte, which is used for reading/writing control data/coefficients to the device for Channel A and B.
- A C/I byte, which contains a 6 bit width C/I channel sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bits are used for handshaking functions for Channel A and B. Both MX and MR are low active.

Figure 19 shows the overall Compressed GCI frame structure.

The upstream and downstream C/I channel bytes are continuously carrying I/O information every frame to and from the NW1068. In this way, the upstream processor can have an immediate access to SLIC output data present on NW1068's programmable I/O port on SLIC side through downstream C/I channel, as well as to SLIC input data through upstream C/I channel. The NW1068 transmits or receives data with the Most Significant Bit first. When I/O4 is selected as an input, its data can be read by Global Command 13 only.

Upstream C/I Octet

B7	B6	B5	B4	B3	B2	B1	B0
CD1(A)	CD2(A)	I3(A)	CD1(B)	CD2(B)	I3(B)	MR	MX

Downstream C/I Octet

B7	B6	B5	B4	B3	B2	B1	B0
$\overline{A}$/B	O7	O6	O5	O4	O3	MR	MX

where, $\overline{A}$/B selects channel A or Channel B:
$\overline{A}$/B = 0: Channel A is selected; $\overline{A}$/B = 1: Channel B is selected.

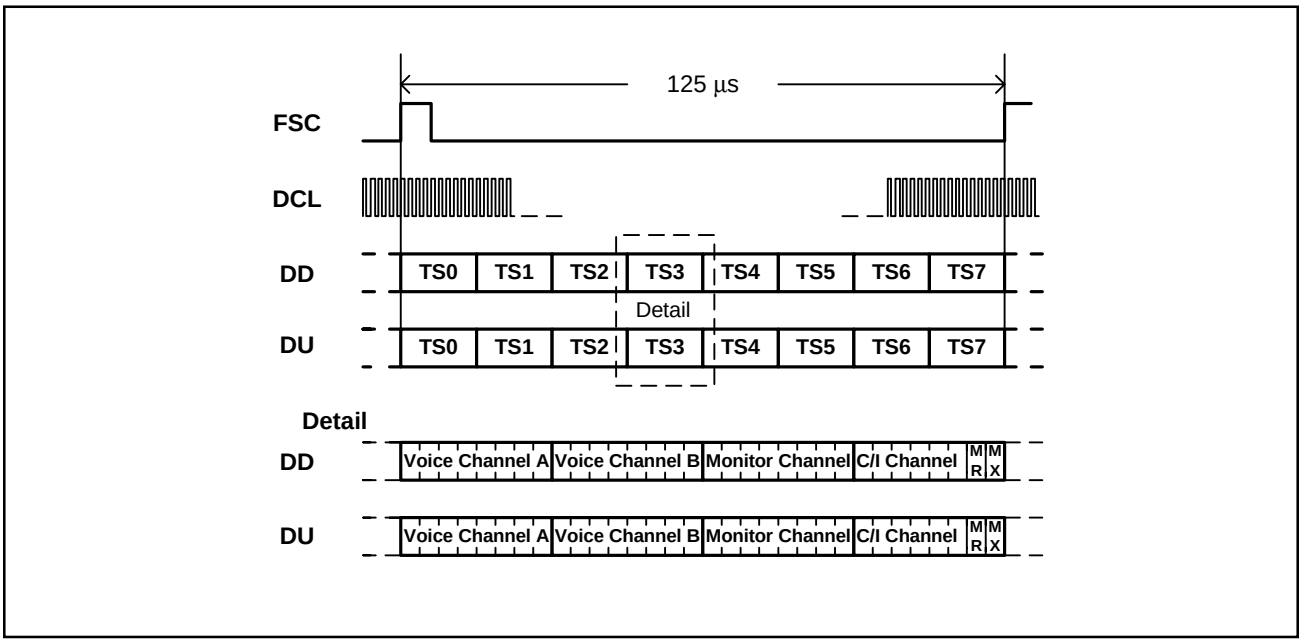


Figure 19. Compressed GCI Frame Structure

When the $\overline{CS}$ pin set the device into Compressed GCI operation, the eight channels of NW1068 are assigned to the Compressed GCI structure according to the status of TS pin as shown in the following table:

NW1068 Channels	TS = 0		TS = 1	
	Timeslot	Voice Channel	Timeslot	Voice Channel
1	Timeslot0	A	Timeslot4	A
2	Timeslot0	B	Timeslot4	B
3	Timeslot1	A	Timeslot5	A
4	Timeslot1	B	Timeslot5	B
5	Timeslot2	A	Timeslot6	A
6	Timeslot2	B	Timeslot6	B
7	Timeslot3	A	Timeslot7	A
8	Timeslot3	B	Timeslot7	B

Linear GCI:

Each Linear GCI frame consists of eight GCI timeslots. When TS pin is low, GCI Timeslot 0-3 are used as Monitor Channel and C/I octet, Timeslot 4-7 are used for linear voice data; when TS pin is high,GCI Timeslot 4-7 are used as Monitor Channel and C/I octet, Timeslot 0-3 are used for linear voice data.

Figure 20 gives an example of Linear GCI frame structure when TS is low.

In this case,Timeslots 0-3 are used as Monitor Channel and C/I octet. Each timeslot consists of four 8-bit bytes, they are:
- 2 don't_care bytes.
- A Monitor Channel byte, which is used for reading/writing control data/coefficients to the device for Channel A and B.
- A C/I byte, which contains a 6 bit width C/I channel sub-byte together with an MX bit and an MR bit. All real time signaling information is carried on the C/I channel sub-byte. The MX (Monitor Transmit) bit and MR (Monitor Receive) bits are used for handshaking functions for Channel A and B. Both MX and MR bits are low active.

Timeslots 4-7 are used for linear voice data (16-bit 2's complement). Each timeslot consists of two 16-bit linear voice data bytes: one byte contains the linear voice data for Channel A, the other byte contains the linear voice data for Channel B.

The upstream and downstream C/I channel bytes are continuously carrying I/O information every frame to and from the NW1068. In this way, the upstream processor can have an immediate access to SLIC output data present on NW1068's programmable I/O port on SLIC side through downstream C/I channel, as well as to SLIC input data through upstream C/I channel. The NW1068 transmits or receives data with the Most Significant Bit first. When I/O4 is selected as an input, its data can be read by Global Command 13 only.

Upstream C/I Octet

B7	B6	B5	B4	B3	B2	B1	B0
CD1(A)	CD2(A)	I3(A)	CD1(B)	CD2(B)	I3(B)	MR	MX

Downstream C/I Octet

B7	B6	B5	B4	B3	B2	B1	B0
$\overline{A}$/B	O7	O6	O5	O4	O3	MR	MX

where, $\overline{A}$/B selects channel $\overline{A}$ or Channel B:
$\overline{A}$/B = 0: Channel A is selected; $\overline{A}$/B = 1: Channel B is selected.

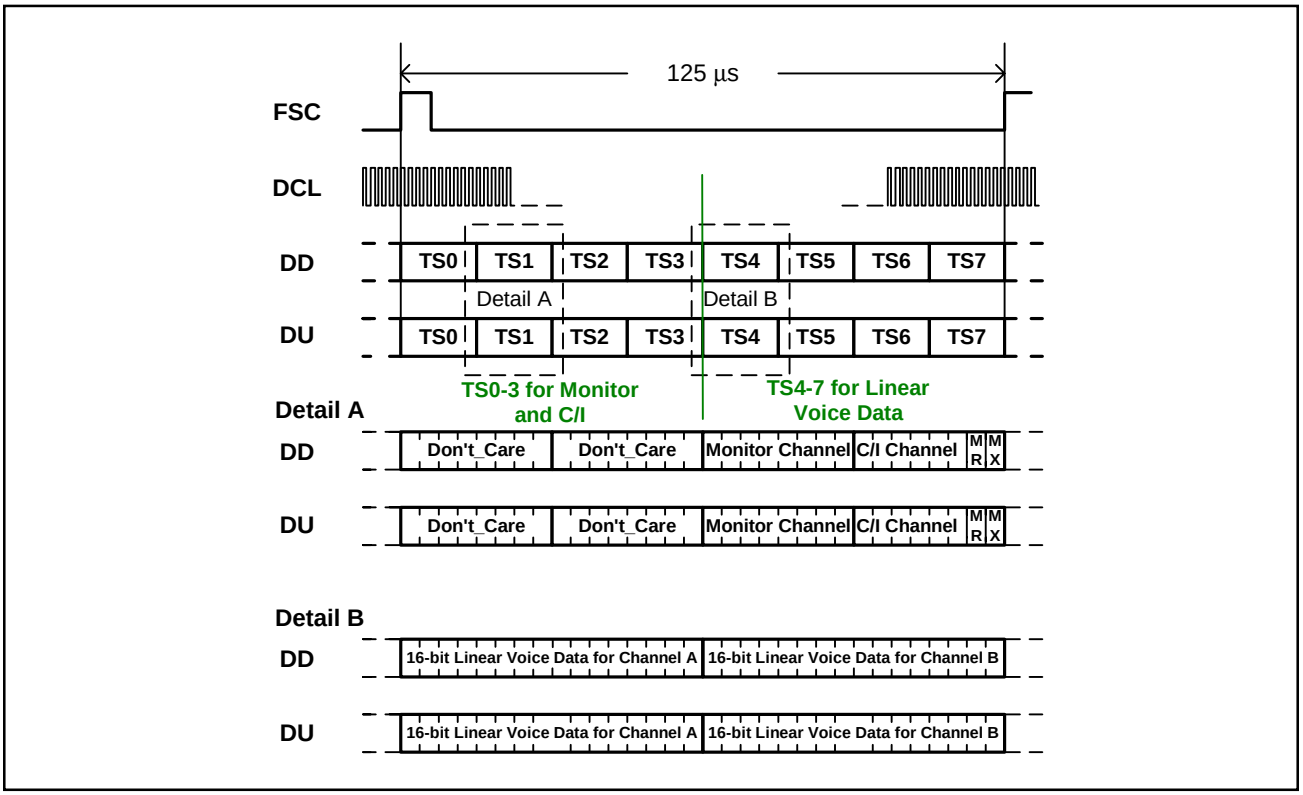


Figure 20. Linear GCI Frame Structure When TS Is Low

When the $\overline{CS}$ pin set the device into Linear GCI operation, the eight channels of NW1068 are assigned to the Compressed GCI structure according to the status of TS pin as shown in the following table:

NW1068 Channels	TS = 0			
	Timeslot	Monitor and C/I	Timeslot	Voice Channel
1	Timeslot0	A	Timeslot4	A
2	Timeslot0	B	Timeslot4	B
3	Timeslot1	A	Timeslot5	A
4	Timeslot1	B	Timeslot5	B
5	Timeslot2	A	Timeslot6	A
6	Timeslot2	B	Timeslot6	B
7	Timeslot3	A	Timeslot7	A
8	Timeslot3	B	Timeslot7	B
	TS = 1			
1	Timeslot4	A	Timeslot0	A
2	Timeslot4	B	Timeslot0	B
3	Timeslot5	A	Timeslot1	A
4	Timeslot5	B	Timeslot1	B
5	Timeslot6	A	Timeslot2	A
6	Timeslot6	B	Timeslot2	B
7	Timeslot7	A	Timeslot3	A
8	Timeslot7	B	Timeslot3	B

GCI Interface Structure

1. Monitor Channel Operation

The monitor channel is used for the transfer of maintenance information between two functional blocks. Using two monitor control bits (MR and MX) per direction, data is transferred in a complete handshake procedure. The MR and MX bits in the C/I Channel of the GCI frame are used for the handshake procedure of the monitor channel.

The monitor channel transmission operates on a pseudo-asynchronous basis:
- Data transfer (bits) on the bus is synchronized to FSC;
- Data flow (bytes) are asynchronously controlled by the handshake procedure.

For example: Data is placed onto the DD Monitor Channel by the Monitor Transmitter of the master device (DD MX bit is activated and set to '0'). This data transfer will be repeated within each frame (125 µs rate) until it is acknowledged by the NW1068 Monitor Receiver by setting the DU MR bit to '0', which is checked by the MX of the master device. Thus, the data rate is not 8-kbytes/sec.

2. Monitor Handshake

The monitor channel works in 3 states:
I. Idle state: A pair of inactive (set to '1') MR and MX bits during two or more consecutive frames: End of Message (EOM);
II. Sending state: MX bit is activated (set to '0') by the Monitor Transmitter, together with data-bytes (can be changed) on the monitor channel;
III. Acknowledging: MR bit is set to active (i.e. '0') by the Monitor Receiver, together with a data byte remaining in the monitor channel.

A start of transmission is initiated by a monitor transmitter by sending out an active MX bit together with the first byte of data (the address of the receiver) to be transmitted in the monitor channel.

This state remains until the addressed monitor receiver acknowledges the received data by sending out an active low MR bit, which means that the data transmission is repeated each 125 µs frame (minimum is one repetition). During this time the Monitor Transmitter keeps evaluating the MR bit.

Flow control, means in the form of transmission delay, can only take place when the transmitters MX and the receivers MR bit are in active state.

Since the receiver is able to receive the monitor data at least twice (in two consecutive frames), it is able to check for data errors. If two different bytes are received the receiver will wait for the receipt of two identical successive bytes (last look function).

A collision resolution mechanism (check if another device is trying to send data during the same time) is implemented in the transmitter. This is done by looking for the inactive ('1') phase of the MX bit and making a per bit collision check on the transmitted monitor data (check if transmitted '1's are on DU/DD line; DU/DD line are open drain lines).

Any abort leads to a reset of the NW1068 command stack, the device is ready to receive new commands.

To obtain a maximum speed data transfer, the transmitter anticipates the falling edge of the receivers acknowledgment.

Due to the inherent programming structure, duplex operation is not possible. It is not allowed to send any data to the NW1068, while transmission is active.

3. Monitor Channel Data Structure

The monitor channel is used for the transfer of maintenance information between two functional blocks.

Address Byte
Messages to and from the NW1068 are started with the following monitor byte:

B7	B6	B5	B4	B3	B2	B1	B0
1	0	0	0	0	0	0	1

Thus providing information for two voice channels, the NW1068 is one device on one GCI timslot. Monitor data for a specific voice channel is selcted by the NW1068 specific command.

Identification Command
In order to be able to identify differenct devices unambiguously by software, a two byte identification command is defined for analog lines GCI devices:

1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0

Each device will then respond with its specific identification code. For NW1068, this two byte identification code is:

1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	0

Each byte is transferred at least twice in two consecutive framse.

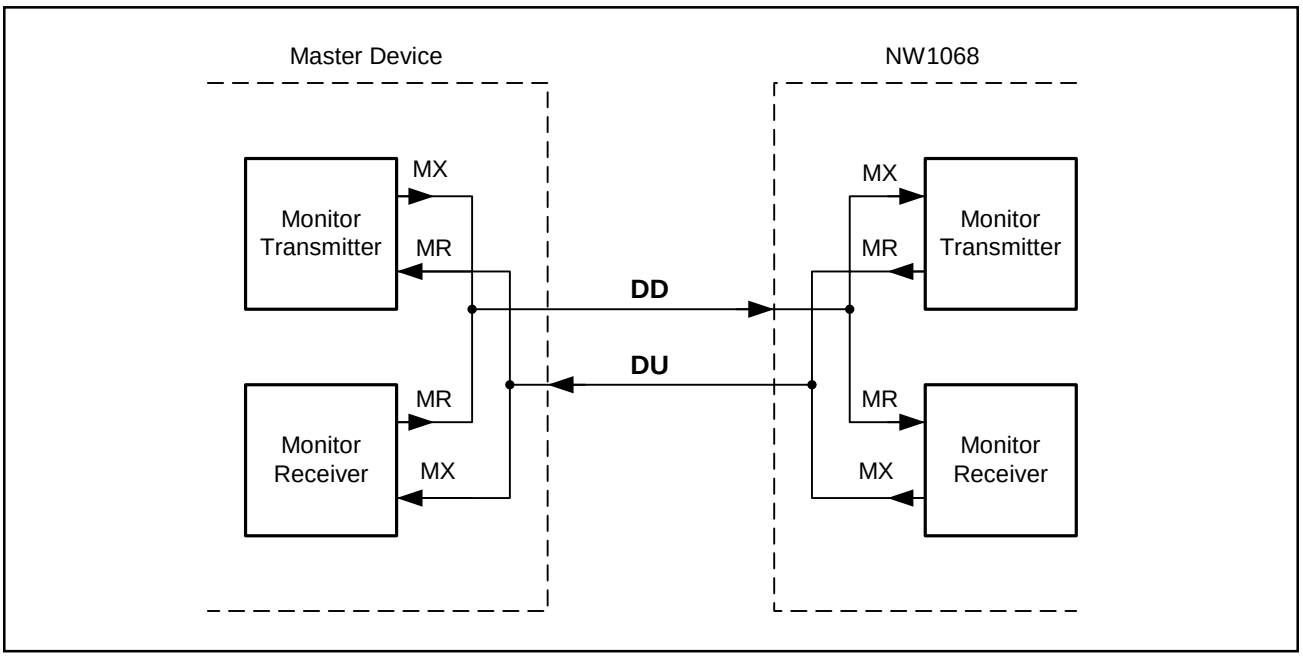


Figure 21. Monitor Channel Operation

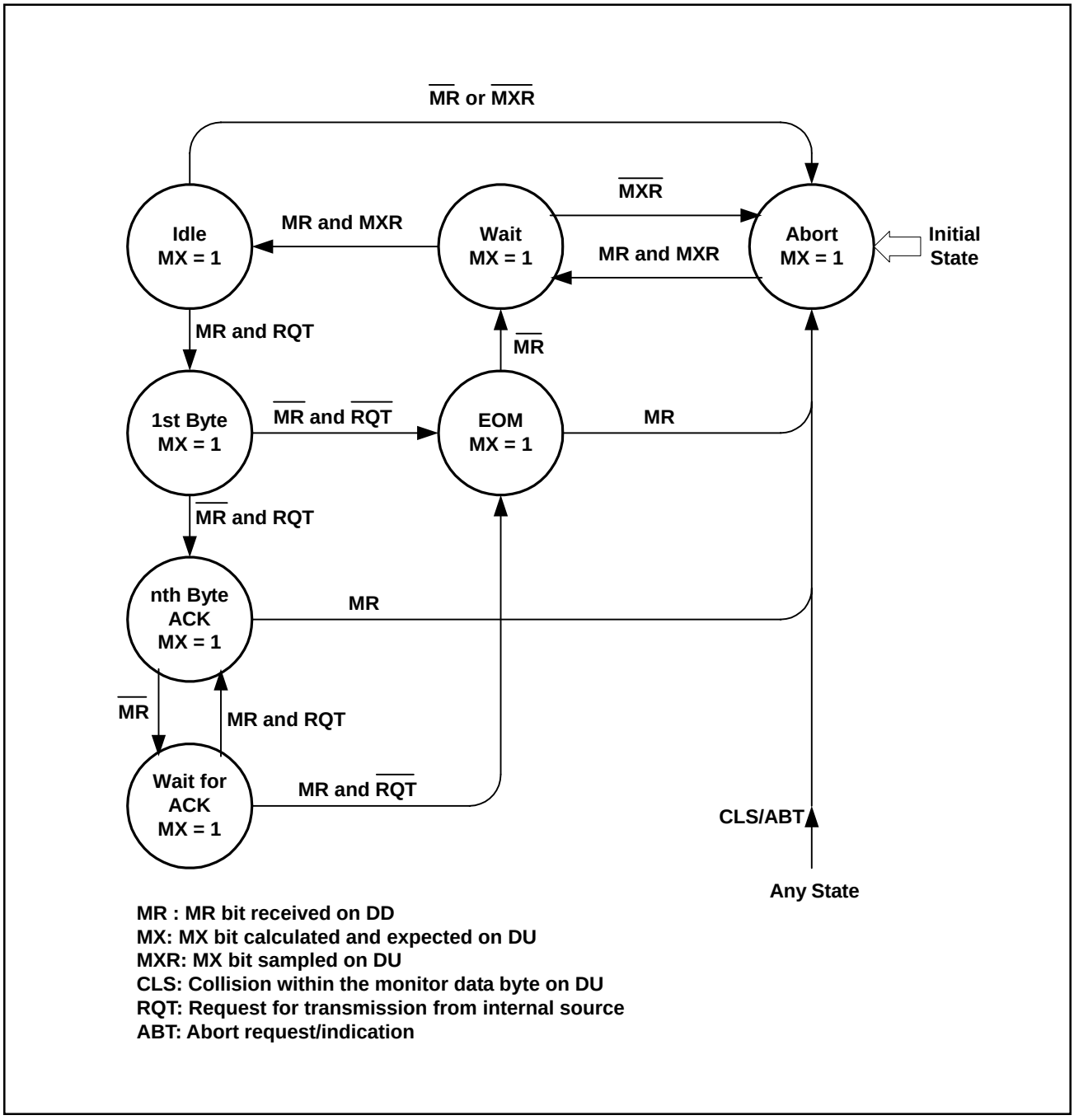


Figure 22. State Diagram of Monitor Transmitter

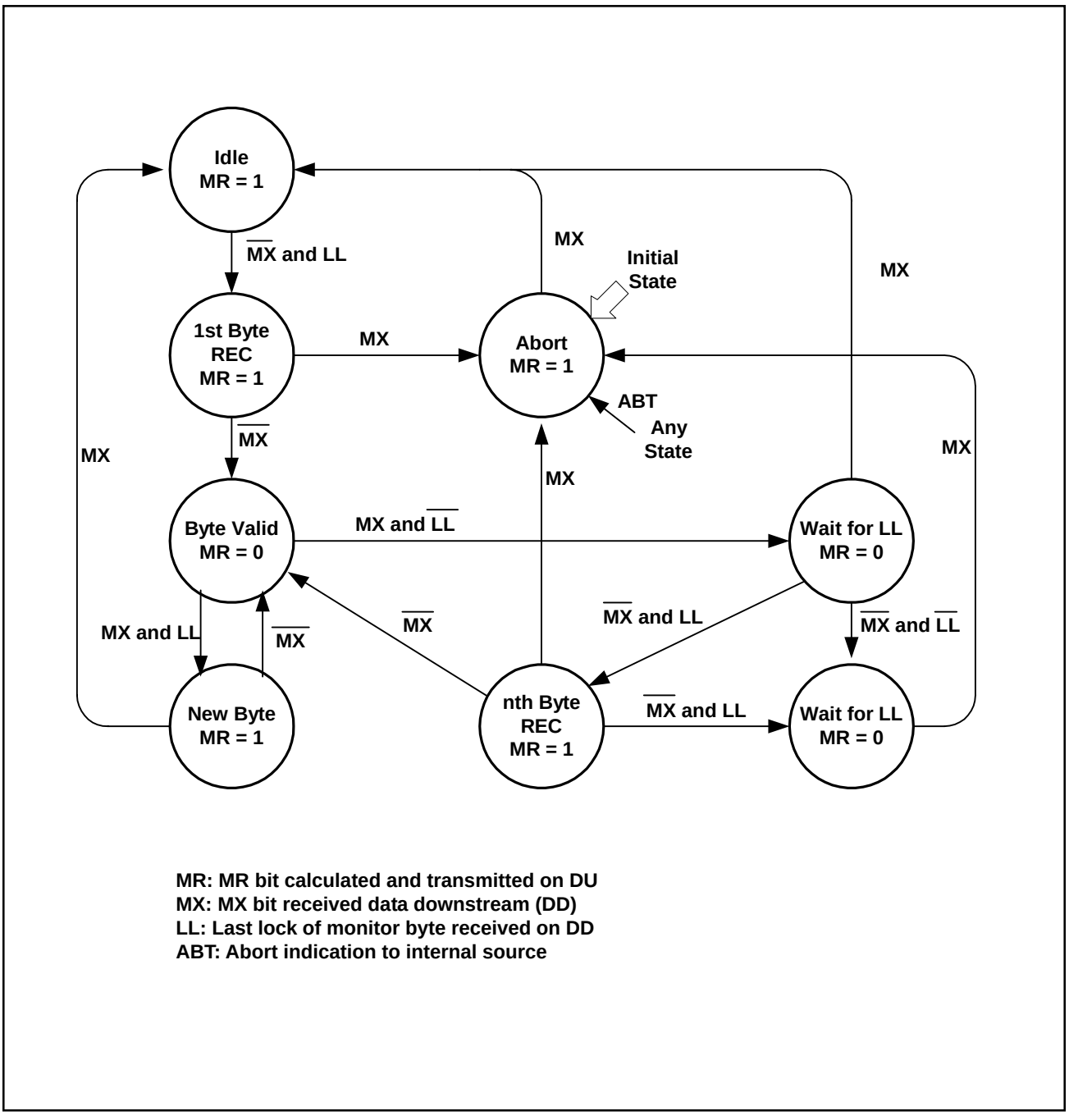


Figure 23. State Diagram of Monitor Receiver

APPENDIX III: Coe-RAM Mapping

Coefficent Memory Address Mapping Method