NEC

High Power N-Channel Silicon MOSFET For Broadcast / Transmitters

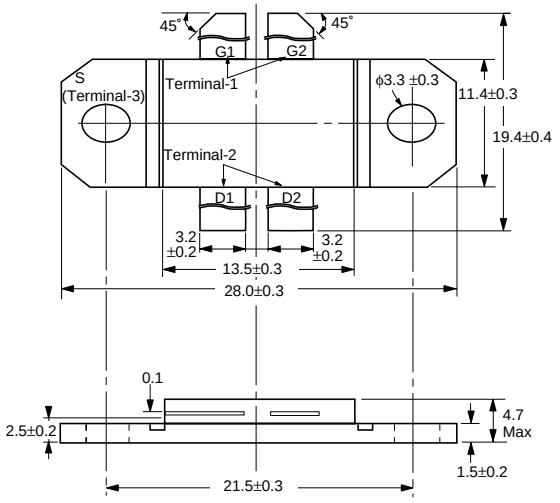
NEM0899F01-30

FEATURES

- **HIGH OUTPUT POWER:** 100 Watts
- **HIGH GAIN:** Linear Gain = 12 dB
- **LOW INTERMODULATION DISTORTION**
- **HIGH DYNAMIC RANGE**
- **HIGH EFFICIENCY:** η_D = 53%
- **INTERNALLY MATCHED FOR THE 470-860 MHz BAND**
- **PUSH-PULL STRUCTURE**

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE F01



DESCRIPTION

The NEM0899F01-30 is a high power enhancement mode Silicon MOSFET. Its design employs a vertical geometry for high drain to source breakdown voltage, a 1.3 mm x 28.8 mm gate, a gold metallization system, and a plasma silicon nitride layer on the surface of the transistor for long life and reliable operation. The NEM0899F01-30 uses two chips in a push-pull configuration and internal input and output pro-matching circuitry to provide broadband impedance transformation in the 470-860 MHz band.

ELECTRICAL PERFORMANCE CHARACTERISTICS (T_A = 25 °C)

PART NUMBER PACKAGE CODE		NEM0899F01-30 F01				
SYMBOLS	**PARAMETERS**	**UNITS**	**MIN**	**TYP**	**MAX**	**CONDITIONS**
P_{OUT}	Output Power	W	90	100	—	860 MHz; P_{IN} = 40 dBm
η_D	Drain Efficiency	%	48	50	—	I_{DQ} = 150 mA x 2
GL	Linear Gain	dB	10	12	—	V_{DD} = 30 V; P_{IN} = 30 dBm
I_{DSS}	Drain-Source Leakage Current	mA	—	—	2.0	V_{DS} = 60 V; V_{GS} = 0 V
V_{GS}(off)	Gate to Source Cutoff Voltage	V	1	—	4	V_{DS} = 5 V, I_D = 50 mA
I_{GSS}	Gate-Source Leakage Current	μA	—	—	1	V_{GS} = 7 V
R_{TH}	Thermal Resistance	°C/W	—	—	0.6	Channel to Case

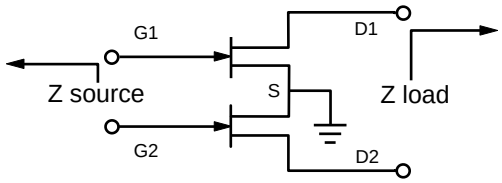
ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25 °C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DSS}	Drain to Source Voltage	V	60
V_{GSS}	Gate to Source Voltage	V	7
I_{DS}	Drain Current	A	15
P_D	Total Power Dissipation	W	290
T_{CH}	Channel Temperature	°C	200
T_{STG}	Storage Temperature	°C	-65 to +150

Note:
1. Operation in excess of any one of these parameters may result in permanent damage.

LARGE SIGNAL IMPEDANCES (Side to Side)

Frequency (MHz)	Z_{SOURCE} (Ω)	Z_{LOAD} (Ω)
470	1.5 + j0.6	7.3 - j6.0
650	2.2 - j2.3	8.0 + j0.8
750	2.5 - j3.6	4.3 - j4.8
860	3.8 - j6.6	3.5 - j5.5

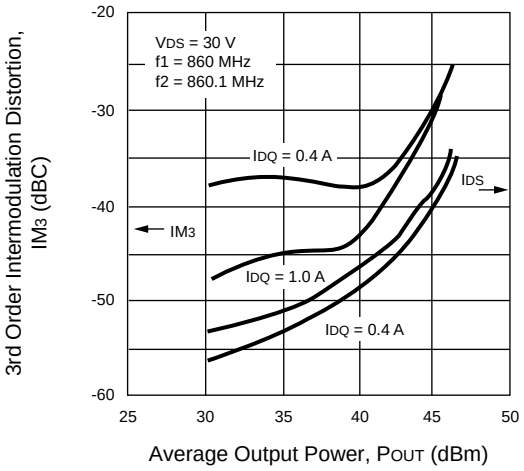


Z_{SOURCE} = Impedance of the external input matching circuit as seen from gate to gate.

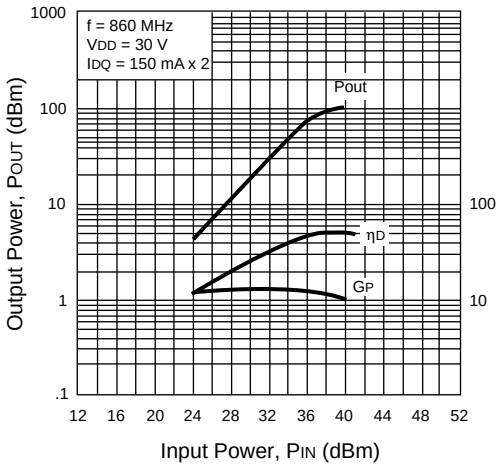
Z_{LOAD} = Impedance of the external output matching circuit as seen from drain to drain.

TYPICAL PERFORMANCE CURVES (T_A = 25°C)

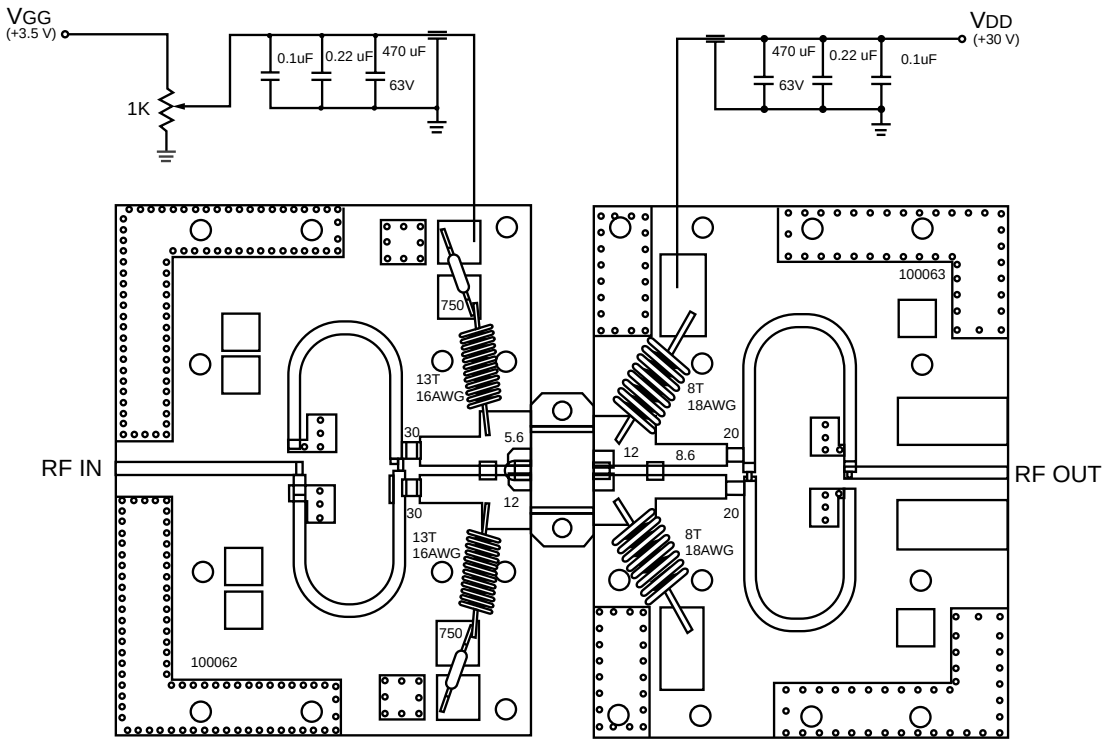
3rd Order INTERMODLATION DISTORTION AND DRAIN CURRENT vs. OUPUT POWER



OUTPUT POWER/DRAIN EFFICIENCY POWER GAIN vs. INPUT POWER



TEST CIRCUIT



Notes: 1. Circuit board: Er = 2.6, thickness = 0.8 mm (0.031").
2. Resistances are in ohms, capacitances are in picofarads unless otherwise noted.
3. Semi rigid coaxial cable: Er = 2.1, Zo = 250 ohms, external diameter = 2.3 mm (0.090"), total jacket length = 57 mm (2.25").