NEC

140 W S-BAND TWIN POWER GaAs MESFET | NES2427P-140

FEATURES

- **HIGH OUTPUT POWER:** 140 W TYP
- **HIGH LINEAR GAIN:** 9.5 dB TYP
- **HIGH EFFICIENCY:** 41% TYP
- **USABLE IN BALANCED OR PUSH-PULL CONFIGURATION.**

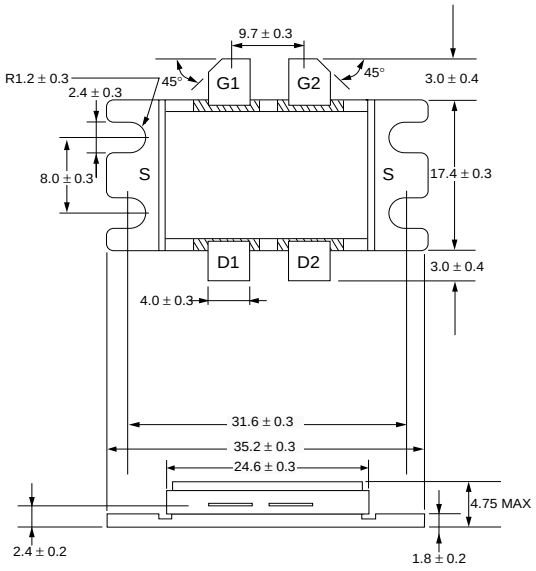
DESCRIPTION

The NES2427P-140 is a "twin" transistor device consisting of two pairs of GaAs MESFET chips which may be combined externally in either balanced or push-pull configurations. It is designed for mobile and fixed wireless (WLL) systems, and with modification of the external matching circuit, can be used for 2.1-2.6 GHz applications. It is capable of delivering 140 W of output power (CW) with high gain, high efficiency and excellent linearity. The device employs 0.9 µm Tungsten Silicide gates, via holes, plated heat sink, and silicon dioxide and nitride passivation for superior performance, thermal characteristics, and reliability.

Reliability and performance uniformity are assured by NEC's stringent quality control procedures.

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE T-92



G1, G2 : Gate
D1, D2 : Drain
S : Source

ELECTRICAL AND THERMAL CHARACTERISTICS (T_F = 40°C)

PART NUMBER / PACKAGE OUTLINE				NES2427P-140 T-92			
	SYMBOLS	CHARACTERISTICS	UNITS	MIN	TYP	MAX	TEST CONDITIONS
Functional Characteristics	P_{OUT}	Output Power	dBm	50.5	51.5		V_{DS} = 12 V f = 2.40 GHz I_{DSQ} = 6.0 A Total (RF off) P_{IN} = 44.5 dBm R_G[1] = 5.0 Ω (Each Side)
	G_L	Linear Gain	dB	8.5	9.5		
	η_{ADD}	Power-Added Efficiency	%		41		
	I_D	Drain Current	A		23		
Electrical DC Characteristics	I_{DSS}	Saturated Drain Current	A		76		V_{DS} = 2.5 V; V_{GS} = 0 V
	V_P	Pinch-off Voltage	V	-4.0	-2.6		V_{DS} = 2.5 V; I_{DS} = 330 mA
	R_{TH}[2]	Thermal Resistance Channel-to-Flange	K/W		0.4	0.55	T_F = 25°C; V_{DS} = 12 V; I_{DS} = 8.0 A

Notes:
1. R_G is the series resistance between the gate supply and the FET gate.
2. To calculate R_{TH} versus T_F and T_{CH} (or P_{DISS}), see AN1032 "Microwave Power GaAs Device Thermal Resistance Basics" application note. For the initial values use: R_{TH1} = 0.55 K/W, T_{F1} = 25°C, T_{CH1} = 77.8°C and for R_F use R_F = 0.18 K/W.

ABSOLUTE MAXIMUM RATINGS[1] (T_F = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DS}	Drain to Source Voltage	V	19
V_{GSO}	Gate to Source Voltage	V	-7
V_{GDO}	Gate to Drain Voltage	V	-22
I_D	Drain Current	A	76
I_G	Gate Current	mA	±440
P_T	Total Power Dissipation	W	237
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.

RECOMMENDED OPERATING LIMITS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{DS}	Drain to Source Voltage	V		12	12
G_{COMP}	Gain Compression	dB			3
T_{CH}	Channel Temperature	°C			150
I_{DSQ}	Quiescent Drain Current[1]	A		see	note[3]
P_{DISS}	Dissapated Power	W		see	note[3]
R_G	Gate Resistance[2]	Ω		5	12.5

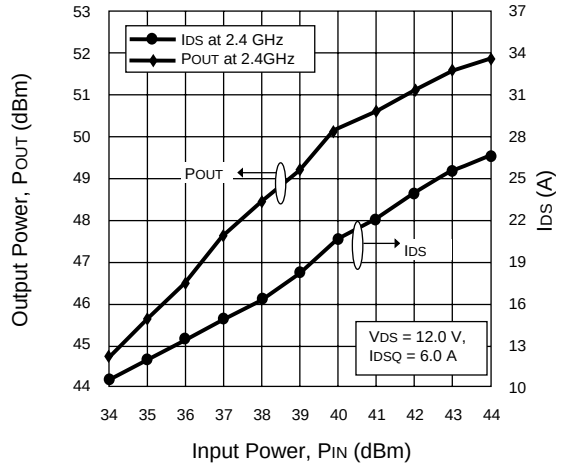
Notes:
1. V_{DS} = 12 V, RF OFF, I_{DSQ} = 3.0 A Each Drain.
2. R_G is the series resistance for each side between the gate supply and the FET gate.
3. See Maximum Power Dissipation vs. Flange Temperature Curve

ORDERING INFORMATION

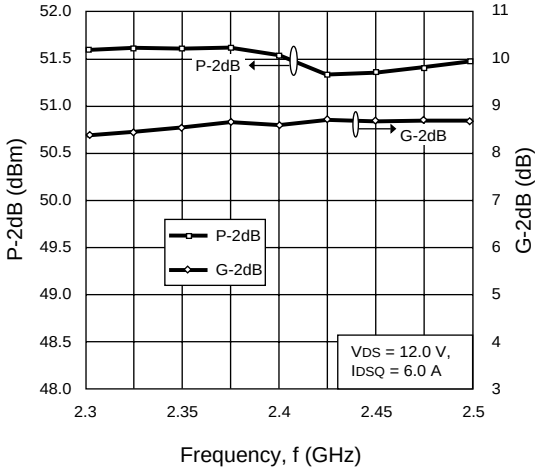
PART NUMBER	PACKAGE
NES2427P-140	T-92

TYPICAL PERFORMANCE CURVES (T_F = 40°C)

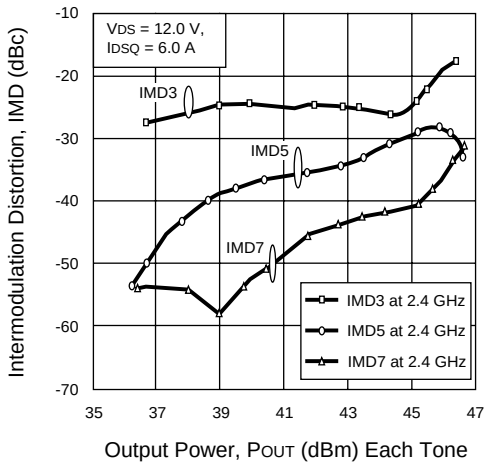
OUTPUT POWER AND I_{DS} vs. INPUT POWER



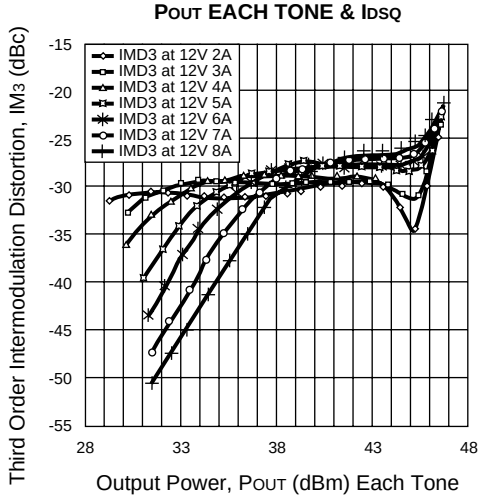
P-2dB AND G-2dB vs. FREQUENCY



INTERMODULATION DISTORTION vs. OUTPUT POWER

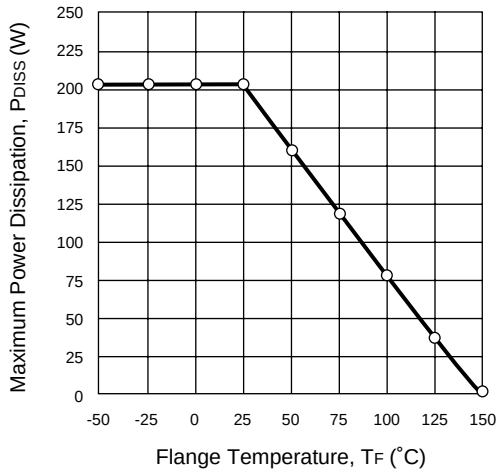


IMD3 vs. POUT EACH TONE & IDSQ



TYPICAL PERFORMANCE CURVES (T_F = 40°C)

MAXIMUM POWER DISSIPATION vs. FLANGE TEMPERATURE



TYPICAL SCATTERING PARAMETERS, (FOR EACH SIDE)

V_{DS} = 12 V, I_{DS} = 3.0 A, Z_O = 50 Ω, T_F = 25°C

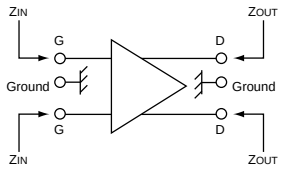
FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)
1.5	0.922	153.4	0.770	-29.0	0.005	-29.8	0.892	162.6
1.6	0.896	149.1	0.934	-41.6	0.006	-41.6	0.881	160.8
1.7	0.859	143.5	1.178	-56.7	0.007	-60.4	0.860	159.0
1.8	0.786	135.3	1.514	-73.3	0.008	-90.0	0.857	158.2
1.9	0.638	123.7	2.115	-96.0	0.011	-118.6	0.846	154.5
2.0	0.334	110.1	2.932	-128.5	0.017	-161.2	0.793	149.5
2.1	0.224	-147.0	3.416	-171.6	0.022	145.4	0.677	148.0
2.2	0.604	-158.5	3.036	148.5	0.023	97.8	0.608	154.2
2.3	0.766	-175.0	2.509	119.3	0.022	61.7	0.609	159.7
2.4	0.817	172.9	2.156	96.8	0.022	35.9	0.624	162.7
2.5	0.812	162.4	1.999	76.7	0.023	14.4	0.638	164.0
2.6	0.775	151.3	1.986	56.4	0.027	-7.1	0.650	165.4
2.7	0.641	138.5	2.023	32.9	0.032	-31.1	0.668	165.9
2.8	0.424	125.0	2.110	5.5	0.038	-58.6	0.700	166.5
2.9	0.132	141.9	2.052	-26.1	0.041	-90.2	0.751	164.0
3.0	0.278	-131.4	1.837	-58.0	0.040	-120.1	0.774	158.4
3.1	0.549	-141.4	1.491	-87.5	0.037	-146.9	0.752	152.8
3.2	0.707	-154.9	1.209	-111.8	0.032	-167.4	0.724	146.5
3.3	0.784	-166.3	1.014	-134.0	0.029	178.8	0.664	139.3
3.4	0.813	-176.6	0.891	-156.0	0.031	164.6	0.586	131.8
3.5	0.807	173.1	0.733	177.1	0.033	135.2	0.489	129.8

HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCES FOR P-2dB

(at V_{DS} = 12 V and I_{DS} = 3.0 A half of the device)

Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)	P-2dB (dBm)
2.08	35.7	-0.78	12.3	8.9	48.8
2.11	32.1	8.8	10.7	3.1	48.9
2.14	27.7	6.2	14.1	3.1	49.0
2.17	33.5	-5.8	11.4	2.1	49.0
2.20	26.0	1.6	12.4	0.4	48.9
2.25	11.8	-2.0	9.2	1.7	49.3
2.30	13.9	-1.3	8.6	4.1	49.2
2.35	10.3	-1.6	8.2	4.9	49.1
2.40	10.0	0.82	7.4	1.8	49.0

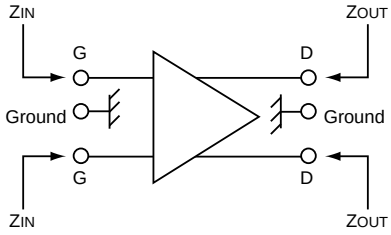
$Z_{IN} = R_{IN} + jX_{IN}$ (Conjugate of source impedance).
$Z_{OUT} = R_{OUT} + jX_{OUT}$ (Conjugate of load impedance).
Z_{IN} is the optimal gate-to-ground input impedance of half of the device.
Z_{OUT} is the optimal drain-to-ground output impedance of half of the device.
The input circuit is optimized for input return loss and tthe output circuit is optimized for P-2dB.



HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCES FOR CDMA SIGNAL

(at V_{DS} = 12 V and I_{DSQ} = 1.5 A half of the device)

Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)	ACPR at 5 MhHz (dBm)
2.08	35.7	-0.78	12.3	8.9	-31.1
2.11	32.1	8.8	10.7	3.1	---
2.14	27.7	6.2	14.1	3.1	-30.0
2.17	33.5	-5.8	11.4	2.1	-30.0
2.20	26.0	1.6	12.4	0.4	-30.5
2.25	17.1	9.9	8.3	3.1	-34.0
2.30	7.3	6.6	5.2	6.7	-34.1
2.35	7.4	5.5	5.2	5.3	-32.8
2.40	6.4	5.4	5.7	4.1	-32.5
2.45	8.2	4.9	10.4	6.5	-32.8



$Z_{IN} = R_{IN} + jX_{IN}$ (Conjugate of source impedance).
$Z_{OUT} = R_{OUT} + jX_{OUT}$ (Conjugate of load impedance).
Z_{IN} is the optimal gate-to-ground input impedance of half of the device.
Z_{OUT} is the optimal drain-to-ground output impedance of half of the device.
The input circuit is optimized for input return loss and the output circuit is optimized for ACPR of CDMA signal.
CDMA signal description:

CDMA SIGNAL	WALSH CODE	CHANNEL TYPE	POWERLEVEL (dB)
1	0	Pilot	-7.00
2	1	Paging	-12.96
3	8	Traffic	-15.96
4	9	Traffic	-15.96
5	10	Traffic	-15.96
6	11	Traffic	-15.96
7	12	Traffic	-15.96
8	13	Traffic	-15.96
9	14	Traffic	-15.96
10	15	Traffic	-15.96
11	16	Traffic	-15.96
12	32	Sync	-13.26

Chip Rate: 8.192 Mcps
Total average output power for half device is 39 dBm.