PRELIMINARY DATA SHEET

NEC

70 W S-BAND TWIN POWER GaAs MESFET

NES2427P-70

FEATURES

- **HIGH OUTPUT POWER:** 70 W TYP
- **HIGH POWER ADDED EFFICIENCY:** 40 % TYP
- **HIGH LINEAR GAIN:** 10 dB TYP at 2.7 GHz

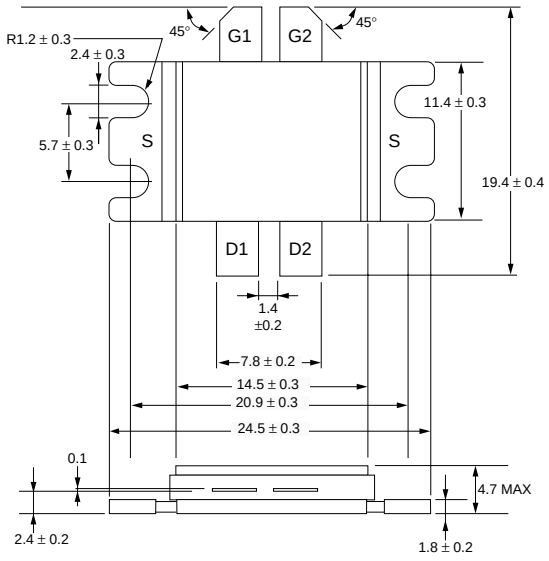
DESCRIPTION

The NES2427P-70 is a "twin" transistor device consisting of two GaAs MESFET chips which may be combined externally in either push-pull or balanced configuration. It is partially matched, and with external matching can operate within the 2.3-2.7 GHz band for WLL applications. It is capable of delivering 70 watts of output power (CW) with high gain, high efficiency and excellent linearity. The device employs 0.9 µm Tungsten Silicide gates, via holes, plated heat sink, silicon dioxide and nitrite passivation for superior performance, thermal characteristics, and reliability.

Reliability and performance uniformity are assured by NEC's stringent quality and control procedures.

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE T-86



G1, G2 : Gate
D1, D2 : Drain
S : Source

ELECTRICAL AND THERMAL CHARACTERISTICS (T_F = 25°C)

	PART NUMBER PACKAGE OUTLINE			NES2427P-70 T-86			
	SYMBOLS	**CHARACTERISTICS**	**UNITS**	**MIN**	**TYP**	**MAX**	**TEST CONDITIONS**
Functional Characteristics	P_{OUT}	Output Power	dBm	47.5	48.5		V_{DS} = 12 V f = 2.7 GHz I_{DSQ} = 5.0 A Total (RF off) P_{IN} = +41.5 dBm RG = 20 Ω[2]
	G_L[1]	Linear Gain	dB	9.0	10.0		
	η_{ADD}	Power-Added Efficiency	%		40		
	I_D	Drain Current	A		12.0		
	IM_3	Third Order Intermodulation Distortion	dBc		-34		P_{OUT} = 39 dBm (2 tone total) Δf = 5 MHz
Electrical DC Characteristics	I_{DSS}	Saturated Drain Current	A		38		V_{DS} = 2.5 V; V_{GS} = 0 V
	V_P	Pinch-off Voltage	V	-4.0	-2.6		V_{DS} = 2.5 V; I_{DS} = 165 mA
	R_{TH}[3]	Thermal Resistance, Channel to Flange	K/W		0.65	0.85	T_F = 25°C, V_{DS} = 12 V, I_{DS} = 8.0 A

Notes:
1. P_{IN} = +24 dBm for Linear Gain.
2. I_{DSQ} = 2.5 A Each Drain.
3. To calculate R_{TH} versus T_F and T_{CH} (or P_{DISS}), see AN1032 "Microwave Power GaAs Device Thermal Resistance Basics" application note. For the initial values use: R_{TH1} = 0.85 K/W, T_{F1} = 25°C, T_{CH1} = 106.6°C and for R_F use R_F = 0.24 K/W.

ABSOLUTE MAXIMUM RATINGS[1] (T_F = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DS}	Drain-to-Source Voltage	V	19
V_{GSO}	Gate-to-Source Voltage	V	-7
V_{GDO}	Gate-to-Drain Voltage	V	-22
I_D	Drain Current	A	38
I_G	Gate Current	mA	±250
P_T	Total Power Dissipation	W	160
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.

RECOMMENDED OPERATING LIMITS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{DS}	Drain to Source Voltage	V		12	12
G_{COMP}	Gain Compression	dB			3
T_{CH}	Channel Temperature	°C			150
I_{DSQ}	Quiescent Drain Current	A		see	note[1]
P_{DISS}	Dissapated Power	W		see	note[1]
R_G	Gate Resistance[2]	Ω			20

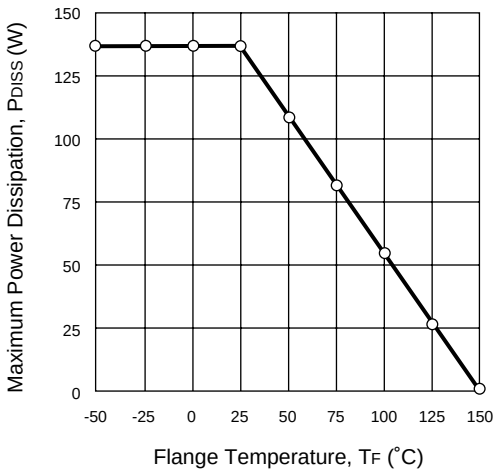
Notes:
1. See Maximum Power Dissipation vs. Flange Temperature Curve.
2. R_G is the series resistance for each side between the gate supply and the FET gate.

ORDERING INFORMATION

PART NUMBER	PACKAGE
NES2427P-70	T-86

TYPICAL PERFORMANCE CURVES (T_F = 25˚C)

MAXIMUM POWER DISSIPATION vs. FLANGE TEMPERATURE



TYPICAL SCATTERING PARAMETERS, (FOR EACH SIDE)

V_{DS} = 12 V, I_{DSQ} = 2.5 A, Z_O = 50 Ω, T_F = 25°C

FREQUENCY	S_{11}		S_{21}		S_{12}		S_{22}	
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)
1.5	0.957	154.0	0.657	36.2	0.009	27.4	0.892	168.2
1.6	0.949	151.3	0.682	31.1	0.010	24.9	0.888	167.3
1.7	0.938	148.3	0.718	25.3	0.011	21.4	0.885	166.0
1.8	0.923	144.9	0.765	18.9	0.012	16.5	0.880	164.8
1.9	0.903	141.3	0.833	11.4	0.013	10.4	0.873	163.6
2.0	0.874	137.4	0.920	2.7	0.014	3.2	0.868	162.5
2.1	0.828	133.0	1.033	-7.8	0.016	-7.1	0.862	161.4
2.2	0.763	128.9	1.166	-21.2	0.018	-21.1	0.857	160.1
2.3	0.674	126.5	1.298	-37.9	0.019	-40.2	0.852	158.9
2.4	0.585	128.7	1.360	-57.6	0.018	-64.7	0.849	158.4
2.5	0.553	136.7	1.335	-77.0	0.015	-91.0	0.876	157.6
2.6	0.608	142.8	1.275	-95.9	0.011	-114.5	0.919	154.1
2.7	0.697	141.6	1.147	-114.8	0.007	-157.0	0.914	148.1
2.8	0.769	136.0	1.025	-130.9	0.005	155.8	0.911	142.0
2.9	0.823	128.7	0.911	-146.4	0.005	86.9	0.890	134.4
3.0	0.859	119.9	0.794	-162.3	0.009	56.0	0.814	125.1
3.1	0.872	109.6	0.671	178.8	0.005	-68.6	0.621	108.3
3.2	0.879	99.8	0.567	167.8	0.050	125.2	0.510	121.0
3.3	0.928	84.9	0.516	153.1	0.069	29.2	0.670	104.5
3.4	0.962	64.5	0.390	128.2	0.110	-21.5	0.547	73.7
3.5	0.968	34.9	0.226	94.3	0.132	-55.7	0.353	22.9

HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCES FOR P-2dB

(at V_{DS} = 12 V and I_{DS} = 2.5 A half of the device)

Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)	P-2dB (dBm)	GSS (dB)	PAE at 2-dB (%)
2.25	3.7	14.4	2.4	7.4	45.6	11.0	49.7
2.30	4.1	15.4	2.4	7.8	45.6	11.3	49.7
2.35	5.1	16.4	2.5	8.2	45.5	11.2	47.9
2.40	5.8	16.7	2.5	8.6	45.5	11.5	48.6
2.45	8.4	19.4	2.6	9.0	45.6	10.8	43.1
2.50	8.2	17.1	2.6	9.4	45.6	10.6	45.1
2.55	9.8	18.6	2.7	9.7	45.7	10.7	43.3
2.60	10.3	17.0	2.7	10.1	45.2	10.6	41.7
2.65	11.6	15.6	2.8	10.5	45.0	10.8	36.2
2.70	12.1	13.5	2.8	10.9	45.2	10.7	40.1
2.75	13.0	12.4	2.9	11.3	45.1	10.5	39.9

$Z_{IN} = R_{IN} + jX_{IN}$ (Conjugate of source impedance).
$Z_{OUT} = R_{OUT} + jX_{OUT}$ (Conjugate of load impedance).
Z_{IN} is the optimal gate-to-ground input impedance of half of the device.
Z_{OUT} is the optimal drain-to-ground output impedance of half of the device.
The input circuit is optimized for input return loss and tthe output circuit is optimized for P-2dB.