PRELIMINARY DATA SHEET

NEC

45 W S-BAND TWIN POWER GaAs MESFET

NES2427P-45

FEATURES

- **HIGH OUTPUT POWER:** 45 W TYP
- **HIGH POWER ADDED EFFICIENCY:** 41 % TYP
- **HIGH LINEAR GAIN:** 11 dB TYP at 2.7 GHz

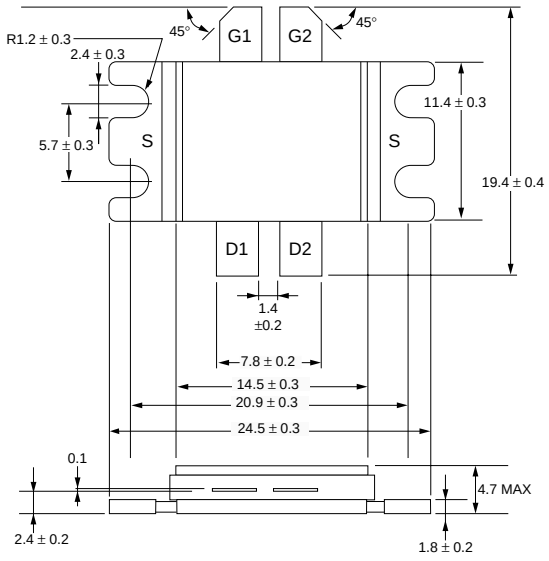
DESCRIPTION

The NES2427P-45 is a "twin" transistor device consisting of two GaAs MESFET chips which may be combined externally in either push-pull or balanced configuration. It is partially matched, and with external matching can operate within the 2.3-2.7 GHz band for WLL applications. It is capable of delivering 45 watts of output power (CW) with high gain, high efficiency and excellent linearity. The device employs 0.9 µm Tungsten Silicide gates, via holes, plated heat sink, silicon dioxide and nitrite passivation for superior performance, thermal characteristics, and reliability.

Reliability and performance uniformity are assured by NEC's stringent quality and control procedures.

OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE T-86



G1, G2 : Gate
D1, D2 : Drain
S : Source

ELECTRICAL AND THERMAL CHARACTERISTICS (T_F = 25°C)

PART NUMBER / PACKAGE OUTLINE				NES2427P-45 / T-86			
	SYMBOLS	CHARACTERISTICS	UNITS	MIN	TYP	MAX	TEST CONDITIONS
Functional Characteristics	P_{OUT}	Output Power	dBm	45.5	46.5		V_{DS} = 12 V f = 2.7 GHz I_{DSQ} = 4.0 A Total (RF off) P_{IN} = +38.5 dBm RG = 30 Ω[2]
	G_L[1]	Linear Gain	dB	10.0	11.0		
	η_{ADD}	Power-Added Efficiency	%		41		
	I_D	Drain Current	A		8		
	IM_3	Third Order Intermodulation Distortion	dBc		-38		P_{OUT} = 37 dBm (2 tone total) Δf = 5 MHz
Electrical DC Characteristics	I_{DSS}	Saturated Drain Current	A		24		V_{DS} = 2.5 V; V_{GS} = 0 V
	V_P	Pinch-off Voltage	V	-4.0	-2.6		V_{DS} = 2.5 V; I_{DS} = 110 mA
	R_{TH}[3]	Thermal Resistance, Channel to Flange	K/W		0.7	0.9	T_F = 25°C, V_{DS} = 12 V, I_{DS} = 8.0 A

Note:
1. P_{IN} = +22 dBm for Linear Gain.
2. I_{DSQ} = 2.0 A Each Drain.
3. To calculate R_{TH} versus T_F and T_{CH} (or P_{DISS}), see AN1032 "Microwave Power GaAs Device Thermal Resistance Basics" application note. For the initial values use: R_{TH1} = 0.9 K/W, T_{F1} = 25°C, T_{CH1} = 111.4°C and for R_F use R_F = 0.24 K/W.

ABSOLUTE MAXIMUM RATINGS[1] (T_F = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{DS}	Drain-to-Source Voltage	V	19
V_{GSO}	Gate-to-Source Voltage	V	-7
V_{GDO}	Gate-to-Drain Voltage	V	-22
I_D	Drain Current	A	24
I_G	Gate Current	mA	240
P_T	Total Power Dissipation	W	152
T_{CH}	Channel Temperature	°C	175
T_{STG}	Storage Temperature	°C	-65 to +175

Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.

RECOMMENDED OPERATING LIMITS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{DS}	Drain to Source Voltage	V		12	12
G_{COMP}	Gain Compression	dB			3
T_{CH}	Channel Temperature	°C			150
I_{DSQ}	Quiescent Drain Current[1]	A		see	note[1]
P_{DISS}	Dissapated Power	W		see	note[1]
R_G	Gate Resistance[2]	Ω			30

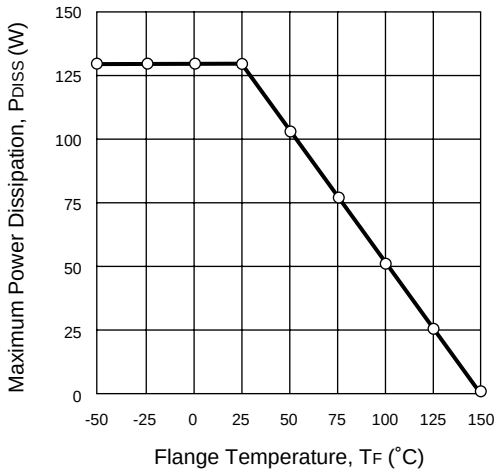
Notes:
1. See Maximum Power Dissipation vs. Flange Temperature Curve.
2. R_G is the series resistance for each side between the gate supply and the FET gate.

ORDERING INFORMATION

PART NUMBER	PACKAGE
NES2427P-45	T-86

TYPICAL PERFORMANCE CURVES (T_F = 25˚C)

MAXIMUM POWER DISSIPATION vs. FLANGE TEMPERATURE



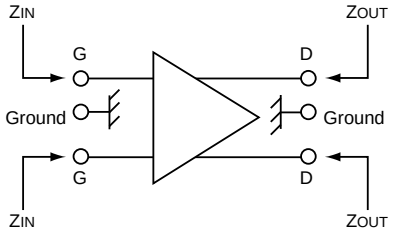
TYPICAL SCATTERING PARAMETERS, (FOR EACH SIDE)

V_{DS} = 12 V, I_{DSQ} = 2.0 A, Z_O = 50 Ω, T_F = 25°C

FREQUENCY	S11		S21		S12		S22	
(GHz)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)	MAG	ANG(°)
1.5	0.938	157.4	0.943	31.4	0.009	15.4	0.845	170.7
1.6	0.928	154.7	0.967	26.2	0.010	13.2	0.842	169.9
1.7	0.915	151.8	1.006	20.1	0.010	9.5	0.842	168.9
1.8	0.897	148.6	1.059	13.6	0.011	5.0	0.839	167.8
1.9	0.870	145.1	1.135	6.0	0.012	-1.0	0.837	167.0
2.0	0.835	141.4	1.232	-2.6	0.013	-8.9	0.837	165.9
2.1	0.783	137.3	1.355	-13.2	0.015	-18.8	0.839	164.9
2.2	0.709	133.6	1.492	-25.9	0.016	-32.0	0.840	163.7
2.3	0.614	131.8	1.623	-41.8	0.017	-50.5	0.845	162.3
2.4	0.518	135.6	1.682	-59.9	0.016	-74.1	0.846	160.6
2.5	0.478	146.6	1.627	-78.1	0.013	-102.1	0.859	159.6
2.6	0.534	155.9	1.572	-95.3	0.011	-128.5	0.900	155.7
2.7	0.629	156.3	1.431	-113.3	0.009	-161.1	0.892	149.8
2.8	0.708	152.1	1.285	-128.8	0.008	158.8	0.882	144.1
2.9	0.769	145.8	1.150	-143.8	0.009	120.1	0.858	137.1
3.0	0.808	138.1	1.016	-159.1	0.013	97.6	0.794	128.6
3.1	0.832	129.2	0.899	-176.9	0.015	80.2	0.690	113.2
3.2	0.853	119.4	0.715	166.7	0.025	48.8	0.481	102.9
3.3	0.885	105.3	0.648	162.8	0.042	14.8	0.585	115.5
3.4	0.914	85.6	0.580	139.7	0.059	-24.3	0.497	84.3
3.5	0.928	54.5	0.410	107.6	0.063	-66.0	0.315	22.8

HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCES FOR IMD

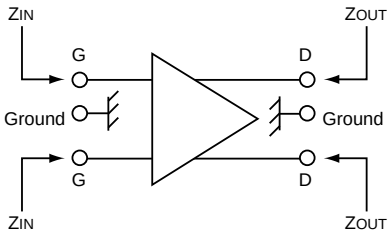
Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)	P_{OUT}/TONE (dBm)	GAIN (dB)	IMD_3 (dBc)	IMD_5 (dBc)	IMD_7 (dBc)
2.45	5.5	9.1	4.7	11.4	33.0	9.4	-42.8	-53.1	-69.8
2.50	5.6	8.1	4.3	10.5	33.0	10.9	-44.5	-57.9	-71.5
2.55	5.0	8.1	3.4	10.7	33.0	10.8	-41.6	-55.9	-70.0
2.60	3.6	5.6	4.9	10.3	33.0	10.4	-41.4	-54.5	-68.8
2.65	3.6	5.4	4.9	11.0	33.0	10.7	-44.7	-59.5	-71.6
2.70	3.9	5.0	4.9	11.0	33.0	11.2	-40.6	-56.5	-70.1
2.75	5.3	4.4	4.4	8.8	33.0	11.7	-40.1	-55.7	-69.4



V_{DS} = 12 V, I_{DS} = 3.0 A (half of the device)
$Z_{IN} = R_{IN} + jX_{IN}$ (Conjugate of source impedance).
$Z_{OUT} = R_{OUT} + jX_{OUT}$ (Conjugate of load impedance).
Z_{IN} is the optimal gate-to-ground input impedance of half of the device.
Z_{OUT} is the optimal drain-to-ground output impedance of half of the device.
The input circuit is optimized for input return loss and the output circuit is optimized for IMD at 33 dBm Output Power each tone.
IMD performance was measured at 33 dBm Output Power each tone.

HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCES FOR P-2dB

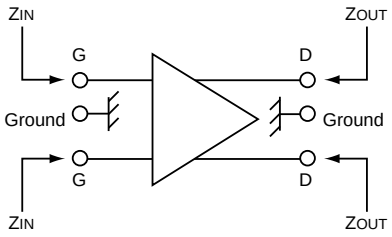
Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)	P-2dB (dBm)	GSS (dB)	PAE at P-2dB (%)
2.25	6.2	18.3	2.1	7.8	45.4	11.3	59.6
2.30	5.8	17.5	2.4	8.6	45.1	10.9	59.3
2.35	5.8	16.7	2.4	9.9	45.0	10.8	49.7
2.40	7.6	19.6	2.7	8.5	44.7	10.8	53.2
2.45	8.0	18.4	2.9	8.1	44.9	10.7	52.9



V_{DS} = 12 V, I_{DS} = 2.0 A (half of the device)
$Z_{IN} = R_{IN} + jX_{IN}$ (Conjugate of source impedance).
$Z_{OUT} = R_{OUT} + jX_{OUT}$ (Conjugate of load impedance).
Z_{IN} is the optimal gate-to-ground input impedance of half of the device.
Z_{OUT} is the optimal drain-to-ground output impedance of half of the device.
The input circuit is optimized for input return loss and the output circuit is optimized for P-2dB.

HALF (EACH SIDE) DEVICE OPTIMAL INPUT AND OUTPUT IMPEDANCES FOR CDMA SIGNAL

Frequency (GHz)	R_{IN} (Ohm)	X_{IN} (Ohm)	R_{OUT} (Ohm)	X_{OUT} (Ohm)	ACPR at 5 MhHz (dBm)
2.25	9.4	23.9	3.3	10.6	-34.1
2.30	8.7	21.8	3.1	9.5	-34.1
2.35	8.0	20.4	3.1	8.2	-35.2
2.40	7.5	19.7	3.1	9.5	-33.0
2.45	6.9	17.7	5.3	12.8	-32.6



V_{DS} = 12 V, I_{DS} = 500 mA (half of the device)
$Z_{IN} = R_{IN} + jX_{IN}$ (Conjugate of source impedance).
$Z_{OUT} = R_{OUT} + jX_{OUT}$ (Conjugate of load impedance).
Z_{IN} is the optimal gate-to-ground input impedance of half of the device.
Z_{OUT} is the optimal drain-to-ground output impedance of half of the device.
The input circuit is optimized for input return loss and the output circuit is optimized for 5 MHz ACPR with average output power is 34 dBm.
CDMA signal description:
12 Channels including pilot, paging, sync and 9 traffic channels. Chip rate is 8.912 MHz. The average output power for half device is 34 dBm.

CDMA SIGNAL	WALSH CODE	CHANNEL TYPE	POWERLEVEL (dB)
1	0	Pilot	-7.00
2	1	Paging	-12.96
3	8	Traffic	-15.96
4	9	Traffic	-15.96
5	10	Traffic	-15.96
6	11	Traffic	-15.96
7	12	Traffic	-15.96
8	13	Traffic	-15.96
9	14	Traffic	-15.96
10	15	Traffic	-15.96
11	16	Traffic	-15.96
12	32	Sync	-13.26

Chip Rate: 8.192 Total average output power for full device is 37 dBm.