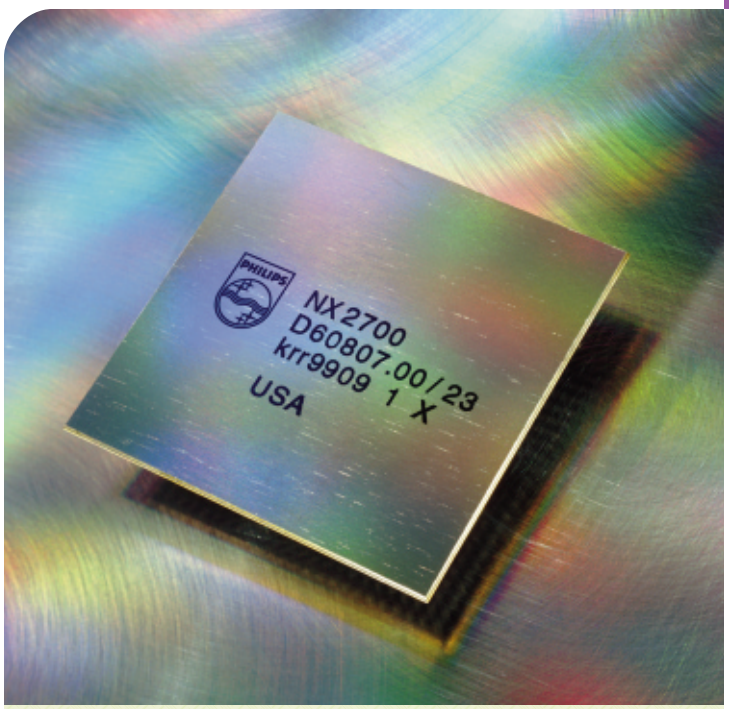
P R E L I M I N A R Y

Programmable Single-chip Media Processor for HDTV Products

Nexperia NX-2700



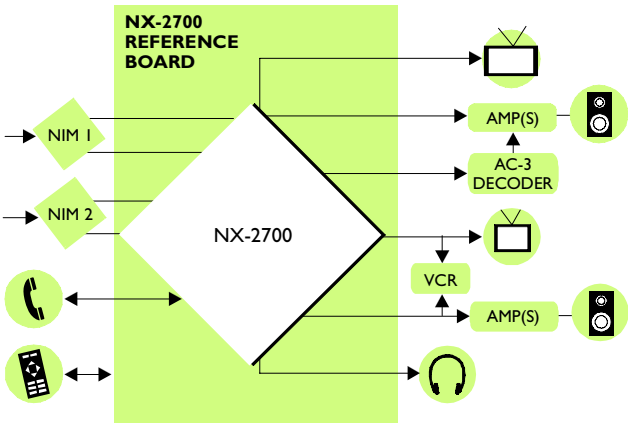
The first member of the Philips Nexperia™ Digital Video Platform family, the NX-2700 processor is a complete system-on-silicon supporting real-time source decoding, system control, and interactive services for high definition television (HDTV) receivers and set-top boxes. On a single chip, an NX-2700 can be programmed to process all video, audio, graphics, data, communications, and control datastreams required for next generation high-definition (HD) video appliances.

Whether the target is a digital TV set or set-top box, the flexible NX-2700 can be programmed in C/C++ to support DTV standards around the world. It accepts input from a variety of modular network interface modules (NIMs) and CCIR 656-compliant devices and outputs different YUV and RGB video formats to a variety of screen display technologies—from CRT to LCD, plasma, and projection.

A NX-2700 developers kit is also available to jump-start product creation. Together the kit's reference board, modular DTV software suite, and robust software development environment enable a wide variety of HD video appliances to be built.

FEATURES

- Powerful HDTV engine processes audio, video, graphics, communications, and data on a single chip
- C/C++ programmable TriMedia™ VLIW CPU
- On-chip I/O and coprocessing units designed for HDTV
  - two transport stream/CCIR-656 video input units
  - on-chip, slice-level MP@HL MPEG-2 accelerator handles one HD or up to four SD streams
  - powerful, HD video output unit prepares video for display and performs a variety of image manipulation and composition functions
  - SD video output unit enables simultaneous SD output
  - dual audio input units support auxillary audio sources
  - three audio output units support Dolby Digital®, stereo, and digital SPDIF
- High-performance internal 64-bit and 32-bit data buses
- Master/slave I^2C interface
- PCI/XIO interface supports PCI and 8-bit microprocessor bus interfaces
- Developers kit available



TM-2700 DTV DEVELOPERS KIT

Let's make things better.

PHILIPS

Building on powerful media processing capabilities of first generation TriMedia™ processors, NX-2700 incorporates features specifically designed to meet the real-time performance and cost demands of real-time consumer DTV products.

ARCHITECTED FOR HDTV

NX-2700 augments the powerful media processing capabilities and high-performance of its very-long instruction word (VLIW) TriMedia CPU with features specifically designed to meet the real-time performance and cost demands of consumer DTV products. Independent, on-chip units handle transport stream, video, and audio input and formatting from multiple independent sources. An on-chip MPEG-2 MP@HL accelerator handles real-time decoding of one HD (1080I) or up to four standard definition (SD) video streams. In addition to an SD video output (SDVO) unit, a second, programmable HD video output (HDVO) unit handles format conversions, generation of picture-in-picture (PIP) display, video generation for VCR recording, vertical and horizontal filtering, color space conversion, alpha blending, and many other video display processing tasks.

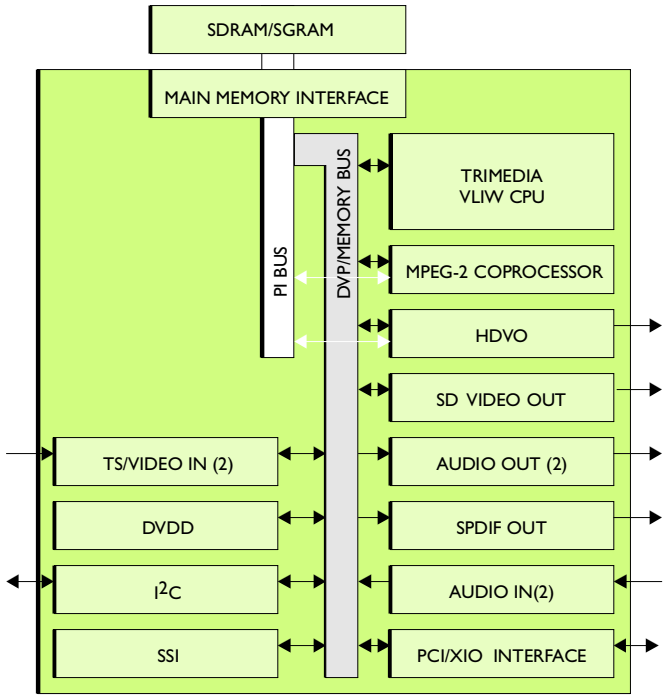
Real-time on-chip communications is ensured through a unique dual bus structure comprising separate, independently arbitrated data highways. NX-2700's V.34/V.90 modem interface provides remote communication support for interactive DTV receiver features requiring a reverse communications channel or Internet connection.

VLIW PROCESSOR CORE

At the heart of the NX-2700 is a powerful 32-bit, general-purpose TriMedia CPU. Through an elegant implementation of a fine-grain parallel VLIW architecture, the TriMedia CPU processes up to five simultaneous operations in a single clock cycle. These operations target any five of the 27 functional units in the CPU. Since the CPU's 128, fully general-purpose, 32-bit registers are not separated into banks, any operation can use any register for any operand.

Key to the TriMedia CPU's VLIW implementation, parallelism is optimized at compile time by a sophisticated compilation system. No specialized scheduling hardware is required to parallelize code during execution, thereby reducing cost and allowing the integration of multimedia-specific features that enhance CPU throughput during execution.

Enhanced instruction set includes special multimedia ops—In addition to traditional microprocessor operations and a full complement of 32-bit IEEE-compliant floating-point operations, the TriMedia instruction set includes special multimedia-specific operations (ops) that dramatically accelerate important multimedia functions such as video decompression. Just one special op (of the up to five operations issued in a single NX-2700 instruction) can implement up to 11 traditional microprocessor operations. Incorporated by the programmer into the C/C++ source code using familiar function-call syntax, special ops dramatically improve performance and enhance the efficiency of the CPU's parallel architecture.



NX-2700 PROCESSOR

The NX-2700's unique architecture and high-level programmability enable CE product developers to create HDTV products to serve many price points, form factors and markets—all from the same basic chip architecture.

Supports industry-standard RTOS kernels—In addition to implementing the non-trivial parts of multimedia algorithms, the NX-2700 CPU supports pSOS+® real-time operating system kernels. Developed by Integrated Systems Inc., pSOS+ kernels deliver the deterministic response and control features essential for consumer DTV products.

REAL-TIME VIDEO PROCESSING

To assist the CPU with input, decoding, and advanced display processing of video streams before output, NX-2700 tasks specialized on-chip I/O and coprocessing peripheral units.

Dual transport stream/video input units—Two independent, identical on-chip transport stream and video input (TS/VI) units enable simultaneous input and processing of two transport and/or digital video streams from different sources.

Each unit can receive a transport stream through a glueless connection to a variety of external sources such as an ATSC 8-VSB or satellite demodulator and decoder, Reed-Solomon decoder IC, channel decoder, or a NIM housing this functionality. After accepting and timestamping each MPEG-2 transport packet, the TS/VI optionally filters packets against a list of 64 PIDs then stores selected service packets in main memory. PID filtering reduces the CPU load and memory bandwidth usage. The unit also detects and optionally rejects erroneous packets. Transport stream demultiplexing and payload extraction appropriate to the HDTV application are performed by software on the TriMedia CPU.

Each TS/VI unit can also accept a digital, eight-bit, CCIR656/YUV 4:2:2 video stream from an off-chip device such as an NTSC NIM, a direct digital camera, or a digital video decoder. Non-CCIR-compliant devices such as an analog camera can be interfaced through a digital video decoder chip. The TS/VI units can also receive raw eight-bit data and unidirectional messages from other devices such as VBI decoders.

NX-2700's TS/VI units support both full and half-resolution data capture modes. Half resolution capture reduces luminance and chrominance data by a factor of two. Co-sited and interspersed chrominance resampling are supported.

MPEG-2 slice-level decoder—Decoding the highest resolution ATSC video formats requires approximately six times the computational power and memory bandwidth required to decode digital SD formats such as DVD or DVB. Under software control, the NX-2700 on-chip MPEG-2 slice-level accelerator performs real-time MPEG-2 decoding of any video format including all 18 ATSC-standard video formats up to the maximum resolution of main profile at high-level (MP@HL). MPEG-1 decoding is also supported.

Transmission errors can be quite frequent in terrestrial ATSC broadcasts, especially in areas having less than ideal reception. The MPEG-2 accelerator also plays a key role in masking transmission errors by implementing an error concealment scheme that reconstructs the damaged image and continues normal video decoding.

HDVO Key Functions

Before generating a digital video stream for display, the HDVO unit can perform powerful image manipulation and display management functions in response to programmed display device requirements and viewer requests. Key HDVO capabilities include:

Image Formatting/Scaling

- arbitrary vertical or horizontal scaling, shrinking, or zooming
- full vertical scaling
- 2X up- and down-sampling
- clipping
- color space conversion (RGB to YUV; YUV to RGB) with programmable coefficients
- RGB pixel format conversion

Filtering

- real-time, 6-tap horizontal filtering including panorama, supports both direct and transposed polyphase modes
- integrated deinterlacing filters (linear or median)
- programmable vertical filtering with up to 6 phases
- up to 165 Mpixels/sec

Blending video and graphics planes

- full 129-level alpha blending (8-bit alpha value) up to 150 Mpixels/sec
- color keying

Display

- outputs 8- or 10-bit RGB or YUV signals on 8/10, 16/20, or 24/30 pins interface
- supports output of other video formats such as YUV or YPrPb
- LUT-driven gamma correction ensures proper display brightness level
- throughput of 80 Mpixels/sec (240 MB/sec)

Synchronization

- video clock generation
- genlock mode (frame synchronization by an external signal)
- synchronization master or slave

High definition video output—The HDVO unit is a powerful, on-chip, programmable, video processor. In addition to preparing video output for high-definition display, HDVO performs a wide variety of image manipulation and composition functions including all image scaling and reformatting required to convert any of the 18 ATSC picture formats for output at the appropriate display resolution. HDVO can also act as a composition engine to mix video and graphics as required to support picture-in-picture (PIP), the electronic programming guide (EPG), other OSD graphics, and ancillary data such as control data, conditional access control data, and data associated with video services, such as closed captioning.

The HDVO unit comprises a microcontroller and video processing units (such as filters) connected to memory blocks through crossbar connections. Part of the memory can be used for line-buffer-based video processing. The microcontroller provides the programming flexibility for implementing various video processing functions. To simplify programming, an application programming interface is provided.

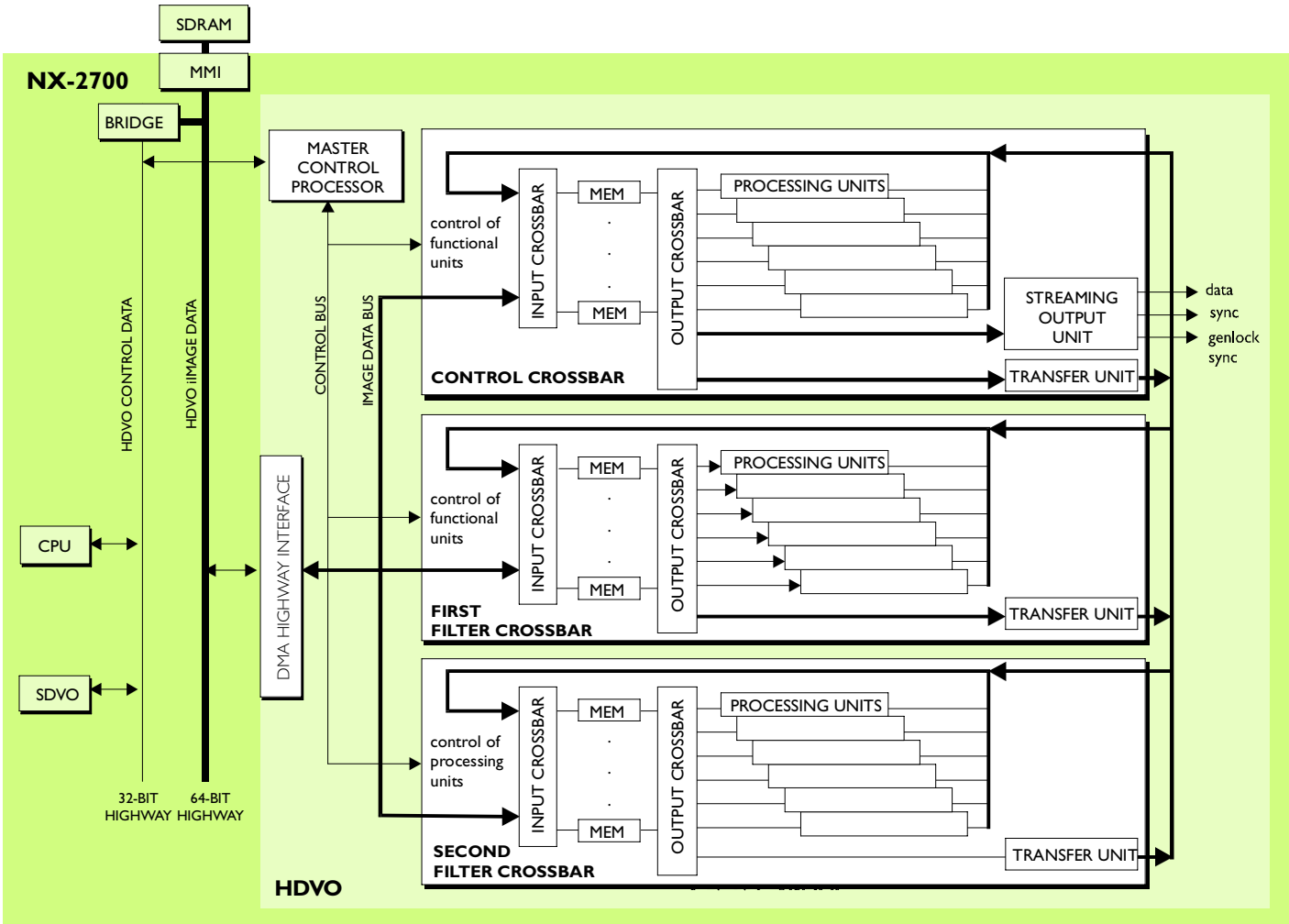
Standard definition video output—The SDVO unit outputs an SD signal of the main HD video program that is prepared by the HDVO unit. In HD product designs this signal is primarily used for display on a separate PAL/NTSC monitor or recording to a VCR or similar device. Format conversion, graphics overlay, alpha blending and other display manipulations are performed for the SDVO unit by the HDVO unit.

AUDIO INPUT & OUTPUT

The audio stream accompanying a DTV broadcast transmission is part of the transport stream input through the TS/VI unit. The NX-2700's two audio input (AI) units handle audio originating from alternate sources. After software processing, digital audio is output through one of the NX-2700's three audio output units.

Dual, independent audio input units—NX-2700 incorporates two identical AI units to capture audio bitstreams from non-transport stream sources, such as the audio program from an NTSC/PAL VCR, DVD player, etc. These units connect gluelessly to most serial ADC chips and can receive stereo audio or SPDIF data through external glue logic.

Audio decoding & processing—Decoding digital audio formats is performed by NX-2700 in software appropriate to the HDTV product features. Software modules for decoding Dolby Digital (AC-3)® streams and for audio mixing and rendering of stereo PCM audio data are included in the NX-2700 DTV Developers Kit.



A powerful programmable on-chip video processor, the HDVO unit utilizes a series of filters, video processing units, and local memory blocks to provide scaling, filtering, color space conversion and many other powerful display formatting features before output of the final video frames.

Dual independent audio output units—Two independent audio-out (AO) units provide all signals needed to gluelessly interface to high-quality, low-cost oversampling digital to analog converters (DACs). The primary AO unit can output up to eight channels of PCM audio data, including decoded six-channel Dolby Digital, four-channel Dolby Pro Logic®, and stereo audio. The secondary AO unit outputs PCM stereo audio. Both audio-out units support a maximum 32-bits per channel sample size.

All audio I/O units utilize a programmable oversampling D/A system clock and can be programmed to handle most reasonable audio protocols. Sampling clocks support a wide range of sample sizes giving programmers subtle control over sampling frequency and enabling audio and video synchronization to be achieved in any system configuration.

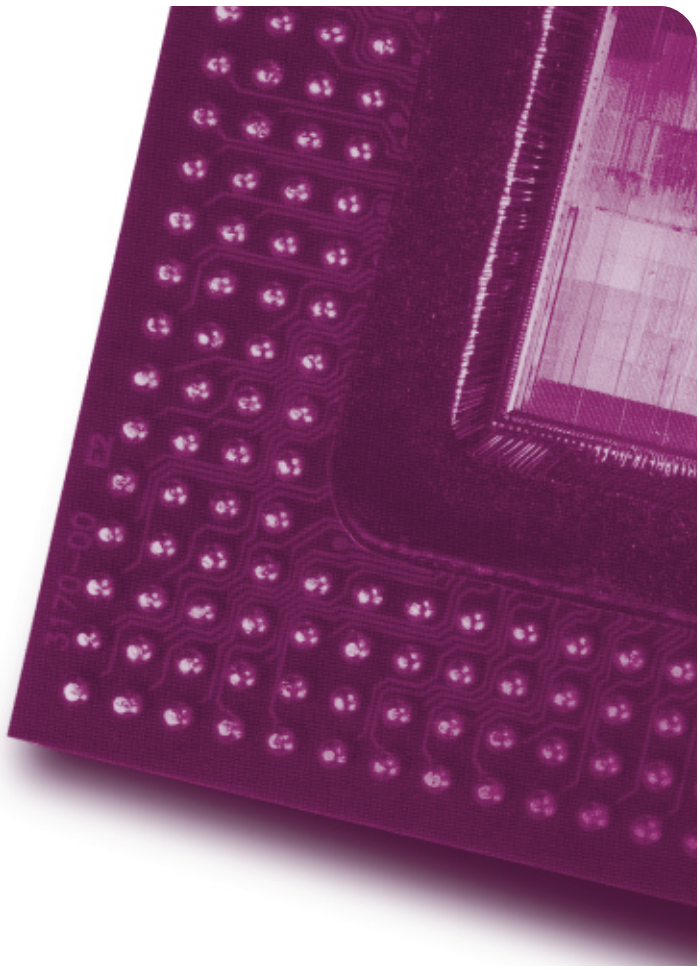
SPDIF output unit—The NX-2700 processor's SPDIF output block, SPDO, allows generation of a one-bit, high-speed serial data stream. The primary application is output of SPDIF (Sony/Philips Digital Interface) data for use by external audio equipment supporting the SPDIF format. The two-channel SPDIF datastream can contain one or more embedded Dolby Digital six-channel datastreams or one or more embedded MPEG-1 or MPEG-2 audio streams. Though SPDIF dictates format, the content of the SPDIF datastream is entirely software programmable. How the SPDO unit is used is determined by DTV product developers. Like the other audio units, SPDO allows arbitrary, programmable, sample rates from one Hz to 300 kHz.

SYSTEM CONTROL & EXTERNAL COMMUNICATIONS

Synchronous serial interface—Through its synchronous serial interface (SSI), NX-2700 provides V.34/V.90 remote communication support for interactive datacasting applications requiring a reverse communications channel or Internet connection. The SSI unit connects to an off-chip modem analog front end, network terminator, ADC/DAC, or Codec through a flexible bit-serial connection and performs full-duplex serialization/deserialization of a bitstream from any of these devices.

In DTV applications, the external front-end chip and phone line interface required for V.34/V.90 communications are provided on the reference board included in the NX-2700 DTV Developers Kit. V.34 communications is implemented in software enabling support for a wide variety of modem, network, and fax protocols.

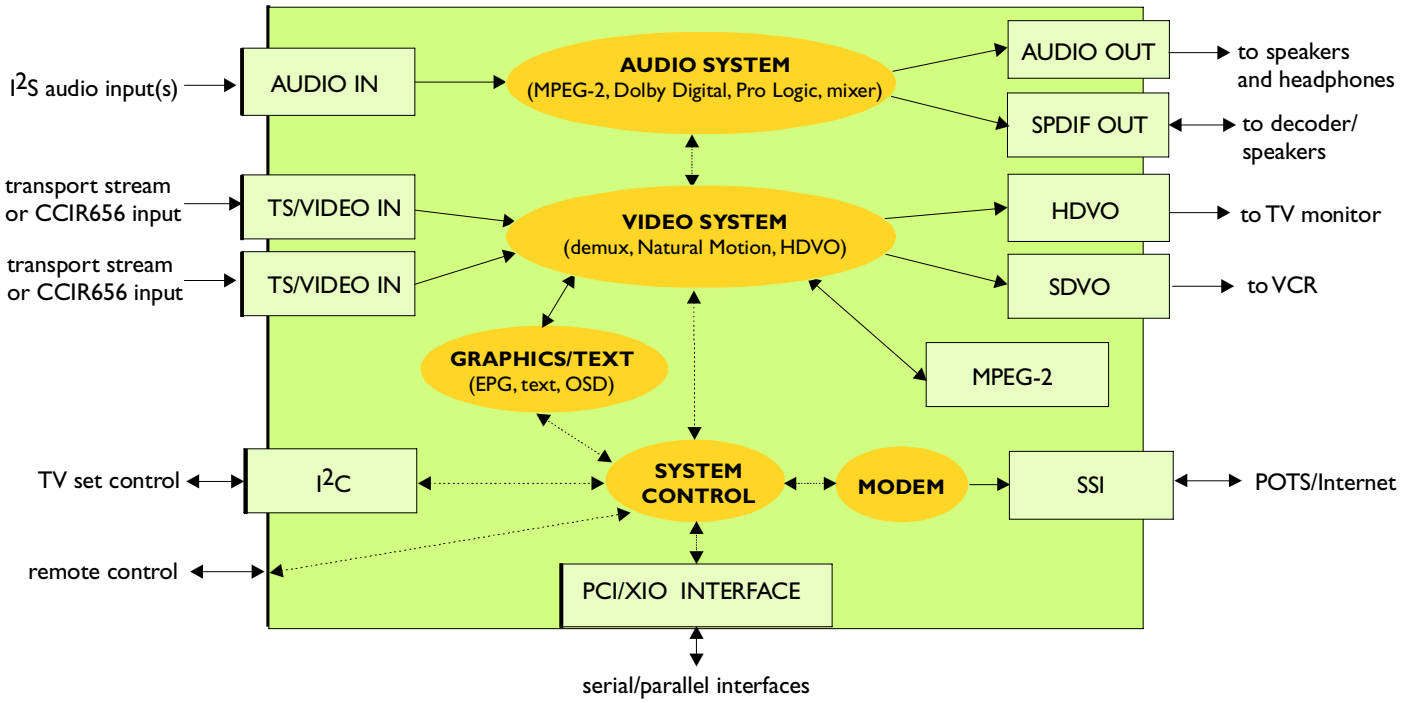
I^2C master-slave interface—The NX-2700 includes an I^2C interface used to control or be controlled by a variety of off-chip multimedia devices such as digital multi-standard decoders, VSB tuners, DACs, digital encoders, and parallel I/O expanders. It implements a single-master only mode and multiple slave mode functions. Master mode allows NX-2700 to configure and inspect status of peripheral devices. Slave mode allows an external I^2C master to access the NX-2700 main memory and device MMIO address space. The I^2C pins are also used to load the initial boot parameters or code from a serial EEPROM and can be programmed to implement software I^2C or similar protocols.



PCI bus interface with XIO support—NX-2700 includes a simple, glueless PCI/XIO bus interface for easy integration with systems using a PCI bus to connect high-speed peripherals. The PCI bus interface is also handy for PC-based DTV product development. The time-multiplexed eight-bit XIO bus allows glueless connection to general-purpose chips such as ROM, flash EEPROM and 68K and x86 peripheral devices. The XIO bus shares the PCI bus signals without conflict to PCI or XIO devices.

System boot sequence—NX-2700 implements low-level system initialization by combining a small block of on-chip system boot logic with a single external serial boot EEPROM connected to its I^2C interface. Both host-assisted and standalone bootstrapping are supported.

Multi-level power management—NX-2700 software-controlled power management features include both global power-down and block-level power shut-down modes. In global mode most on-chip clocks are shut down and main memory is brought into low-power self-refresh mode. In block-level mode, an individual block can be shutdown completely by disabling its clock.



NX-2700 HDTV SOFTWARE
The DTV software suite includes modules to handle audio, video, graphics, data, control, and communications processing.

MEMORY HIERARCHY & INTERNAL COMMUNICATIONS

To ensure the high bandwidth and low latency required for real-time video and audio I/O, NX-2700 uses two high-performance internal buses to interconnect its CPU, peripheral blocks, and main memory interface.

Local RAM—Processing multimedia video streams can require a significant amount of memory for temporary storage. NX-2700's support for SDRAM and SGRAM minimizes the cost of bulk memory. Synchronous DRAM (SDRAM) provides a fast, synchronous interface with higher bandwidth and a narrower, simpler interface than standard DRAM. Similar to SDRAM augmented with additional features to accelerate raster graphics functions, synchronous graphics DRAM (SGRAM) can also be used.

A variety of memory device types, speeds, and rank sizes are supported allowing a range of NX-2700-based system configurations to be built. In addition, memory-system speed can differ from NX-2700 core speed; the ratio between clock speeds is programmable.

Main memory interface—A dedicated, glueless 64-bit main memory interface (MMI) connects the NX-2700 to a local memory system. The MMI provides all control and data signals with sufficient drive capacity for a glueless connection to a 150-MHz memory system of up to eight memory chips.

The MMI takes advantage of the on-chip interleaving of SDRAM devices to deliver sustainable full-bandwidth data transfer. It contains the SDRAM controller, MMIO logic, the data-highway arbiters, and the central arbiter that determines how much of the available memory bandwidth will be allocated to each on-chip processing unit.

Separate instruction and data caches—NX-2700's separate, dedicated on-chip caches supply the majority of instructions and data to the CPU. Serving only the CPU, dual-ported data cache allows two concurrent memory accesses. Many techniques, such as cache locking, early restart, and background copyback are employed to ensure high cache hit rates and reduce read latency and CPU stalls. To reduce internal bus bandwidth requirements, instructions in main memory and cache use a compressed format. Cache coherency is maintained in software.

Dual, high-speed internal data highways—NX-2700's processing units access the external SDRAM through dual on-chip data buses, or data highways. Most peripheral units and the TriMedia CPU communicate across a 32-bit highway. A 64-bit highway connects the HDVO and MPEG-2 units to the MMI unit for main memory transactions and to the 32-bit highway for control transactions. The 32-bit highway interfaces with the MMI and thus with main memory through a bridge.

To move the data efficiently, both internal highways use separate address and data buses. Main memory bus transactions use a block-transfer protocol. On-chip peripheral units and coprocessors can be masters or slaves on their respective buses.

NX-2700's true real-time bus allocation mechanism incorporates an independent arbiter in the MMI unit for each bus. The arbitration algorithm can be programmed to meet the latency and bandwidth demands of any application.

HDTV DEVELOPMENT SUPPORT

Unlike all- or mostly-hardware embedded solutions, NX-2700's programmability and the robust TriMedia software development tools enable it to be configured or customized for an unlimited variety of HDTV products. The NX-2700 DTV Developers Kit is available to jump-start product development efforts. The Kit includes a NX-2700-based reference board, a suite of DTV software libraries, and the TriMedia Software Development Environment (SDE).

Comprehensive software development environment—The TriMedia SDE is a full suite of system software tools to compile and debug code, analyze and optimize performance and simulate execution for the NX-2700 processor.

By enabling development of DTV applications in C and C++, the SDE dramatically lowers development costs, reduces product time-to-market, and ensures code portability to next generation architectures. The SDE includes the TCS compilation tools (compiler, loader, scheduler, assembler, simulator), performance analysis and optimization tools, and device and application libraries required to drive all NX-2700 on-chip peripheral units.

DTV software suite—The DTV software suite includes key drivers and application modules needed for various DTV end products. Together the DTV suite and SDE enable CE developers to quickly create core DTV products or customize a range of product form factors, features levels, and price points.

JTAG debugging support—The IEEE 1149.1 (JTAG) standard is used for board-level and internal IC testing and for monitoring and modification of a running system. NX-2700 provides a four-pin JTAG port for communication between a debug monitor running on the CPU and a debugger front-end running on the development host.

Programmable GPIO pins—NX-2700 includes 19 pins usable by any software application for general purpose I/O (GPIO). These pins are useful for a variety of system functions including infrared remote input, printer output, software controllable switches in the system logic, software communication links, and more. In addition to the GPIO pins, pins of other on-chip peripheral blocks may be reassigned when they are not in use.

NX-2700 Specifications

PHYSICAL

Process	0.25 m, 5-layer metal CMOS
Packaging	VBGA
Pins	352
Voltage	DC input voltage on 2.5V pins: -0.5 2.75 V DC input voltage on 3.3V pins: -0.5 3.465 V
Power	external interface: 3 pins supply voltage: V_{DD2} 2.5 ±10%; V_{DPS} 3.3 ±10; electrostatic handling all pins: ±2000 V
Temperature	storage: -65 to 150°C; operating: 0 to 70°C

CPU

Instruction Length	variable (2 to 26 bytes); compressed
Addressing	32-bit linear address space
Instruction Set	arithmetic and logical ops, load/store ops., special multimedia and DSP ops., IEEE-compliant floating point ops.
Issue Slots	5
Functional Units	27, pipelined: integer and floating-point units, data-parallel DSP-like units
Registers	128 32-bit general purpose; hardware program counter; 4 user-accessible special purpose, dual load-store
Timers	4 programmable (3 general purpose, 1 system software)
Special Ops	32

DATA CACHE

Size	16 KB
Associativity	8-way set-associative with LRU replacement; 32 sets each containing 8 tags
Block Size	64-bytes; 1 valid bit/block; 1 dirty bit/block
Miss Transfer Order	miss transfers begin with first word in the block
Replacement Policies	Copyback, allocate on write, hierarchical LRU (least-recently used)
Endianness	little or big endian
Ports	quasi-dual ported (2 accesses can proceed concurrently if referencing different banks)
Alignment	32-bit words access on 32-bit boundaries, 16-bit half-words access on 16-bit boundaries
Partial Word Ops	implements byte and 16-bit accesses with the same performance as 32-bit accesses
Transfers	32-bit, 16-bit, 8-bit
Coherency	software controlled through special ops
Cache Locking	up to half (4/8 blocks of each set) cache contents can be locked; 64-byte granularity

NX-2700 Specifications

INSTRUCTION CACHE

Size	32 KB
Associativity	8-way set-associatiive with LRU replacement
Block Size	64 bytes
Valid Bits	one valid bit per block
Replacement Policy	hierarchical LRU among the 8-block set
Coherency	enforced through special op (software)
Cache Locking	up to half (4/8 blocks of each set) cache contents can be locked; granularity is 64 bytes

MEMORY SYSTEM & MAIN MEMORY INTERFACE

Bandwidth	1.2 GB/sec
CPU/Memory Speed Ratios	programmable; 1:1, 5:4, 4:3, 3:2, 2:1
Size	2 to 64 MB
Supported Types	Jedec SDRAM (x16, x32); Jedec SGRAM (x32, DSF tied low)
Data Width	64-bit (SDRAM); 32-bit (SGRAM)
Ranks	2 chip-select signals support up to 2 ranks
Interface	glueless up to 8 chips; supports 16- and 64-Mbit SDRAM
Signal Levels	3.3-V LVTTL
MMI External Interface	96 pins (excluding power and ground)

VIDEO/TRANSPORT STREAM IN

No. Units	2
Bandwidth	38 MHz
Supported Inputs	digital CCIR601-resolution video signal MPEG-2 transport stream per ISO/IEC 13818-1 standard raw 8- or 10-bit unidirectional data messages
Functions	signal input; timestamp; PID filtering

MPEG-2 ACCELERATOR

Capacity	slice-level decoding up to MP@HL (1080I)
Functional Units	variable length decoder; run-level decoder and inverse scan block; inverse quantization block; inverse discrete cosine transform (IDCT) block; motion compensation (MC) block
IDCT Unit	IEEE compliant
MC Unit	supports MPEG-1; MPEG-2 MP@ML and MP@HL
Modes	full- and half-resolution
Performance	at least 1 (Y, U, or V) pixel per cycle
Error Concealment	CPU control
External Interface	none

STANDARD DEFINITION VIDEO OUT

Output Formats	CCIR601/656 8-bit video, PAL or NTSC
Resolutions	flexible, including CCIR601; max. 4K x 4K pixels (subject to 80 MB/sec data rate)
Clock Rates	programmable (4-80 MHz), typically 27 MB/sec (13.5 Mpixels/sec for NTSC, PAL)
Transfer Speeds	80 MB/sec in data streaming and message passing modes; 40 Mpix/sec in YUV 4:2:2 mode

HIGH DEFINITION VIDEO OUT

Output Resolutions	all ATSC formats up to 1920 x 1080 60I
Output Formats	RGB 10:10:10; YUV 4:2:2; YUV 4:4:4
RGB/YUV Component Size	8- or 10-bit
Supported Inputs	TriMedia YUV, planar YUV 4:2:0, 4:2:2, RGB2 to RGB8, RGB565, RGB555+1, RGB8:8:8, RGBa324:2:2 co-sited, 4:2:2 interspersed, 4:2:0 interspersed
Bandwidth	100 Mpixels/sec (240 MB/s)
Output Interface	programmable; up to 30 bits
Scaling/Clipping	programmable; arbitary vertical or horizontal scaling (.25 to 4.0) full vertical scaling (4-tap filter for HD resolution, 6-taps for resolution lower or equal to 1280 pixels per line)
Synchronization	genlock mode frame synchronization by an external signal; HDVO can be sync master or slave
Horizontal Upsampling	2X up- or down-sampling (4:2:0 to 4:4:4, 4:4:4 to 4:2:0); interspersed to co-sited; co-sited to co-sited
Horizontal Filters	6-tap; support direct polyphase mode (compression factors: 1 to 4.0) and transposed polyphase mode (compression factors: 1 to 0.25) programmed to work with 64 or 32 phases, 10-bit coefficients configurable as a simple 11- or 12-tap sym metrical FIR filter for signal processing time-share mode saves and restores current context coefficient bank splits to two independent banks for 2 filters with different coefficients on the same unit

NX-2700 Specifications

	automatic right or left mirroring, for correct image hedges variable zoom
Vertical Filters	software controlled; programmable as a linear filter with up to 6 phases (direct polyphase only); integrated de-interlacing filters (linear or median)
Matrix/Dematrix	RGB to YUV (4:4:4); YUV (4:4:4) to RGB; fully programmable matrix coefficients
Gamma Correction	programmable using look-up tables (LUT)

AUDIO IN

No. Units	2
Channels	2 channels per unit
Sample Size	8- or 16-bit samples per channel
Sample Rates	programmable, 1-Hz to 100 KHz with 0.001 Hz resolution (independent rates each unit)
Data Formats	8-bit mono and stereo, 16-bit mono and stereo PC standard memory data format
Clock Source	internal or external
Memory Formats	little and big endian
Native Protocols	I^2S and other serial 3-wire protocols
External Interface	4 pins each unit; 1 programmable clock output, 3 flexible serial data inputs

FOR MORE INFORMATION CONTACT:

PHILIPS SEMICONDUCTORS TRIMEDIA BUSINESS LINE
811 EAST ARQUES AVENUE, M/S 71, SUNNYVALE CA 94088-3409
PH 800-914-9239 (NORTH AMERICA), 408-991-3838 (WORLDWIDE)
FX 408-991-3300, E-MAIL info@trimedia.sv.sc.philips.com
WEBSITE www.trimedia.philips.com

Philips Semiconductors - a worldwide company

Argentina: see South America
Australia: Tel. +61 2 9805 4455 Fax. +61 2 9805 4466
Austria: Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210
Belarus: Tel. +375 172 20 0733, Fax. +375 172 20 0773
Belgium: see The Netherlands
Brazil: see South America
Bulgaria: Tel. +359 2 68 9211, Fax. +359 2 68 9102
Canada: Tel. +1 800 234 7381, Fax. +1 800 943 0087
China/Hong Kong: Tel. +852 2319 7888, Fax. +852 2319 7700
Colombia: see South America
Czech Republic: see Austria
Denmark: Tel. +45 33 29 3333, Fax. +45 33 29 3905
Finland: Tel. +358 9 615 800, Fax. +358 9 6158 0920
France: Tel. +33 1 4099 6161, Fax. +33 1 4099 6427
Germany: Tel. +49 40 2353 60, Fax. +49 40 2353 6300
Hungary: see Austria
India: Tel. +91 22 493 8541, Fax. +91 22 493 0966
Indonesia: Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080
Ireland: Tel. +353 1 7640 000, Fax. +353 1 7640 200
Israel: Tel. +972 3 645 0444, Fax. +972 3 649 1007
Italy: Tel. +39 2 6752 2531, Fax. +39 2 6752 2557
Japan: Tel. +81 3 3740 5130, Fax. +81 3 3740 5077
Korea: Tel. +82 2 709 1412, Fax. +82 2 709 1415
Malaysia: Tel. +60 3 750 5214, Fax. +60 3 757 4880
Mexico: Tel. +9-5 800 234 7381, Fax. +9-5 800 943 0087
Middle East: see Italy
Netherlands: Tel. +31 40 27 82785, Fax. +31 40 27 88399
New Zealand: Tel. +64 9 849 4160, Fax. +64 9 849 7811
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