12-Bit 20MSPS Sampling Analog-to-Digital Converter

nAD2167

FEATURES

- 2.7-3.6V power supply
- SINAD typ. 64dB for (f_{in} = 5MHz)
- Low power (200mW@3.3V)
- Sample rate: > 20MSPS
- Internal Sample/Hold
- Differential input
- Low input capacitance

APPLICATIONS

- Imaging
- Test equipment
- Computer scanners
- Communications
- Set top boxes

GENERAL DESCRIPTION

The nAD2167 is a compact, high-speed, low power 12-bit monolithic analog-to-digital converter, implemented in a 0.5µm CMOS process. It has 12-bit resolution with close to 11 effective bits, and more than 11 bit dynamic range for video signals. The converter includes sample and hold. The full scale range can be set between ±0.5V and ±1V using external references. It operates from a single 2.7-3.6V supply - compatible with modern digital systems. Most converters in this performance range demand at least a +5V supply. Its low distortion and high dynamic range offers the performance needed for demanding imaging, multimedia, telecommunications and instrumentation applications.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage		2.7	3.3	3.6	V
I_{DD}	supply current			60		mA
P_D	power dissipation			200		mW
DNL	differential nonlinearity	f_{IN}=0.9991MHz			±0.5	LSB
INL	integral nonlinearity	f_{IN}=0.9991MHz			±1	LSB
f_S	max conversion rate		20		TBD	MHz
N	resolution				12	bit

Table 1. Quick reference data

GENERAL DESCRIPTION (Continued)

The nAD2167 has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 11 most significant bits ensures good linearity for input frequencies approaching Nyquist. The excellent linearity at the color subcarrier frequency makes the converter ideally suited for video. It is also well suited for demanding ultrasonic imaging and flow measurements. The nAD2167 is very compact - occupying less than 4mm^2 of die area in a standard dual poly 0.5µm CMOS process. The fully differential architecture makes it insensitive to substrate noise. Thus it is ideal as a mixed signal ASIC macro cell.

BLOCK DIAGRAM

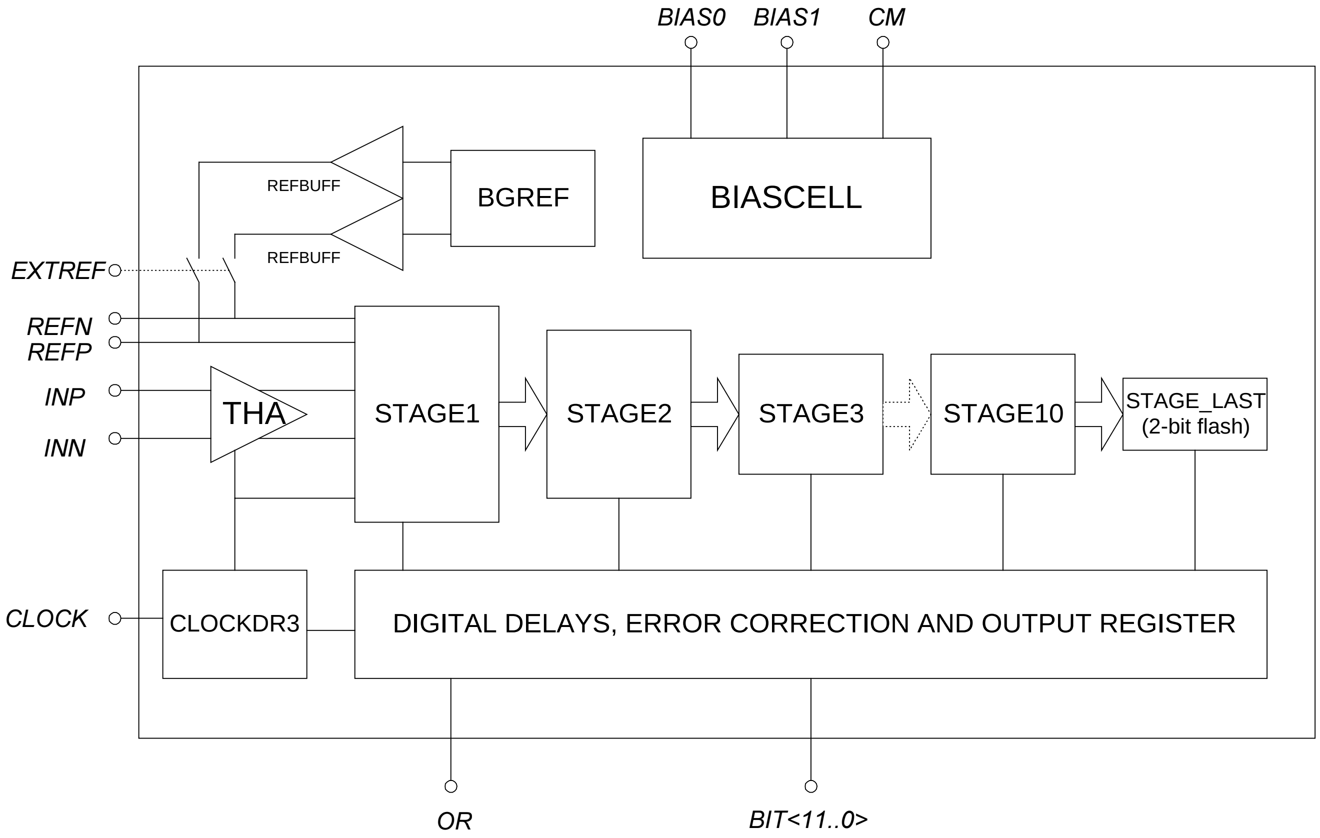


Figure 1. Block diagram nAD2167

ELECTRICAL SPECIFICATIONS

(At T_A = 25°C, V_{DD} = 3.0V, Sampling Rate = 20MHz, Input frequency = 4.4995MHz, Differential input signal, 50% duty cycle clock with 2.5ns rise and fall times unless otherwise noted)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Units
	DC Accuracy					
DNL	Differential Nonlinearity					
	f_{IN} = 0.9991 MHz	I			±0.5	LSB
INL	Integral Nonlinearity					
	f_{IN} = 0.9991 MHz	I			±1.0	LSB
V_{OS}	Midscale offset	I			10	LSB
CMRR	Common Mode Rejection Ratio	V		TDB		
ε_G	Gain Error	I		TBD		
	Dynamic Performance					
SINAD	Signal to Noise and Distortion Ratio					
	f_{IN} = 4.4995 MHz	I	62	64		dB
	f_{IN} = 18.9991 MHz	I		60		dB
SNR	Signal to Noise Ratio (without harmonics)					
	f_{IN} = 4.4.995 MHz	I	66	68		dB
	f_{IN} = 18.9991 MHz	I		64		dB
SFDR	Spurious Free Dynamic Range					
	f_{IN} = 4.4995 MHz	I	66	71		dB
	f_{IN} = 18.9991 MHz	I		63		dB
DP	Differential Phase	V		TBD		
DG	Differential Gain	V		TBD		
PSRR	Power Supply Rejection Ratio	V		TBD		
	Analog Input					
V_{FSR}	Input Voltage Range (differential)	V		±1	±1.3	V
V_{CMI}	Common mode input voltage	V		1.5		V
C_{INA}	Input Capacitance (from each input to ground)	V		4		pF
	Reference Voltages					
V_{REFNI}	Internal reference voltage on pin 10		0.95	1.0	1.05	V
V_{REFPI}	Internal reference voltage on pin 11		1.95	2.0	2.05	V
	Internal reference voltage drift				100	ppm/°C
V_{REFNO}	Negative Input Voltage	VI	0.7	1.0	1.3	V
V_{REFPO}	Positive Input Voltage	VI	1.7	2.0	2.3	V
V_{REFP}-V_{REFN}	Reference input voltage range	V	0.6	1.0	1.5	V
V_{CM}	Common mode output voltage	VI	TBD	1.65	TBD	V
	Digital Inputs					
V_{IL}	Logic “0” voltage	VI			20% V_{DD}	
V_{IH}	Logic “1” voltage	VI	80% V_{DD}			
I_{IL}	Logic “0” current (V_I=V_{SS})	VI			±10	µA
I_{IH}	Logic “1” current (V_I=V_{DD})	VI			±10	µA
C_{IND}	Input Capacitance	V		1.2		pF
	Digital Outputs					
V_{OL}	Logic “0” voltage (I = 2 mA)	VI		0.2	0.4	V
V_{OH}	Logic “1” voltage (I = 2 mA)	VI	85% V_{DD}	90% V_{DD}		V
t_H	Output hold time	VI		5		ns
t_D	Output delay time	VI		8		ns

(table continued on next page)

	Switching Performance					
f_S	Conversion Rate	VI	20		TBD	MSPS
	Pipeline Delay (see timing diagram)	IV		8		Clocks
σ_{AP}	Aperture jitter	V		10		ps
t_{AP}	Aperture delay	V		2		ns
	Power Supply					
V_{DD}	supply voltage	V	2.7	3.3	3.6	V
I_{DD}	supply current	VI		63		mA
V_{SS}	supply voltage			GND		
AV_{DD}-DV_{DD1}	analog power – digital power pins		-0.2		+0.2	V
DV_{DD1}-DV_{DD2}	digital power – output driver power		-0.2		+0.2	V
P_D	Power dissipation	VI		200		mW
T	Ambient operating temperature		-40		+85	°C

Table 3. Electrical specifications

Test Levels

Test Level I: 100% production tested at +25°C
Test Level II: 100% production tested at +25°C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterization testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25°C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages

AV_{DD}............................... - 0.3V to +6V
DV_{DD1} .... - 0.3V to V_{DD} + 0.3V
DV_{DD2} .... - 0.3V to V_{DD} + 0.3V

Input voltages

Analog In .... - 0.3V to AV_{DD} + 0.3V
Digital In............. - 0.3V to V_{DD} + 0.3V
REF_P................. - 0.3V to AV_{DD} + 0.3V
REF_N .... - 0.3V to AV_{DD} + 0.3V
CLOCK............... - 0.3V to V_{DD} + 0.3V

Temperatures

Operating Temperature ….-55 to +95°C
Storage Temperature......- 65 to +125°C

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
IN_P IN_N	Differential input signal pins. Common mode voltage: 1.65V
REF_P REF_N	Reference input pins. Bypass with 100nF capacitors close to the pins. See Application Information below.
EXTREF	Digital input: Reference select. EXTREF=1: Internal reference powered down, use external reference EXTREF=0: Internal reference is used
BIAS0, BIAS1	Digital inputs for max. sampling rate programming. BIAS1=0, BIAS0=0: Sleep mode (power save) BIAS1=0, BIAS0=1: Max. 5MHz sampling BIAS1=1, BIAS0=0: Max. 20MHz sampling (default by internal pull-up/pull-down) BIAS1=1, BIAS0=1: Max. 30MHz sampling
CLOCK	Clock input
CM	Common mode voltage output.
BIT11 - BIT0	Digital outputs (MSB to LSB)
OR	Digital output. OR=1 indicates input out of range
BGAP	Band gap reference output, nominally 2.415V Option for characterization purposes: BGAP can be used to override internal bias currents in ADC by applying external voltage (BGAP input resistance, approx. 5kohm). Bias current will be proportional to applied voltage. When this option is used, external references must be used, as it will influence the operation of the internal voltage references!
AV_{DD}	Analog power pins. Should be connected to V_{DD}
DV_{DD1}	Digital power pins. Should be connected to V_{DD}
DV_{DD2}	Power pins for output drivers. Should be connected to V_{DD}

Table 4. Pin functions

PIN ASSIGNMENT

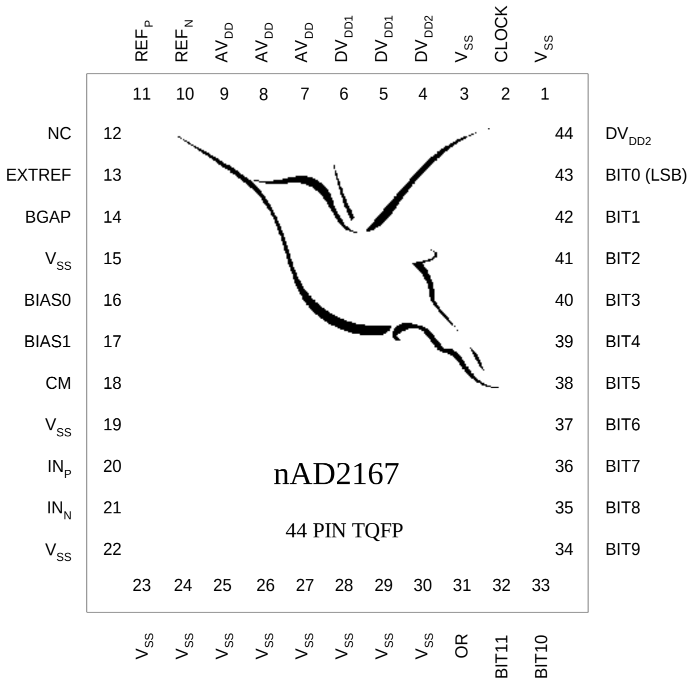


Figure 2. Pin assignment

TIMING DIAGRAM

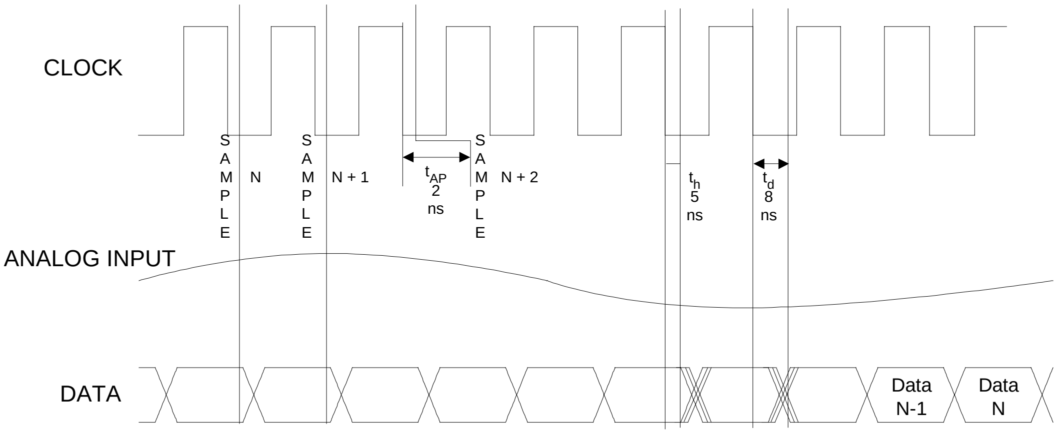


Figure 3. Timing diagram

TYPICAL PERFORMANCE CURVES

At T_A = 25°C, V_{DD} = 3.0V, Input frequency = 4.4995MHz , Sampling Rate = 20MHz, with a 50% duty cycle clock with 2.5ns rise and fall times, Full scale range = 2V, unless otherwise noted

INL
Input frequency: 0.9991MHz

DNL
Input frequency: 0.9991MHz

SPECTRAL PERFORMANCE
INPUT FREQUENCY = 4.5MHz

SPECTRAL PERFORMANCE
INPUT FREQUENCY = 9.5MHz

DYNAMIC PERFORMANCE
vs FULL SCALE RANGE

HARMONIC DISTORTION
vs FULL SCALE RANGE

SWEPT POWER SNR, SINAD

SWEPT POWER SFDR

DYNAMIC PERFORMANCE
vs SAMPLING FREQUENCY

SMALL SIGNAL
FREQUENCY RESPONSE

DYNAMIC PERFORMANCE
vs REFERENCE COMMON MODE

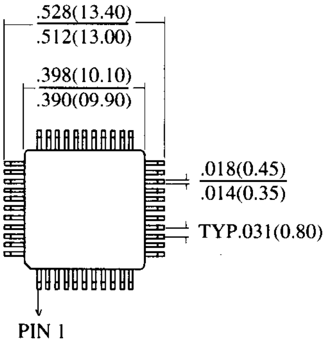
DYNAMIC PERFORMANCE
vs TEMPERATURE

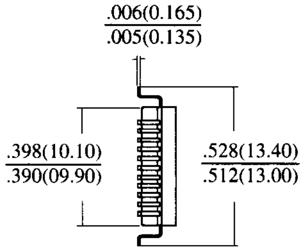
DYNAMIC PERFORMANCE
vs TEMPERATURE (V_{DD} = 2.7V)

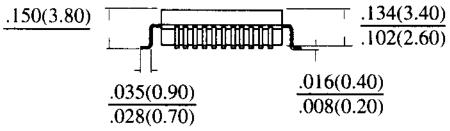
DYNAMIC PERFORMANCE
vs TEMPERATURE (V_{DD} = 3.3V)

OFFSET vs TEMPERATURE

PACKAGE OUTLINE







All dimensions are in inches and paranthetically in millimeters.

Figure 5. Package outline

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 5. Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION (section to be revised!)

References

The nAD2167 has a differential analog input. The input range is determined by the voltages V_P and V_N applied to reference pins REF_P and REF_N respectively, and is equal to $\pm(V_P\text{-}V_N)$. Externally generated reference voltages connected to REF_P and REF_N should be symmetric around 1.5V. The input range can be defined between ±0.6V and ±1.5V. An internal reference exists – providing reference voltages at pins REF_P and REF_N equal to +2.00V ($VREF_P$) and +1.00V ($VREF_N$). These can be connected to REF_P and REF_N by connecting pin EXTREF to VSS. The references should be bypassed as close to the converter pins as possible using 100nF capacitors in parallel with smaller capacitors (e.g. 220pF) (to ground).

Analog input

The input of the nAD2167 can be configured in various ways - dependent upon whether a single ended or differential, AC- or DC-coupled input is wanted.

AC-coupled input is most conveniently implemented using a transformer with a center tapped secondary winding. The center tap is connected to the CM-node, as shown in figure 1. In order to obtain low distortion, it is important that the selected transformer does not exhibit core saturation at full-scale. Excellent results are obtained with the Mini Circuits T1-6T or T1-1T. Proper termination of the input is important for input signal purity. A small capacitor (typ. 68pF) across the inputs attenuates kickback-noise from the sample and hold. A small capacitor (1nF) between CM and ground has also been proven to be advantageous.

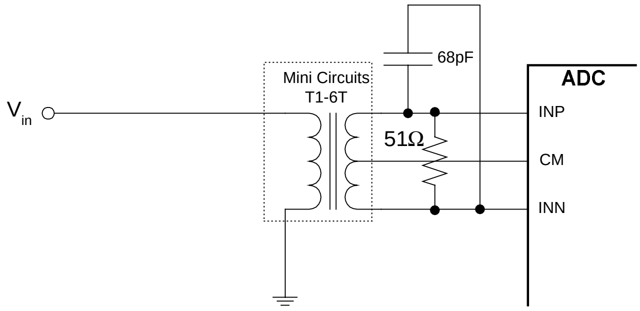


Figure 6. AC coupled input using transformer

If a DC-coupled single ended input is wanted, a solution based on operational amplifiers - as shown in Figure 7, is usually preferred. The AD826 is suggested for low distortion and video bandwidth. Lower cost operational amplifiers may be used if the demands are less strict.

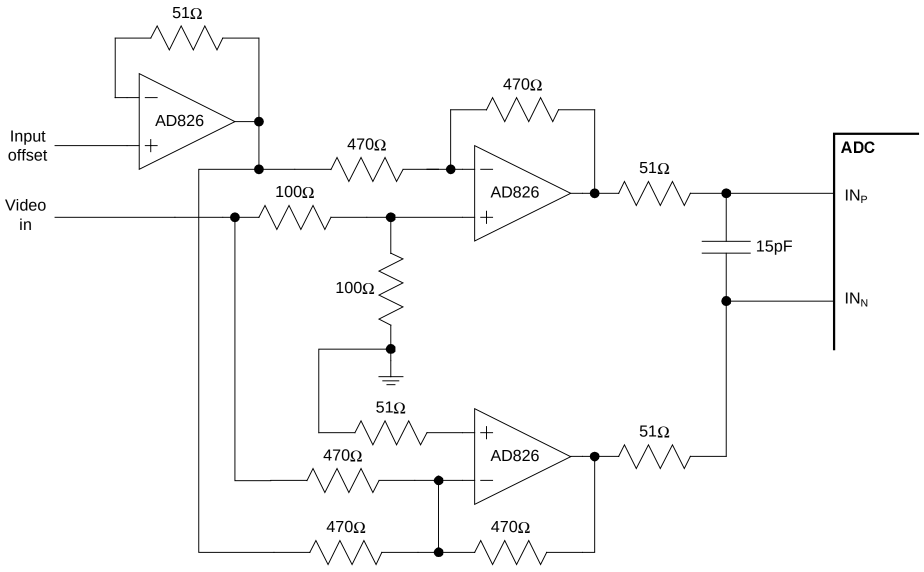


Figure 7. DC-coupled single ended to differential conversion (power supplies and bypassing not shown)

Clock

The nAD2167 accepts a CMOS logic level clock at the CLK-node. The duty cycle of the clock should be close to 50%. Consecutive pipeline stages in the ADC are clocked in antiphase. With a 50% duty cycle, every stage has the same time for settling. If the duty cycle deviates from 50%, every second stage has a shorter time for settling - thus it operates less accurately, causing degradation of SNR.

In order to preserve accuracy at high input frequency, it is important that the clock has low jitter and steep edges. Rise/fall times should be kept shorter than 2ns whenever possible. Overshoot should be avoided. Low jitter is especially important when converting high frequency input signals. Jitter causes the noise floor to rise proportionally to input signal frequency. Jitter may be caused by crosstalk on the PCB. It is therefore recommended that the clock trace on the PCB is made as short as possible.

Digital outputs

The digital output data appears in offset binary code at CMOS logic levels. Full scale negative input results in output code 000...0. Full scale positive input results in output code 111...1. Output data are available 7.5 clock cycles after the data are sampled. The analog input is sampled one aperture delay (t_{AP}) after the high to low clock transition. Output data should be sampled on the low to high clock transition, as shown in the timing diagram.

PCB layout and decoupling

A well designed PCB is necessary to get good spectral purity from any high performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC are connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered. One should make sure that the analog and digital supply voltages are equal.

Dynamic testing

Careful testing using high quality instrumentation is necessary to achieve accurate test results on high speed A/D-converters. It is important that the clock source and signal source has low jitter. A spectrally pure, low noise RF signal generator - such as the HP8662A or HP 8644B is recommended for the test signal. Low pass filtering or band pass filtering of the input signal is usually necessary to obtain the required spectral purity (SFDR > 75dB). The clock signal can be obtained from either a crystal oscillator or a low-jitter pulse generator. Alternatively, a low-jitter RF-generator can be used as a clock source. At Nordic VLSI, the Marconi Instruments 2041A is used. The sinewave clock must then be applied to an ultra high speed comparator (e.g. AD9696) and a TTL to CMOS level shifter (e.g. 74LV04) before application to the converter. The most consistent results are obtained if the clock signal is phase locked to the input signal. Phase locking allows testing without windowing of output data. A logic analyzer with deep memory - such as the HP16500-series, is recommended for test data acquisition.

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