Nordic VLSI ASA

20-Bit Low Power Delta Sigma Modulator

nAD2001

FEATURES

- Low power (6mW)
- Standby mode
- 5 volt supply
- 0.7 mm^2 area
- 0.8µm dual poly CMOS process
- Available as macrocell
- 20 bit dynamic range in 20Hz bandwidth
- 17 bit dynamic range in 300Hz bandwith

APPLICATIONS

- Magnetic sensors
- Seismic instrumentation
- Medical instrumentation

GENERAL DESCRIPTION

The nAD2001 is a compact, second order delta sigma modulator. Only a decimation filter must be added to achieve a complete 20 bit or 17 bit A/D-converter. It utilizes a switched capacitor CMOS architecture to achieve low power dissipation and a high dynamic range. A fully differential implementation insures low sensitivity to interference from the digital part of the system, when the modulator is used as a macrocell in system ICs. The converter is very compact, typically occupying less than 0.7 mm^2 in a 0.8µm dual polysilicon CMOS technology.

The nAD2001 features a standby mode - in which the static current consumption is reduced to less than 1µA. It is therefore an excellent choice for battery operated systems.

QUICK REFERENCE DATA

(Conditions: 25°C, 5V supply, 2.25V input range)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		4.75	5.0	5.25	V
I_{DD}	Supply current			1.1		mA
P_D	Power dissipation			5.5		mW
SNR	Signal to noise ratio	f_{IN} = 20Hz		116		dB
SINAD	Signal to noise and distortion ratio	f_{IN} = 20Hz		116		dB
V_{OS}	Offset error				TBD	mV
C_I	Input capacitance			10		pF
f_{CK}	Clock frequency				620	kHz
T_{OPER}	Operating temperature range		-40		85	°C

Table 1. Quick reference data

ORDERING INFORMATION

Type number	Name	Description	Version
nAD2001-CORE	CORE	layout in GDSII-format	c-1

Table 2. Ordering information

BLOCK DIAGRAM

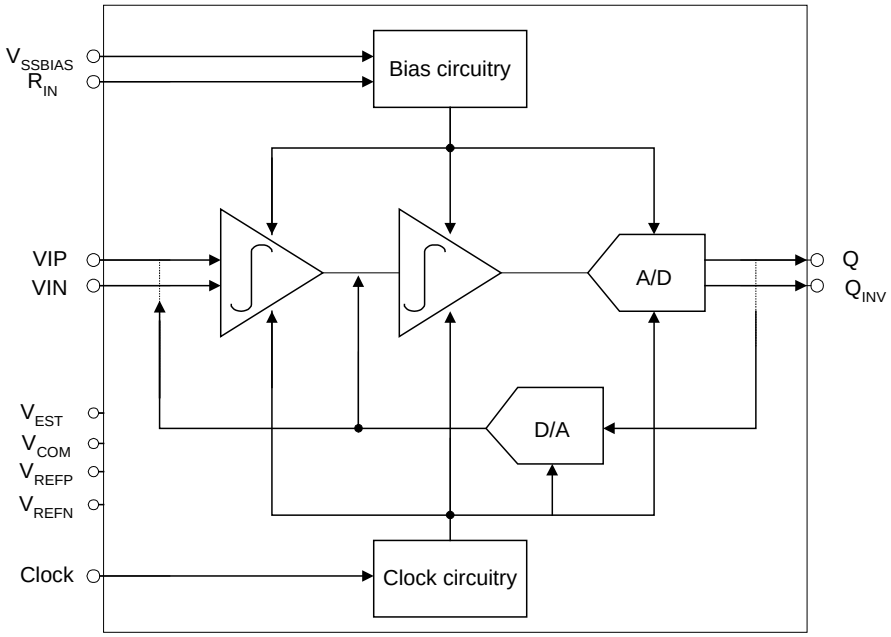

Figure 1. Block diagram nAD2001

ELECTRICAL SPECIFICATIONS

(V_{DD} =5.0V, f_{CK} = 620kHz, T = 25°C)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Units
	DC Accuracy					
V_{OS}	Offset Error				TBD	mV
ε_G	Gain Error				TBD	
	Dynamic Performance					
SNR	Signal to Noise Ratio					
	f_{IN} = 20Hz			116*		dB
	f_{IN} = 300Hz			98*		dB
THD	Total Harmonic Distortion					
	f_{IN} = 20Hz			TBD		%
	f_{IN} = 300Hz			TBD		%
SINAD	Signal to Noise and Distortion Ratio					
	f_{IN} = 20Hz			116*		dB
	f_{IN} = 300Hz			98*		dB
	Analog Input					
V_{FSR}	Input Voltage Range (Differential)		- 2		+ 2	V
V_{CMI}	Common Mode Input Voltage		TBD	2.5	TBD	V
C_I	Input Capacitance			10		pF
	Reference Voltages					
V_{REFP}	Positive Input Voltage		TBD	3.5	TBD	V
V_{REFN}	Negative Input Voltage		TBD	1.5	TBD	V
	Digital Output					
V_{OL}	Logic “0” voltage				0.4	V
V_{OH}	Logic “1” voltage			90% V_{DD}		
	Power Supply					
V_{DD}	Supply Voltage		4.75	5.0	5.25	V
I_{DD}	Supply Current			1.1		mA
P_D	Power Dissipation			5.5		mW

* design target - 6dB

Table 3. Electrical specifications

Test Levels

Test Level I: 100% production tested at +25°C
Test Level II: 100% production tested at +25°C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterization testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25°C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages

Input voltages

Temperatures

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
VIN VIP	Differential input signal pins.
V_{REFP} V_{REFN}	Reference input pins. (V_{REFP} = 3.5V, V_{REFN} = 1.5V)
R_{IN}	Connect a 270kΩ resistor between AV_{DD} and R_{IN}. Connect a 100nF capacitor between V_{SSBIAS} and R_{IN} to protect the bias circuit from external and internal noise sources.
V_{EST}	Analog input. (V_{EST} = 1.2V)
V_{COM}	Analog input. (V_{COM} = 2.5V)
Clock	Clock input.
Q Q_{INV}	Digital outputs.
Sel_bias	Connect to $V_{SS.}$
Sub	Connect to ground.
AV_{DD}	Analog power.
DV_{DD}	Digital power.
AV_{SS}	Analog ground.
DV_{SS}	Digital ground.
V_{SSBIAS}	Ground pin for bias circuit, should not be connected to PCB-ground.

Table 4. Pin functions

PIN ASSIGNMENT

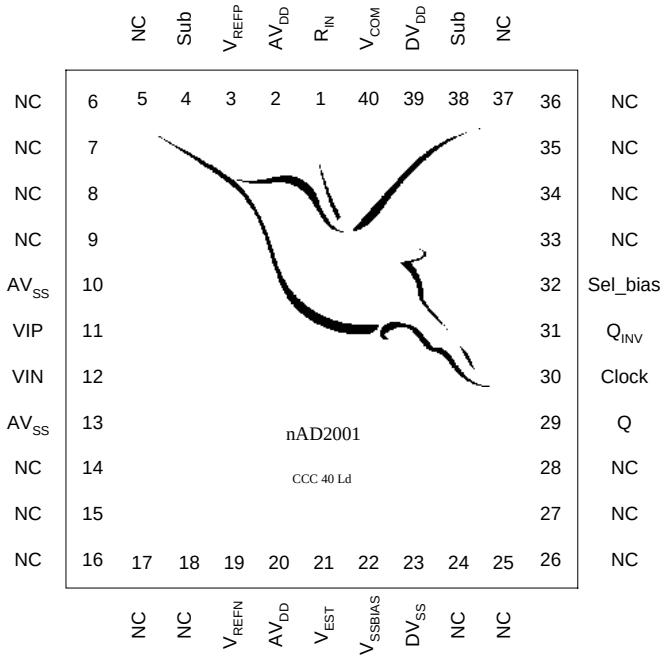

Figure 2. Pin assignment

TIMING DIAGRAM

To be included

Figure 3. Timing diagram

TYPICAL PERFORMANCE CURVES

To be included

Figure 4. Typical performance curves

PACKAGE OUTLINE

Encl.
Please note that the no. 1 pin marker is **under** the CCC40 package.

Figure 5. Package outline

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 5. Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

(Preliminary)

References
The references should be bypassed to ground using 100nF surface mounted capacitors as close - thar is, not more than 3mm from the package.

Analog input

Clock

Digital outputs

PCB layout and decoupling
A well designed PCB is necessary to get good spectral purity from any high performance ADC. A multilayer PCB with a solid ground plane is recommended for optimum performance. If the system has a split analog and digital ground plane, it is recommended that all ground pins on the ADC are connected to the analog ground plane. It is our experience that this gives the best performance. The power supply pins should be bypassed using 100nF surface mounted capacitors as close to the package pins as possible. Analog and digital supply pins should be separately filtered. One should make sure that the analog and digital supply voltages are equal.

Dynamic testing

To be inserted

YOUR NOTES

DESIGN CENTER

Nordic VLSI ASA
Vestre Rosten 81
N-7075 TILLER
NORWAY
Telephone: +47 72 89 89 00
Telefax: +47 72 89 89 89

E-mail: For further information regarding datasheets, please send mail to datasheet@nvlsi.no

World Wide Web/Internet: Visit our site at http://www.nvlsi.no

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