Nordic VLSI ASA

4th Order Delta-Sigma ADC Core for Audio

nAD1804

FEATURES

- Stereo
- 18-Bit Resolution
- Single 2.7-3.6 V Power Supply
- Low Power Dissipation
- Built-In Linear-Phase Decimator
- SNR typ. 91dBA (A-weighted)
- Switched Capacitor Design (CMOS)
- Differential Input
- Low Input Capacitance

APPLICATIONS

- Portable Audio Recording
- Sampling Synthesizers
- Digital Karaoke Systems
- Sound Reinforcement
- Active Noise Cancellation
- GSM/DECT Baseband Processing
- Audio PC Peripherals

GENERAL DESCRIPTION

The nAD1804 is a 4th order delta sigma modulator with MASH architecture and built-in decimation filter, suited for audio analog-to-digital conversion. The output word-length is 18-bit. The core targets 0.5µm and 0.35µm CMOS triple layer metal, dual layer poly processes. The output is 18-bit PCM with sampling frequency in the range from 32kHz to 48kHz. The full-scale range can be set between 1V and 2.3V using external references. It operates from a single 2.7-3.6V supply - compatible with digital ASICs. The core area for a complete stereo converter in a 0.35µm process is 6.5mm^2.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage		2.7	3.3	3.6	V
I_{DD}	supply current			28		mA
P_D	power dissipation			92		mW
f_S	output data rate		32		48	kHz
N	resolution			18		bits

Table 1: Quick reference data

GENERAL DESCRIPTION (Continued)

The nAD1804 uses delta-sigma modulation with 32X oversampling. A block diagram of the complete core is shown in Figure 1. The modulator architecture is a cascade of one 2nd order and two 1st order delta-sigma modulators. The 1-bit output from each

modulator is combined in the noise-cancellation logic, which cancel the quantization noise from all stages except the last. The multibit output from the noise-cancellation logic is feed to the decimation filter.

In the serial out interface the outputs from each channel is intermixed, and the digital output is available in serial format on three pins (LRCK, SCLK, SDATA).

BLOCK DIAGRAM

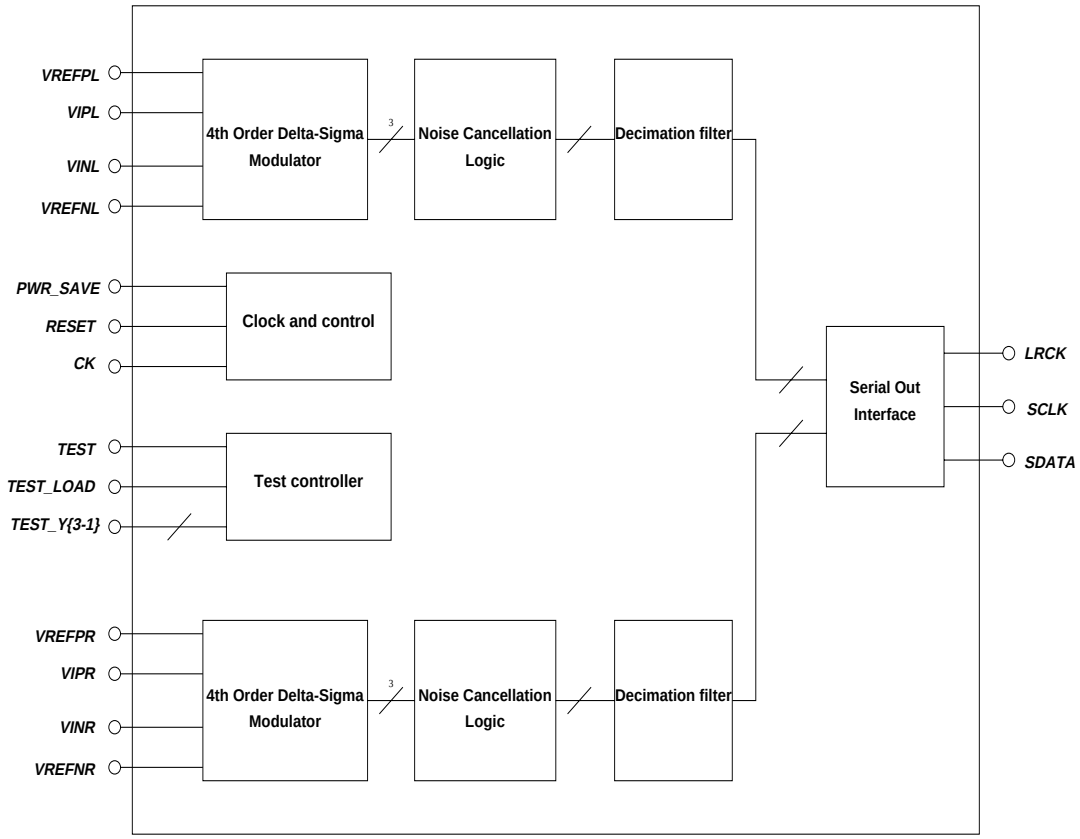

Figure 1: Block diagram nAD1804

ELECTRICAL SPECIFICATIONS

(At VDD = 3.3V, Clock frequency = 22.5792MHz, Input frequency = 999 Hz, Noise bandwidth: 20Hz to 20kHz, V_{ref} = 2.2V, input signal -2dBFS, 50% duty cycle clock with 2.5ns rise and fall times unless otherwise noted)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Unit
	Dynamic Performance					
SINAD	Signal to Noise and Distortion Ratio	III		88		
DR	Dynamic range (-60 dBFS input signal)					
	A-weighted	III		94		
	unweighted	III		91		
SNR	Signal to Noise Ratio (without harmonics)					
	A-weighted	III		91		dB
	unweighted	III		88		dB
SFDR	Spurious Free Dynamic Range	III		103		dB
	HD2	III		-109		dB
	HD3	III		-106		
PSRR	Power Supply Rejection Ratio			TBD		
	Analog Input					
V_{FSR}	Input Voltage Range (differential)			±2.2	±2.5	V
V_{CMI}	Common Mode Input Voltage			1.7		V
C_{INA}	Input Capacitance (from each input to ground)			10		pF
	Reference Voltages					
V_{REFN}	Negative Reference Voltage		0.5	1.0	1.2	V
V_{REFP}	Positive Reference Voltage		2.1	2.3	3.0	V
V_{REF}	Reference Input Voltage Range (V_{REFN}-V_{REF})		0.9	1.3	2.5	V
V_{CM}	Common Mode Input Voltage		TBD	1.65	TBD	V
	Digital Outputs					
V_{OL}	Logic “0” voltage (I = 2 mA)			0.2	0.4	V
V_{OH}	Logic “1” voltage (I = 2 mA)		85% V_{DD}	90% V_{DD}		V
t_H	Output hold time			6		ns
t_D	Output delay time			8		ns
	Switching Performance					
F_{SO}	Output Sample Rate		32		48	kHz
f_{CK}	CK frequency (512xF_{SO})		16.384		24.576	MHz
t_{slr}	SCLK falling to LRCK		-15		15	ns
t_{sdv}	SCLK falling to SDATA valid		-15		15	ns
	SCLK Duty Cycle			50		%

Table 2: Electrical specifications

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Unit
	Power Supply					
V_{DD}	Supply Voltage		2.7	3.3	3.6	V
I_{AVDD}	Analog Supply Current	III		16		mA
I_{VDD}	Digital Supply Current	III		12		mA
V_{SS}	Supply Voltage			GND		
AV_{DD}-DV_{DD}	Analog Power - Digital Power Pins		-0.2		+0.2	V
P_D	Power Dissipation	III		92		mW
T	Ambient Operating Temperature		0		70	˚C

Table 2: Electrical specifications

Test Levels

Test Level I: 100% production tested at +25˚C
Test Level II: 100% production tested at +25˚C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterization testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25˚C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages

AVDD ..... - 0.5V to +6V
DVDD1.....- 0.5V to VDD + 0.5V
DVDD2.....- 0.5V to VDD + 0.5V

Input voltages

Analog In ..... - 0.5V to AVDD + 0.5V
Digital In.....- 0.5V to VDD + 0.5V
REFP..... - 0.5V to AVDD + 0.5V
REFN ..... - 0.5V to AVDD + 0.5V
CLOCK.....- 0.5V to VDD + 0.5V

Temperatures

Operating Temperature.....-55 to +95 C
Storage Temperature.....- 65 to +125 C

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
$V_{IP}R$ $V_{IN}R$	Analog input signal (differential), Rch
$V_{IP}L$ $V_{IN}L$	Analog input signal (differential), Lch
$V_{REFP}R$ $V_{REFN}R$	Differential voltage reference pins, Rch
$V_{REFP}L$ $V_{REFN}L$	Differential voltage reference pins, Lch
AVDD	Analog power pins. Should be connected to outside V_{DD}
VDDCO	Digital power supply for digital core. Should be connected to outside VDD
VDD	Digital power supply for pads. Should be connected to outside V_{DD}
VSSCO	GND
VSS	GND
CK	Clock input
RESET	Reset input pin, active high
PWR_SAVE	Power save input, high level will stop clock to digital part
TEST	Connect to outside GND
TEST_LOAD	Connect to outside GND
TEST_Y1, TEST_Y2 TEST_Y3	Connect to outside GND
LRCK, SCLK, SDATA	Digital output pins as described in “Timing Diagram” on page 6.

Table 3: Pin Functions

PIN ASSIGNMENT

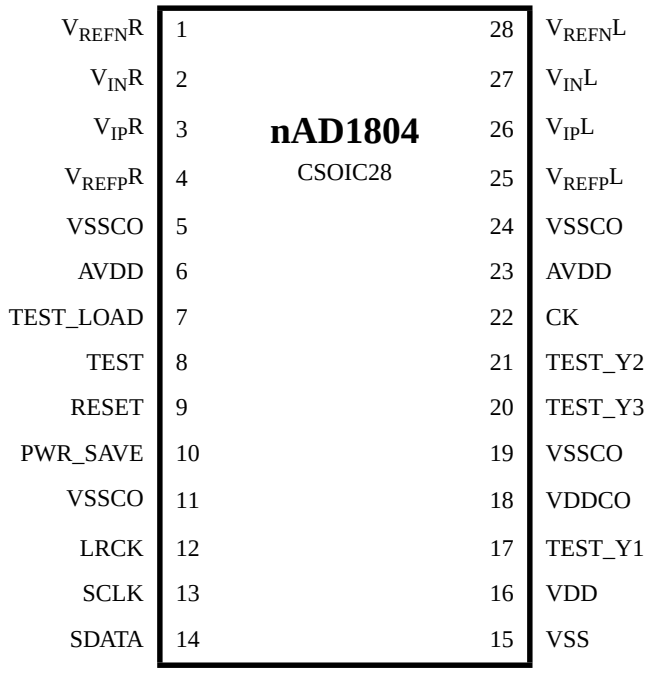

Figure 2: Pin assignment

TIMING DIAGRAM

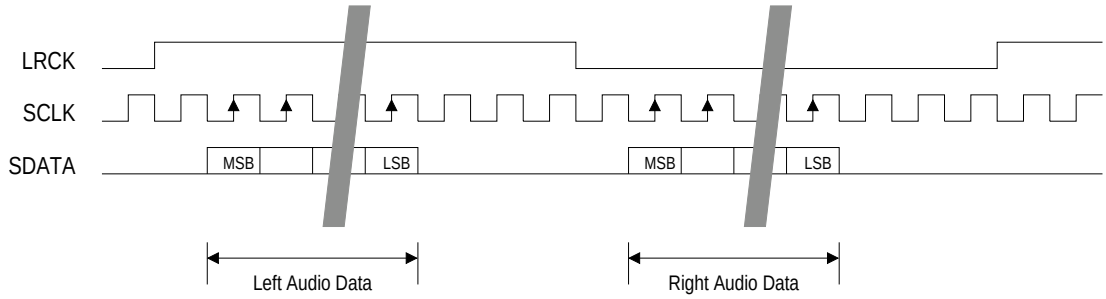

Figure 3: Serial data out interface

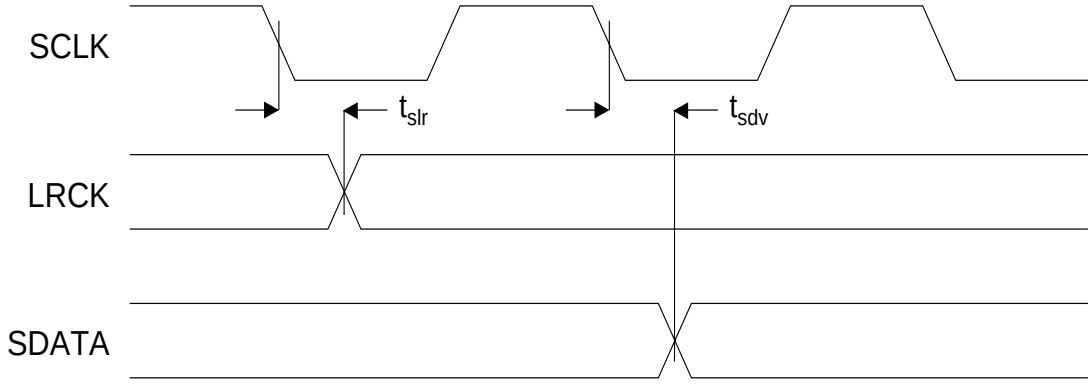

Figure 4: Data output timing

TYPICAL PERFORMANCE CURVES

(TBD)

DEFINITIONS

Data sheet status	
Objective product specification	This data sheet contains target specifications for product development.
Preliminary product specification	This data sheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later
Product specification	This data sheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 4: Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

References

Each channel of the nAD1804 has a differential analog input. The input range for each channel is independently set by the reference pins $V_{IP}R$ ($V_{IP}L$) and $V_{IN}R$ ($V_{IN}L$). The input-range is equal to $V_{IP}R$-$V_{IN}R$ ($V_{IP}L$-$V_{IN}L$). The externally generated reference voltages connected to $V_{IP}R$ and $V_{IN}R$ ($V_{IP}L$ and $V_{IN}L$) should be symmetric around half the supply voltage. See Table 2 on page 3 for valid values for V_{REF} (i.e. the input range).

The references should be decoupled as close to the converter pins as possible using 1µF capacitors in parallel with smaller capacitors (e.g. 220pF).

Clock input (CK)

CK runs the digital filters and it is used to generate the sampling clock to the modulator. The following table shows some common clock frequencies and the corresponding sample rate from the modulator and the output sample rate:

Clock Frequency (f_{CK}) [MHz]	**Modulator Sample Rate (F_{sm}) [MHz]**	**Output Sample Rate (F_{so}) [kHz]**
16.384	1.0240	32
22.5792	1.4112	44.1
24.576	1.536	48

Table 5: Recommended clock frequencies

Serial Data Interface

The serial data interface contains three signals:

- Left/Right Clock: LRCK
- Serial Clock: SCLK
- Serial Data: SDATA

LRCK and SCLK are derived from CK, $f_{LRCK} = f_{CK}/512$ and $f_{SCLK} = f_{CK}/8$. The output sample rate is equal to the frequency of LRCK. Data from the left channel is shifted out when LRCK is high, and data from the right channel is shifted out when LRCK is low. The falling edges of SCLK cause new data bit on SDATA, the data bit is valid on rising edge of SCLK (see Figure 3 on page 6).

DESIGN CENTER

Nordic VLSI ASA
Vestre Rosten 81
N-7075 TILLER
NORWAY
Telephone: +47 72898900
Telefax: +47 72898989

E-mail: For further information regarding datasheets, please send mail to datasheet@nvlsi.no

World Wide Web/Internet: Visit our site at http://www.nvlsi.no

Product specification. Revision Date: June 29, 2000

Datasheet order code: 2000.06.29-nAD1804.