Nordic VLSI ASA

15-Bit Ratio-Metric Delta Sigma Analog-to-Digital Converter

nAD1501

FEATURES

- Single +5 V Power Supply
- Differential Input
- Built-In Decimation filter
- Built-In Ratio-Metric Voltage References
- Switched Capacitor Design
- TBD Core Area
- 0.5µm dual poly CMOS process
- 15 bit Dynamic Range in 300Hz Bandwidth

APPLICATIONS

- Sensors
- Ratio-Metric Measurements
-

GENERAL DESCRIPTION

The nAD1501 is a switched capacitor second order delta sigma analog-to-digital converter, implemented in a 0.5µm CMOS process. The converter needs a minimum of external circuitry due to its internally generated ratio-metric reference voltages (which can be externally decoupled or overridden), and built-in decimation filter. The converter achieves a 15-bit dynamic range in a 300Hz bandwidth. The fully differential implementation ensures low sensitivity to interference from digital circuits on the same chip.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current			1.0		mA
P_D	Power dissipation			5.0		mW
SNR	Signal to noise ratio	0 to 300 Hz		86		dB
SINAD	Signal to noise and distortion ratio	0 to 300 Hz		86		dB
V_{OS}	Offset error				TBD	mV
C_I	Input capacitance			0.5		pF
f_S	Modulator sampling frequency			512		kHz
f_{CK}	Clock frequency [16×f_S]			8.192		MHz
f_{DATA}	Output data rate [f_S/128]			4		kHz
T_{OPER}	Operating temperature range		-40		90	°C

Table 1. Quick reference data

ORDERING INFORMATION

Type number	Name	Description	Version

Table 2. Ordering information

BLOCK DIAGRAM

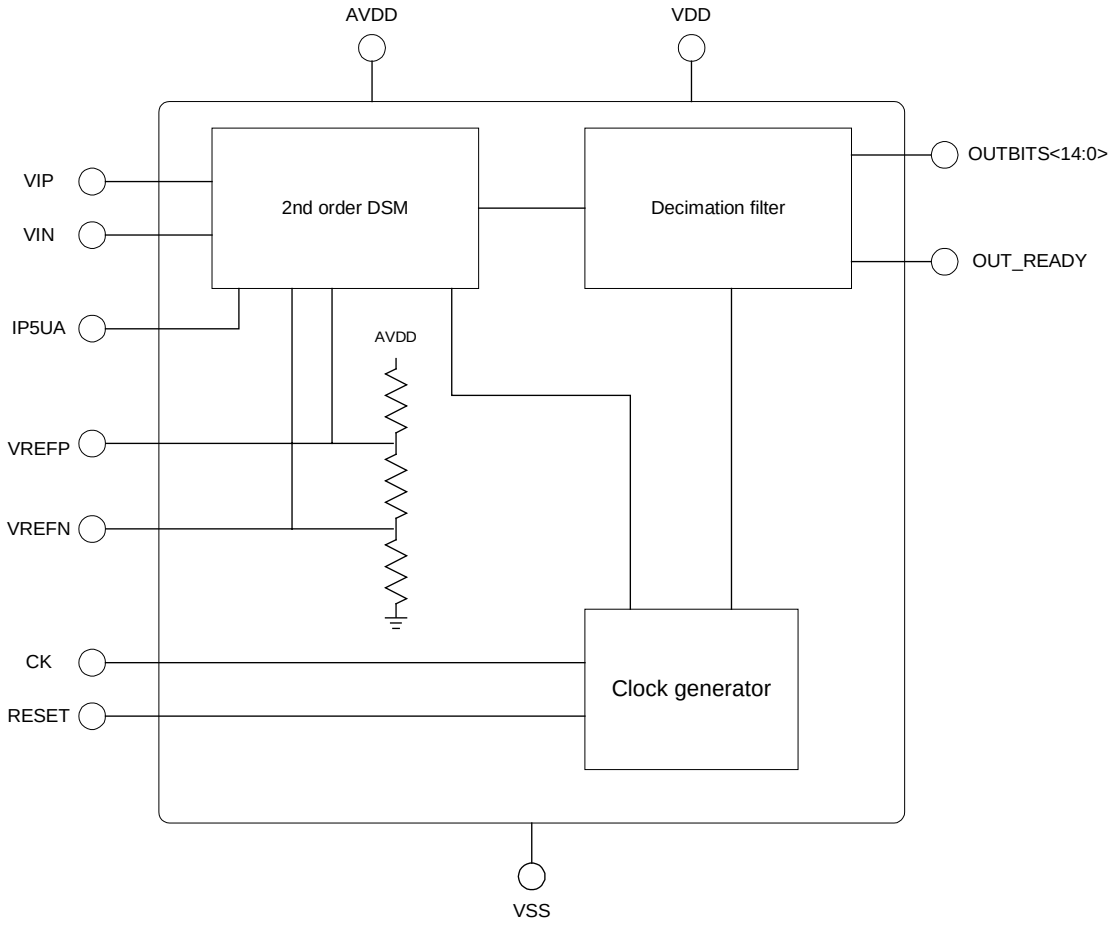

Figure 1. Block diagram

ELECTRICAL SPECIFICATIONS

(V_{DD} = 5.0V, f_{CK} = 8.192MHz, T = 25°C)

Symbol	Parameter (condition)	Test Level	Min.	Typ.	Max.	Units
	DC Accuracy					
V_{OS}	Offset Error				TBD	mV
	Dynamic Performance					
SNR	Signal to Noise Ratio (without harmonics)		86			
	0 to 300 Hz, f_i = 63 Hz					dB
THD	Total Harmonic Distortion					
	0 to 300 Hz, f_i = 63 Hz		-86			dB
SINAD	Signal to Noise and Distortion Ratio					
	0 to 300 Hz, f_i = 63 Hz			86		dB
	Analog Input					
V_{FSR}	Input Voltage Range (Differential)		- 2		+ 2	V
V_{CMI}	Common Mode Input Voltage		1.5	2.5	V_{DD}-1.5 V	V
C_I	Input Capacitance (V_{IP}, V_{IN} to GND)			0.5		pF
	Digital Output					
V_{OL}	Logic “0” voltage				0.4	V
V_{OH}	Logic “1” voltage			90% V_{DD}		
	Power Supply					
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}	Supply Current			1.0		mA
P_D	Power Dissipation			5.0		mW

Table 3. Electrical specifications

Test Levels

Test Level I: 100% production tested at +25°C
Test Level II: 100% production tested at +25°C and sample tested at specified temperatures
Test Level III: Sample tested only
Test Level IV: Parameter is guaranteed by design and characterization testing
Test Level V: Parameter is typical value only
Test Level VI: 100% production tested at +25°C. Guaranteed by design and characterization testing for industrial temperature range

ABSOLUTE MAXIMUM RATINGS

Supply voltages

AV_{DD}..... -0.5V to V_{DD}+0.5V

V_{DD}..... -0.5V to 6.0V

Input voltages

Analog In ..... -0.5V to AV_{DD}+0.5V

Digital In..... -0.5V to V_{DD}+0.5V

Temperatures

Operating Temperature….-40 to +90°C

Storage Temperature .....-60 to +125°C

Note: Stress above one or more of the limiting values may cause permanent damage to the device.

PIN FUNCTIONS

Pin Name	Description
VIP VIN	Differential input signal pins
IP5UA	Bias current for modulator. Should be proportional to absolute temperature (PTAT) with a nominal value 5.0µA
CK	Clock input
RESET	Reset input. Reset of the digital part
OUTBITS<14:0>	Digital output
OUT_READY	Digital data-ready output
VREFP VREFN	Differential in/out pins. May be used to external decouple or override internal generated reference voltages
AVDD	Analog power pin. Should be connected to positive supply
VDD	Digital power pin. Should be connected to positive supply
VSS	Ground

Table 4. Pin functions

PIN ASSIGNMENT

To be included

Figure 2. Pin assignment

TIMING DIAGRAM

To be included

Figure 3. Timing diagram

TYPICAL PERFORMANCE CURVES

To be included

Figure 4. Typical performance curves

PACKAGE OUTLINE

To be included

Figure 5. Package outline

DEFINITIONS

Data sheet status	
Objective product specification	This datasheet contains target specifications for product development.
Preliminary product specification	This datasheet contains preliminary data; supplementary data may be published from Nordic VLSI ASA later.
Product specification	This datasheet contains final product specifications.
Limiting values	
Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Specifications sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

Table 5. Definitions

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Nordic VLSI ASA customers using or selling these products for use in such applications do so at their own risk and agree fully indemnify Nordic VLSI ASA for any damages resulting from such improper use or sale.

APPLICATION INFORMATION

TBD

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