nAD1280-25

12-Bit 80MSPS Sampling Analog-to-Digital Converter

FEATURES

- 2.5V/3.3V power supply
- SINAD typ 67dB (for f_{in} = 50MHz)
- Low power (400mW@2.5V)
- Sample rate: 15-80MSPS
- Frequency dependent biasing
- Internal, wideband T/H
- Differential input
- Low input capacitance

APPLICATIONS

- Imaging
- Test equipment
- Computer scanners
- Communications
- Set top boxes
- Video products

GENERAL DESCRIPTION

The nAD1280-25 is a compact, high-speed, low power 12-bit monolithic analog-to-digital converter, implemented in a 0.25µm double poly CMOS process with poly-poly capacitor option. Refer to the nAD1280-18 objective product specification for a single-poly design. nAD1280-25 has 12-bit resolution with 11.5 effective bits, and close to 15 bit dynamic range for video frequency signals. The converter includes a high bandwidth track and hold. Using internal references, the full scale range is ±1V. The full scale range can be set between ±0.75V and ±1.0V using external references. It operates from a single 2.5V supply, while I/O is biased with 3.3V. Its low distortion and high dynamic range offers the performance needed for demanding imaging, multimedia, telecommunications and instrumentation applications. The bias current level for the ADC is automatically adjusted based on the clock input frequency. Hence, the power dissipation of the device is continuously minimised for the current operating frequency. The nAD1280-25 has a pipelined architecture - resulting in low input capacitance. Digital error correction of the 10 most significant bits ensures good linearity for input frequencies approaching Nyquist. The excellent linearity makes the converter ideally suited for IF sampling. It is also well suited for demanding ultrasonic imaging and flow measurements. The nAD1280-25 is compact. The core occupies less than 3mm^2 of die area in a standard double poly 0.25µm CMOS process. The fully differential architecture makes it insensitive to substrate noise. Thus it is ideal as a mixed signal ASIC macro cell.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	supply voltage		2.25	2.5	2.75	V
I_{DD}	supply current			160		mA
P_D	power dissipation (80 MSPS)	Except digital output drivers		400		mW
P_D	power dissipation (15 MSPS)	Except digital output drivers		90		mW
DNL	differential nonlinearity	f_{IN}=0.9991MHz		±0.5		LSB
INL	integral nonlinearity	f_{IN}=0.9991MHz		±1.0		LSB
f_S	max conversion rate		15		80	MHz
N	resolution				12	bit

Table 1. Quick reference data

nAD1280-25 - ELECTRICAL SPECIFICATIONS

(At T_A = 25°C, V_{DD} = 2.5V, Sampling Rate = 80MHz, Input frequency = 15MHz, Differential input signal, differential sine wave clock unless otherwise noted)

Symbol	Parameter (condition)	Testlev.	Min.	Typ.	Max.	Units
	DC Accuracy					
DNL	Differential Nonlinearity					
	f_{IN} = 0.9991 MHz	I		±0.5		LSB
INL	Integral Nonlinearity					
	f_{IN} = 0.9991 MHz	I		±1.0		LSB
V_{OS}	Midscale offset	I		± 1		%FS
CMRR	Common Mode Rejection Ratio	V		TBD		
ε_G	Gain Error	I		+/-2	+/-5	%
	Dynamic Performance					
SINAD	Signal to Noise and Distortion Ratio					
	f_{IN} = 10 MHz	I		68		dB
	f_{IN} = 50 MHz	I		67		dB
SNR	Signal to Noise Ratio (without harmonics)					dB
	f_{IN} = 10 MHz	I		70		dB
	f_{IN} = 50 MHz	I		69		dB
SFDR	Spurious Free Dynamic Range					
	f_{IN} = 10 MHz	I		95		dB
	f_{IN} = 50 MHz	I		90		dB
DP	Differential Phase	V		TBD		
DG	Differential Gain	V		TBD		
PSRR	Power Supply Rejection Ratio	V		TBD		
	Analog Input					
V_{FSR}	Input Voltage Range (differential)	V		±1		V
V_{CMI}	Common mode input voltage	V		1.65		V
C_{INA}	Input Capacitance (from each input to ground)	V		8		pF
	Reference Voltages					
V_{REFNI}	Internal reference voltage on pin 10		0.70	0.75	0.80	V
V_{REFPI}	Internal reference voltage on pin 11		1.70	1.75	1.80	V
	Internal reference voltage drift				100	ppm/°C
V_{REFP}-V_{REFN}	Reference input voltage range	V	0.75	1.0	TBD	V
V_{CM}	Common mode output voltage	VI	TBD	1.25	TBD	V
	Clock Input (see application information)					
V_{CLKP} - V_{CLKN}	Differential clock input voltage (peak to peak)			0.8		V
	Single ended clock input					
	Clock logic “0” voltage (I = 2 mA)	VI		0	0.4	V
	Clock logic “1” voltage (I = 2 mA)	VI	3.0	3.3	3.6	V
	Switching Performance					
f_S	Conversion Rate	VI	15		80	MSPS
	Pipeline Delay	IV		2.5		Clocks
σ_{AP}	Aperture jitter	V		TBD		Ps
t_{AP}	Aperture delay	V		TBD		Ns
	Power Supply					
V_{DD}	supply voltage	V	2.25	2.5	2.75	V
I_{DD}	supply current (except digital output)	VI		160		mA
V_{SS}	supply voltage			GND		
$AV_{DD}DV_{DD1}$	analog power – digital power pins		-0.2		+0.2	V
OV_{DD}	Output driver supply voltage		3.0	3.3	3.6	V
T	Ambient operating temperature		-40		+85	°C