New

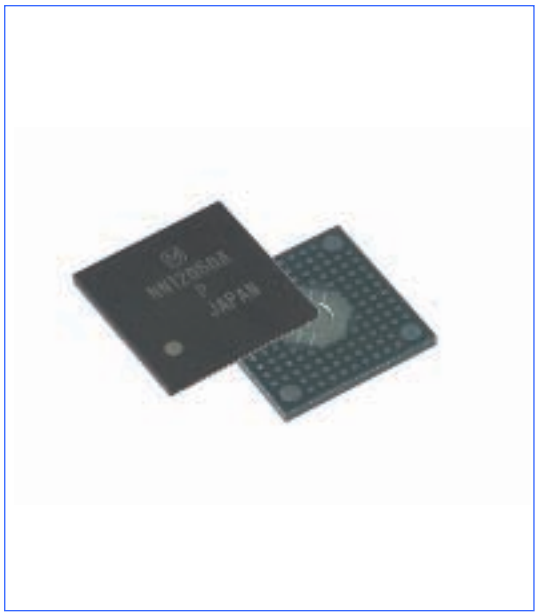
Panasonic

CCD peripheral circuits in a single package

Analog Front-End IC for CCD Camera
NN12060A/61A

■ Overview

NN12060A/61A are ICs that incorporate a Panasonic CCD-compatible timing generator and vertical driver into the analog front-end processing sections (correlated double sampler (CDS), gain control amplifier (GCA) and A/D converter) for CCD cameras. Built-in dedicated timing generator and vertical driver help to reduce CCD camera design time and save space.



■ Features

- ●Broad input dynamic range: 1.2V
- ●Wide gain range fir GCA:-2dB to 34dB
- ●3dB higher S/N ratio than conventional model
- ●Horizontal driver provided
- ●Flash sync pulse output provided
- ●Built-in electronic zoom and electronic shutter function
- ●Built-in 8-channel vertical driver and 1-channel SUB driver
- ●Small LLGA package

■ Applications

CCD cameras (Digital still cameras, cellular phone cameras, etc.)

■ Specification

	NN12060A	NN12061A
Power supply voltage	CDS+GCA+AD/TG:2.7V to 3.6V Vdr VL:-8.5V to -4.0V VDC :2.7V to 5.5V VHH, VH:11.5V to 15.5V	
A/D converter resolution	10-bit	12-bit
Max. conversion frequency	27MHz	
Compatible CCDs:	1/2.7” 3,340,000 pixel:MN39480/85 1/2.5” 4,200,000 pixel:MN39482 1/1.76” 5,360,000 pixel:MN39593	
Package	107-pin LLGA (9mm×9mm)	

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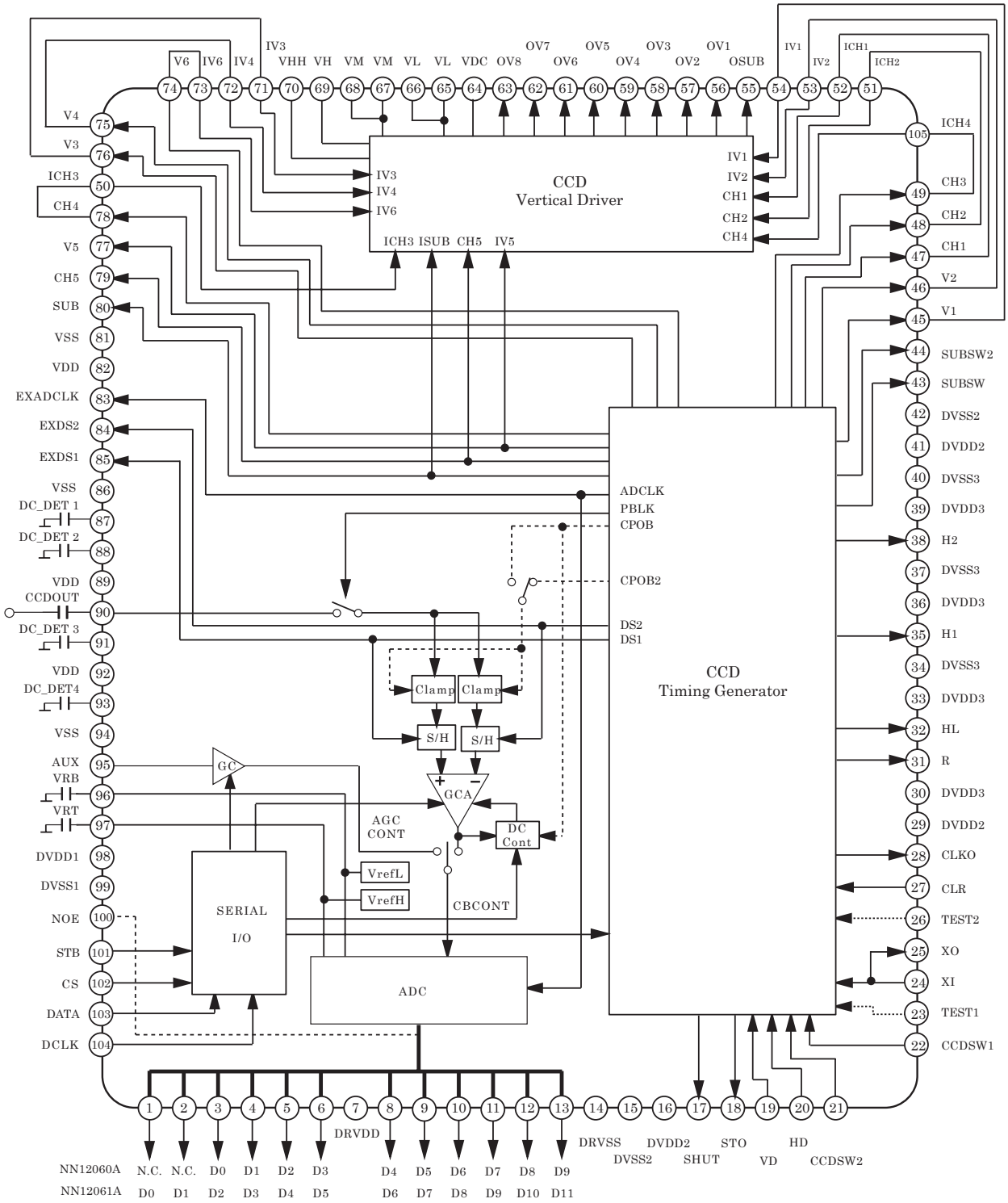
■ Block Diagram



■ Pin arrangement（TOP VIEW）

Package: MLGA107-L-0909

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N
13	22		19	52	54	13	64	66	8	5	2	57	
12			20	18	16	14	11	68	7	4	56		
11	71	23	21	17	15	12	10	9	6	3	1	104	103
10	25	24	51	☒	☒				☒	☒	101	102	58
9	28	27	26	☒						☒	98	100	99
8	53	29	50								59	97	60
7	31	32	30								95	96	62
6	33	34	72								93	94	63
5	73	35	N.C.	☒						☒	90	91	92
4	37	38	36	☒	☒				☒	☒	88	89	61
3	39	40	N.C.	78	44	69	49	47	46	82	86	55	87
2	77		105	41	43	74	75	45	81	83	85	67	
1				79	80	42	76	48	70	65	84		

TOP VIEW

	A	B	C	D	E	F	G	H	J	K	L	M	N
13	CCDSW1		VD	ICH1	IV1	D9/D11	VDC	VL	D4/D6	D2/D4	N.C./D1	OV2	
12			HD	STO	DVDD2	DRVSS	D7/D9	VM	DRVDD	D1/D3	OV1		
11	IV3	TEST1	CCDSW2	SHUT	DVSS2	D8/D10	D6/D8	D5/D7	D3/D5	D0/D2	N.C./D0	DCLK	DATA
10	XO	XI	ICH2	☒	☒				☒	☒	STB	CS	OV3
9	CLKO	CLR	TEST2	☒						☒	DVDD1	NOE	DVSS1
8	IV2	DVDD2	ICH3								OV4	VRT	OV5
7	R	HL	DVDD3								AUX	VRB	OV7
6	DVDD3	DVSS3	IV4								DC_DET4	VSS	OV8
5	IV6	H1	N.C.	☒						☒	CCDOUT	DC_DET3	VDD
4	DVSS3	H2	DVDD3	☒	☒				☒	☒	DC_DET2	VDD	OV6
3	DVDD3	DVSS3	N.C.	CH4	SUBSW2	VH	CH3	CH1	V2	VDD	VSS	OSUB	DC_DET1
2	V5		ICH4	DVDD2	SUBSW	V6	V4	V1	VSS	EXADCLK	EXDS1	VM	
1				CH5	SUB	DVSS2	V3	CH2	VHH	VL	EXDS2		

☒ Thermal / dummy land　　□ No land　　N.C. Land without wire connection

■ Pin description

	No	Terminal name	PIN	I/O	Description	Note
*	1	N.C./D0	L11	-/O	N.C./AD output (LSB)	MOT1FY 1mA
*	2	N.C./D1	L13	-/O	N.C./AD output	MOT1FY 1mA
*	3	D0/D2	K11	O	AD output (LSB)/AD output	MOT1FY 1mA
*	4	D1/D3	K12	O	AD output	MOT1FY 1mA
*	5	D2/D4	K13	O	AD output	MOT1FY 1mA
*	6	D3/D5	J11	O	AD output	MOT1FY 1mA
	7	DRVDD	J12	-	Digital output power supply for signal processing block	MVDD1Y
*	8	D4/D6	J13	O	AD output	MOT1FY 1mA
*	9	D5/D7	H11	O	AD output	MOT1FY 1mA
*	10	D6/D8	G11	O	AD output	MOT1FY 1mA
*	11	D7/D9	G12	O	AD output	MOT1FY 1mA
*	12	D8/D10	F11	O	AD output	MOT1FY 1mA
*	13	D9/D11	F13	O	AD output (MSB)	MOT1FY 1mA
	14	DRVSS	F12	-	Digital output ground for signal processing block	MVSS1Y
	15	DVSS2	E11	-	Ground for timing generator block	MVSS1Y
	16	DVDD2	E12	-	Power supply for timing generator block	MVDD1Y
	17	SHUT	D11	O	Mechanical shutter control pulse	MOP8SY 7.2 mA
	18	STO	D12	O	Strobe trigger output	MOP2FY 1.8 mA
	19	VD	C13	I	Vertical sync pulse input	MISCY Schmidt
	20	HD	C12	I	Horizontal synchronization pulse input	MISCY Schmidt
	21	CCDSW2	C11	I	CCD setting input 2	MBD1Y Pull-down with resistor
	22	CCDSW1	A13	I	CCD setting input 1	MBD1Y Pull-down with resistor
	23	TEST1	B11	I	Test input 1(Normal:L)	MBD1Y Pull-down with resistor
	24	XI	B10	I	Crystal oscillator input(2FCK=49.09/54.0 MHz)	MXIY
	25	XO	A10	O	Crystal oscillator output (2FCK) with 3 times multiplier and external feedback resistor	MOSC90DY
	26	TEST2	C9	I	Test input 2 (Normally set low)	MBD1Y Pull-down with resistor
	27	CLR	B9	I	All clear input	MBU1Y Pull-up with resistor
	28	CLKO	A9	O	CLKO(FCK) clock output(24.5454/27.0MHz)	MOT4FY 3.6 mA
	29	DVDD2	B8	-	Power supply for timing generator block	MVDD1Y

NN12060A and NN12061A terminal names are also put down with pins marked *.

■ Pin description 2

No	Terminal name	PIN	I/O	Description	Note
30	DVDD3	C7	-	ΦH and ΦR power supply for	MVDDIOXY
31	R	A7	O	ϕR pulse output (positive logic)	KNOT8FY 7.2 mA
32	HL	B7	O	ϕHL transfer pulse output (positive logic)	KNOT8FY x3 7.2 mA*
33	DVDD3	A6	-	ΦH and ΦR power supply	MVDDIOXY
34	DVSS3	B6	-	ΦH and ΦR ground	MVSS1Y
35	H1	B5	O	ϕH1 transfer pulse output (positive logic)	KNOT8FY x3 14.4 mA*
36	DVDD3	C4	-	ΦH and ΦR power supply for	MVDDIOXY
37	DVSS3	A4	-	ΦH and ΦR ground	MVSS1Y
38	H2	B4	O	ϕH2 transfer pulse output (positive logic)	KNOT8FY x3 14.4 mA*
39	DVDD3	A3	-	ΦH and ΦR power supply	MVDDIOXY
40	DVSS3	B3	-	ΦH and ΦR ground	MVSS1Y
41	DVDD2	D2	-	ΦH and ΦR power supply	MVDDIOXY
42	DVSS2	F1	-	ΦH and ΦR ground	MVSS1Y
43	SUBSW	E2	O	SUB bias voltage setting selection output1	MOP2FY 1.8 mA
44	SUBSW2	E3	O	SUB bias voltage setting selection output2	MOP2FY 1.8 mA
45	V1	H2	O	ϕV1 transfer pulse output	MOP2FY 1.8 mA
46	V2	J3	O	ϕV2 transfer pulse output	MOP2FY 1.8 mA
47	CH1	H3	O	ϕV1PD charge read pulse output	MZ2FY 1.8 mA
48	CH2	H1	O	ϕV3PD charge read pulse output	MOP2FY 1.8 mA
49	CH3	G3	O	ϕV5PD charge read pulse output	MOP2FY 1.8 mA
50	ICH3	C8	I	(V Driver) ϕV7PD charge read pulse input	
51	ICH2	C10	I	(V Driver) ϕV3PD charge read pulse input	
52	ICH1	D13	I	(V Driver) ϕV1PD charge readt pulse input	
53	IV2	A8	I	(V Driver) ϕV2 transfer pulse input	
54	IV1	E13	I	(V Driver) ϕV1 transfer pulse input	
55	OSUB	M3	O	(V Driver) PD charge PCB discharge pulse output	
56	OV1	L12	O	(V Driver) ϕV1 transfer pulse output (binary :VH,VM,VL)	
57	OV2	M13	O	(V Driver) ϕV2 transfer pulse output (binary :VM,VL)	
58	OV3	N10	O	(V Driver) ϕV3 transfer pulse output (3値:VH,VM,VL)	ϕV3B (MN39480/MN39482)

・Drive ability setting is required by Serial setting.

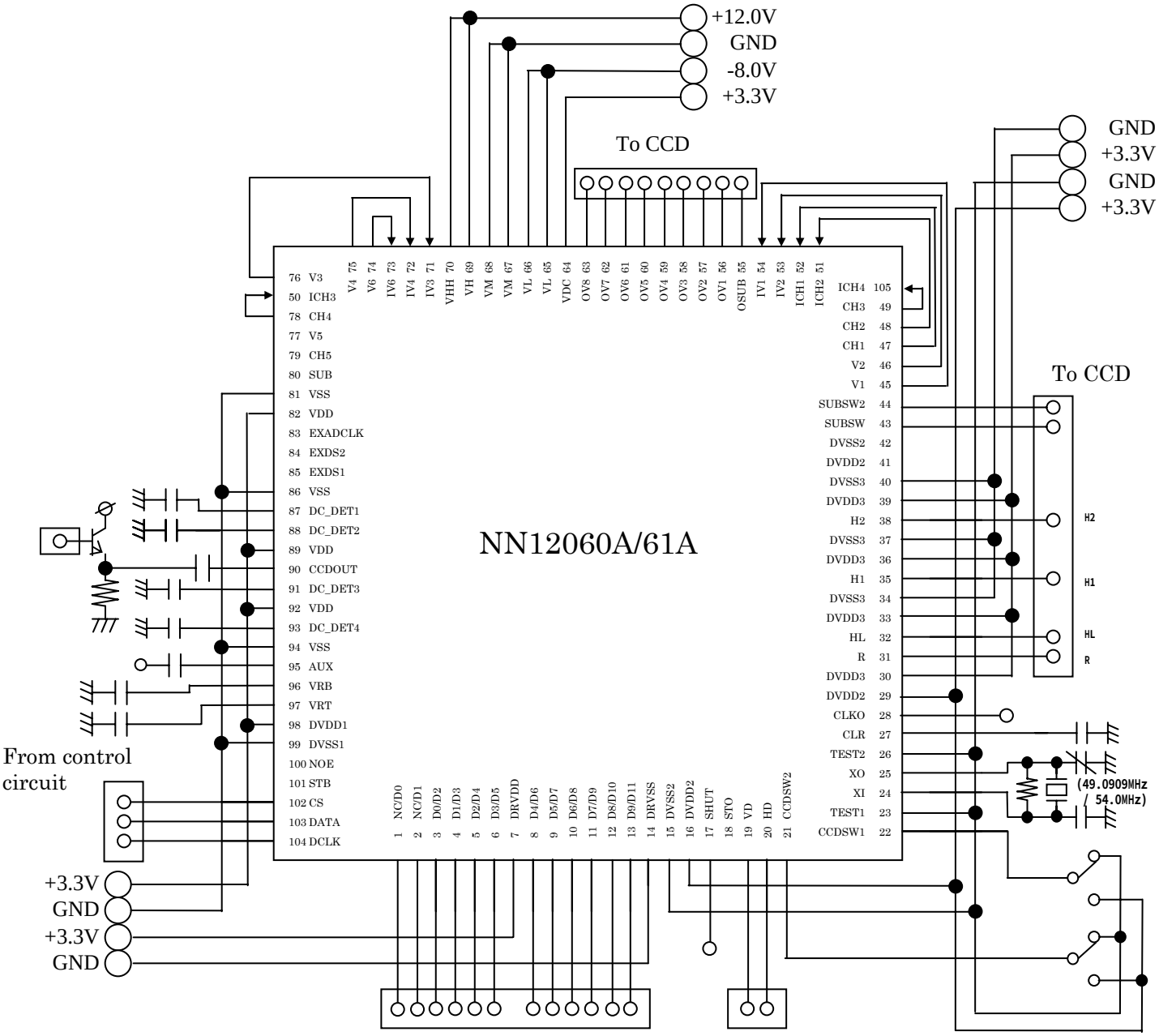
■ Pin description 3

No	Terminal name	PIN	I/O	Description	Note
59	OV4	L8	O	(V Driver) ϕV4 transfer pulse output (binary:VM,VL)	
60	OV5	N8	O	(V Driver) ϕV7 transfer pulse output (value:VH,VM,VL)	ϕV3A (MN39480/MN39482)
61	OV6	N4	O	(V Driver) ϕV6transfer pulse output (binary:VM,VL)	
62	OV7	N7	O	(V Driver) ϕV5transfer pulse output (value: VH,VM,VL)	ϕV5B (MN39480/MN39482)
63	OV8	N6	O	(V Driver) ϕV8 transfer pulse output (value:VH,VM,VL)	ϕV5A (MN39480/MN39482)
64	VDC	G13	-	(V Driver) Input block High-level power supply	
65	VL	K1	-	(V Driver) Low-level power supply	
66	VL	H13	-	(V Driver) Low-level power supply	
67	VM	M2	-	(V Driver) Middle-level power supply	
68	VM	H12	-	(V Driver) Middle-level power supply	
69	VH	F3	-	(V Driver) vertical drive HI-level power supply	
70	VHH	J1	-	(V Driver) SUB-Driver block Hi-level power supply	
71	IV3	A11	I	(V Driver) ϕV3 transfer pulse input	
72	IV4	C6	I	(V Driver) ϕV4 transfer pulse input	
73	IV6	A5	I	(V Driver) ϕV6 transfer pulse input	
74	V6	F2	O	ϕV6 transfer pulse output	MOP2FY 1.8 mA
75	V4	G2	O	ϕV4 transfer pulse output	MOP2FY 1.8 mA
76	V3	G1	O	ϕV3 transfer pulse output	MOP2FY 1.8 mA
77	V5	A1	O	ϕV5 transfer pulse output	MOP2FY 1.8 mA
78	CH4	D3	O	ϕV7P Charge read pulse output	MOP2FY 1.8 mA
79	CH5	D1	O	ϕV8PD Charge read pulse output	MOP2FY 1.8 mA
80	SUB	E1	O	PD charge PCB discharge pulse output	MZ2FY 1.8 mA
81	VSS	J2	-	Analog ground for signal processing block	MVSS1Y

■ Pin Descriptions 4

No	端子名	PIN	I/O	Description	Note
82	VDD	K3	-	Analog power supply for signal processing block	MVDD1Y
83	EXADCLK	K2	O	A/D Clock output （24.5454/27.0MHz）	MOT4FY 3.6 mA
84	EXDS2	L1	O	Data S/H pulse output （fixed negative logic）	MZ4FD2Y Pull-down with resistor 3.6mA
85	EXDS1	L2	O	Pre-charge S/H pulse output（ fixed negative logic）	MZ4FD2Y Pull-down with resistor 3.6mA
86	VSS	L3	-	Analog ground for signal processing block	MANVSSY
87	DC_DET1	N3	-	CDS output DC level stabilization	MAINY
88	DC_DET2	L4	-	GCA output DC level stabilization	MAINY
89	VDD	M4	-	Analog power supply for signal processing block	
90	CCDOUT	L5	-	CDS output signal input	MAINY
91	DC_DET3	M5	-	Bias stabilization	MAINY
92	VDD	N5	-	Analog power supply for signal processing block	MANVDDY
93	DC_DET4	L6	-	Bias stabilization 2	MAINY
94	VSS	M6	-	Analog ground for signal processing	MANVSSY
95	AUX	L7	-	Externally input signal input	MAINY
96	VRB	M7	-	VRB	MAINY
97	VRT	M8	-	VRT	MAINY
98	DVDD1	L9	-	Analog power supply for signal processing block	MANVDDY
99	DVSS1	N9	-	Analog ground for signal processing block	MANVSSY
100	NOE	M9	I	NOE input terminal	MBCY
101	STB	L10	I	STB input terminal	MBCY
102	CS	M10	I	Data latch input for serial communications	MISCY Schmidt
103	DATA	N11	I	Data input for serial communications	MISCY Schmidt
104	DCLK	M11	I	Clock input for serial communication	MISCY Schmidt
105	ICH4	C2	I	(V Driver) ϕV5PD charge read pulse input	

■ Application circuit



・Please refer to CCD instruction manual for CCD connection.
・ϕ R and ϕH power supply
V ϕ Hh(min)+0.05 V < DVDD3 ≦ 3.6 V
V ϕ Hh(min) is the smallest high-level value for ϕ H operation under the condition of CCD standards.

Note: The supply voltage must satisfy the condition DVDD2 ≦ DVDD3.
The DVDD1, DRVDD, and VDD supply voltage must be the same in voltage level as DVDD2 supply voltage. There is no particular input order of each power supply , but is is recommended to input them at the same time.
・Be sure to connect an external feedback resistor to the oscillator circuit. If an external clock signal is input, make sure that the clock with a duty ration of 1 to 1 is input the XI pin.
・If AUX input is not used in the application, the external capacitor at pin 95 is not necessary. Tie pin 95 to ground in that case.