RF MICRO·DEVICES

NDA-410-D

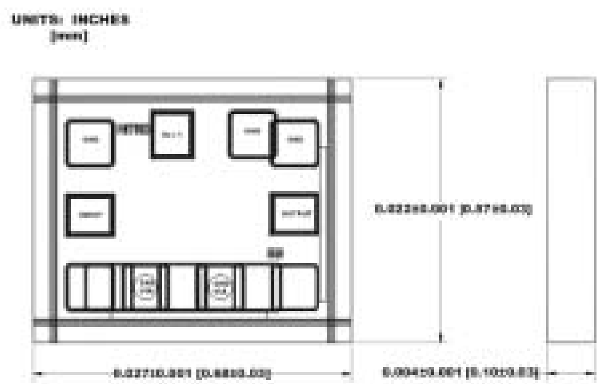
GaInP/GaAs HBT MMIC DISTRIBUTED AMPLIFIER DC TO 11GHz

Typical Applications

- Narrow and Broadband Commercial and Military Radio Designs
- Linear and Saturated Amplifiers
- Gain Stage or Driver Amplifiers for MW Radio/Optical Designs

Product Description

The NDA-410-D GaInP/GaAs HBT MMIC distributed amplifier is a low-cost, high-performance solution for high frequency RF, microwave, or optical amplification needs. This 50Ω matched distributed amplifier is based on a reliable HBT proprietary MMIC design, providing unsurpassed performance for small-signal applications. Designed with an external bias resistor, the NDA-410-D provides flexibility and stability. In addition, the NDA-410-D chip was designed with an additional ground via to enable low junction temperature operation. NDA-series of distributed amplifiers provide design flexibility by incorporating AGC functionality into their designs.



Package Style: Die

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS
- ☑ GaInP/HBT
- ☐ GaN HEMT

Features

- Reliable, Low-Cost HBT Design
- 12.0dB Gain, +15.5dBm P1dB@2GHz
- High P1dB of +14.8dBm@6.0GHz and +13.5dBm@11.0GHz
- Fixed Gain or AGC Operation
- 50Ω I/O Matched for High Freq. Use

Functional Block Diagram

Ordering Information

NDA-410-D	GaInP/GaAs HBT MMIC Distributed Amplifier DC to 11GHz - Die Only

RF Micro Devices, Inc.
7628 Thorndike Road
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Absolute Maximum Ratings

Parameter	Rating	Unit
RF Input Power	+15	dBm
Power Dissipation	300	mW
Device Current, I_{CC1}	42	mA
Device Current, I_{CC2}	42	mA
Junction Temperature, Tj	200	°C
Operating Temperature	-45 to +85	°C
Storage Temperature	-65 to +150	°C

Exceeding any one or a combination of these limits may cause permanent damage.

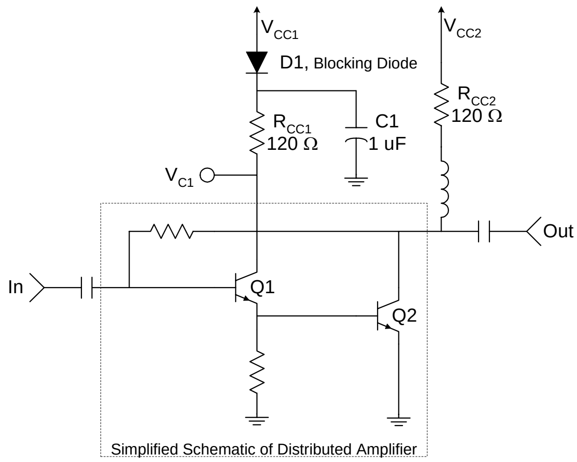
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					V_{CC1}=+10V, V_{CC2}=+10V, V_{C1}=+4.7V, V_{C2}=+2.98V, I_{CC1}=29mA, I_{CC2}=36mA, Z_0=50Ω, T_A=+25°C
Small Signal Power Gain, S21	12.0	13.0		dB	f=0.1GHz to 4.0GHz
		13.0		dB	f=4.0GHz to 6.0GHz
		13.0		dB	f=6.0GHz to 8.0GHz
	9.0	10.0		dB	f=8.0GHz to 11.0GHz
Input and Output VSWR		1.35:1			f=0.1GHz to 4.0GHz
		2.3:1			f=4.0GHz to 8.0GHz
		3.50:1			f=8.0GHz to 11.0GHz
Bandwidth, BW		11.0		GHz	BW3 (3dB)
Output Power @ 1dB Compression		15.5		dBm	f=2.0GHz
		14.8		dBm	f=6.0GHz
		13.5		dBm	f=11.0GHz
Noise Figure, NF		5.0		dB	f=2.0GHz
Third Order Intercept, IP3		+25.5		dBm	f=2.0GHz
Reverse Isolation, S12		-16.0		dB	f=0.1GHz to 11.0GHz
Output Device Voltage, V_{C2}	2.70	2.98	3.20	V	
AGC Control Voltage, V_{C1}		4.7		V	
Gain Temperature Coefficient, $\delta G_T/\delta T$		-0.0015		dB/°C	
MTTF versus Junction Temperature					
Case Temperature		85		°C	
Junction Temperature		144		°C	
MTTF		>1,000,000		hours	
Thermal Resistance					
θ_{JC}		242		°C/W	Thermal Resistance, at any temperature (in °C/Watt) can be estimated by the following equation: θ_{JC} (°C/Watt)=242[T_J(°C)/144]

Suggested Voltage Supply: $V_{CC1}\geq$4.7V, $V_{CC2}\geq$5.0V

Typical Bias Configuration

Application notes related to biasing circuit, device footprint, and thermal considerations are available on request.



Bias Resistor Selection
R_{CC1}: For 4.7V<V_{CC1}<5.0V R_{CC1}=0Ω For 5.0V<V_{CC1}<10.0V R_{CC1}=V_{CC1}-4.7/0.029Ω
R_{CC2}: For 5.0V<V_{CC2}<10.0V R_{CC1}=V_{CC2}-2.98/0.036Ω

Typical Bias Parameters for V_{CC1}=V_{CC2}=10V:

V_{CC1} (V)	V_{CC2} (V)	I_{CC1} (mA)	V_{C1} (V)	R_{CC1} (Ω)	I_{CC2} (mA)	V_{C2} (V)	R_{CC2} (Ω)
10	10	29	4.75	180	36	2.98	195

Application Notes

Die Attach

The die attach process mechanically attaches the die to the circuit substrate. In addition, it electrically connects the ground to the trace on which the chip is mounted, and establishes the thermal path by which heat can leave the chip.

Wire Bonding

Electrical connections to the chip are made through wire bonds. Either wedge or ball bonding methods are acceptable practices for wire bonding.

Assembly Procedure

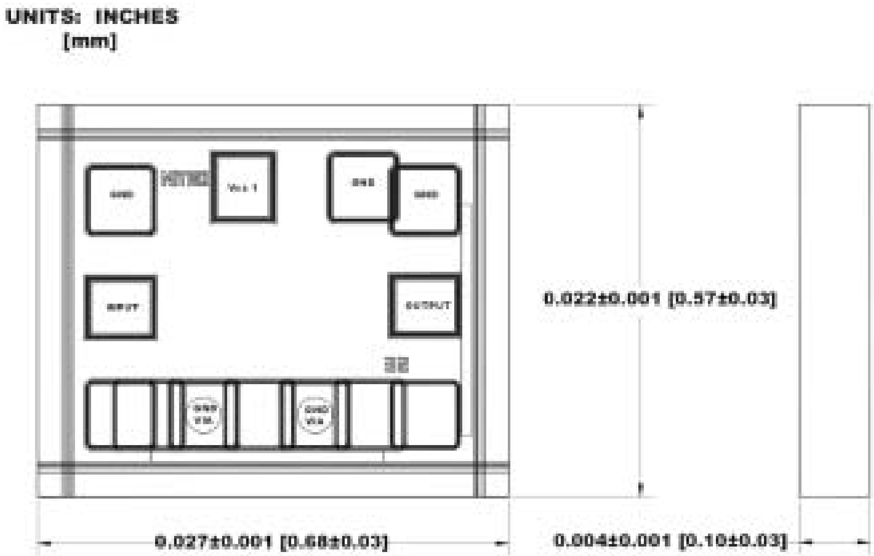
Epoxy or eutectic die attach are both acceptable attachment methods. Top and bottom metallization are gold. Conductive silver-filled epoxies are recommended. This procedure involves the use of epoxy to form a joint between the backside gold of the chip and the metallized area of the substrate. A 150°C cure for 1 hour is necessary. Recommended epoxy is Ablebond 84-1LMI from Ablestik.

Bonding Temperature (Wedge or Ball)

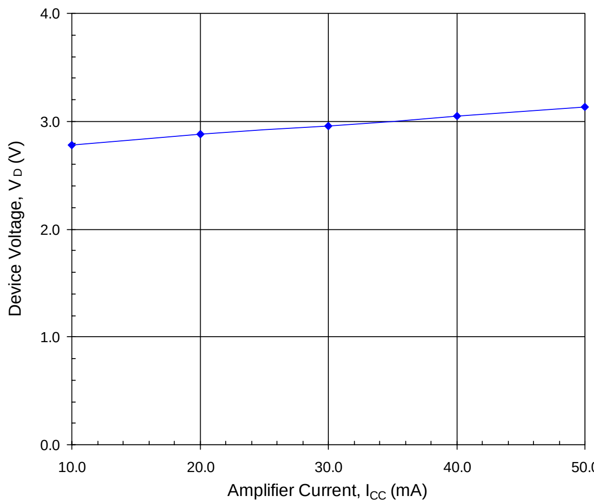
It is recommended that the heater block temperature be set to 160°C±10°C.

Chip Outline Drawing - NDA-410-D

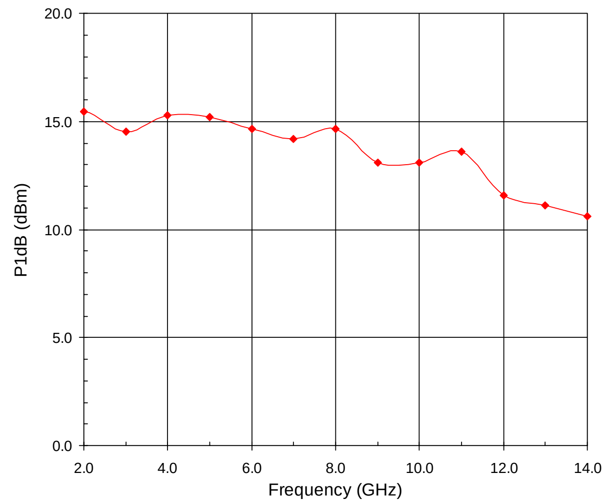
Chip Dimensions: 0.027” x 0.022” x 0.004”



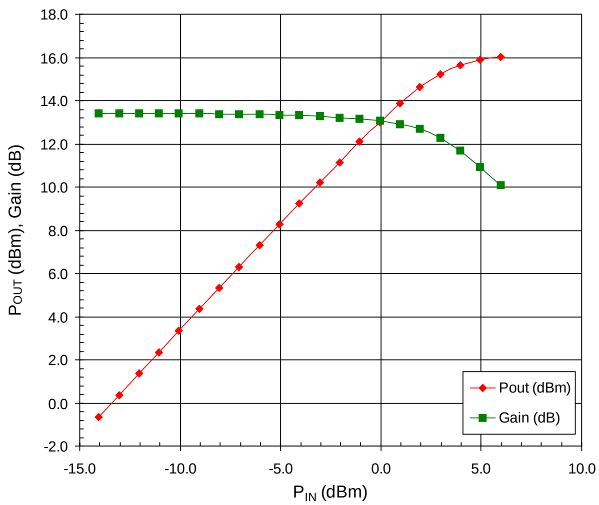
Device Voltage versus Amplifier Current



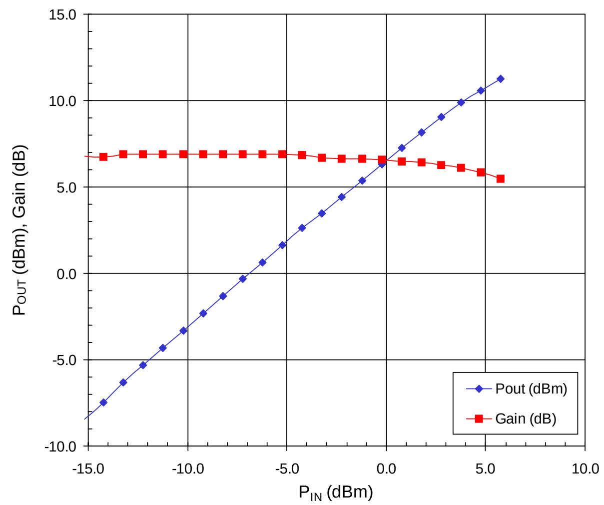
P1dB versus Frequency at 25°C



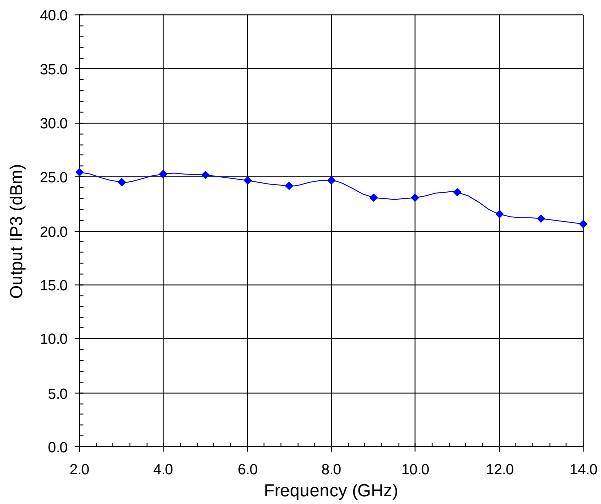
P_{OUT}/Gain versus P_{IN} at 6 GHz



P_{OUT}/Gain versus P_{IN} at 14 GHz



Third Order Intercept versus Frequency at 25°C

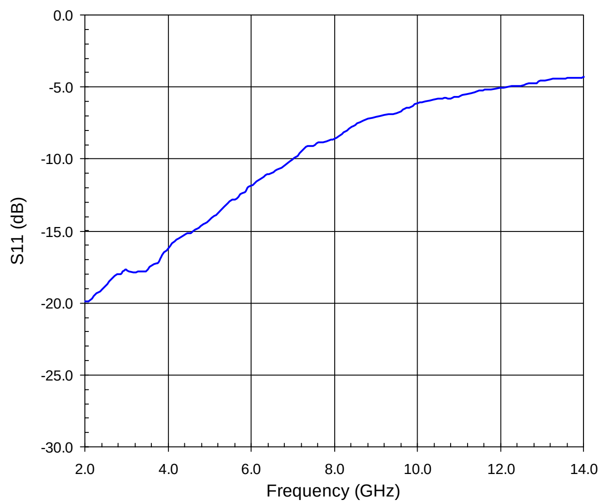


NDA-410-D

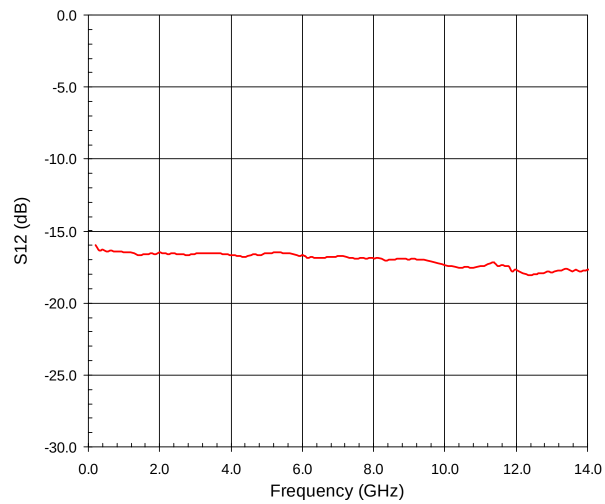
Note: The s-parameter gain results shown below include device performance as well as evaluation board and connector loss variations. The insertion losses of the evaluation board and connectors are as follows:

1GHz to 4GHz=-0.06dB
5GHz to 9GHz=-0.22dB
10GHz to 14GHz=-0.50dB
15GHz to 20GHz=-1.08dB

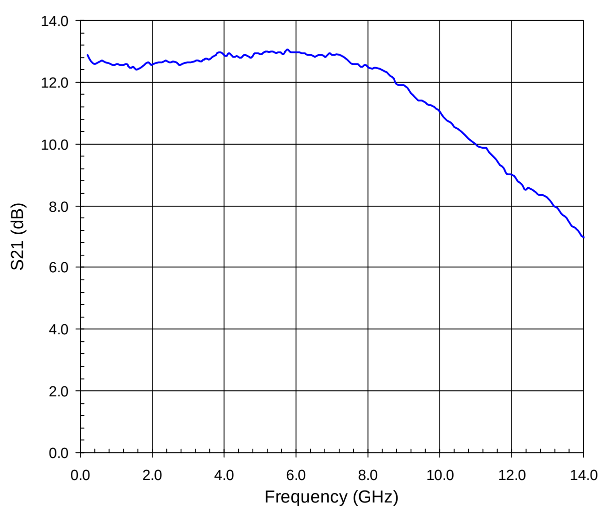
S11 versus Frequency



S12 versus Frequency



S21 versus Frequency



S22 versus Frequency