Low-power Multi-rate (OC-48/12/3/GbE/FEC) SONET/SDH Transceiver

NLD0442 **PRELIMINARY**

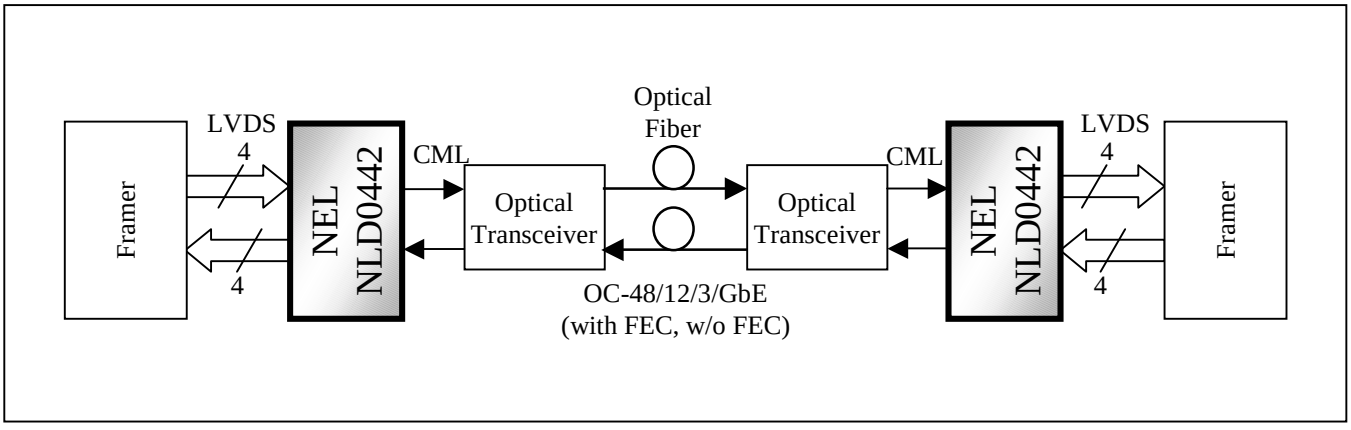
<General Description>

The NLD0442 is a low-power multi-rate transceiver LSI for SONET/SDH-based optical communication systems and Gigabit Ethernet systems.

<Features>

- Fully integrated transceiver LSI with clock and data recovery (CDR), 1:4 demultiplexer (DEMUX), 4:1 multiplexer (MUX), and clock multiplication unit (CMU),
- Applicable for SONET/SDH-based optical communication systems (OC-48/STM-16, OC-12/STM-4, OC-3/STM-1) and Gigabit Ethernet Systems,
- Supports RS(255,239) forward error correction (FEC) data rate of 2.666 Gb/s,
- Complies with Bellcore and ITU-T jitter specifications (jitter tolerance, jitter transfer, and jitter generation),
- Selectable reference-clock mode: no reference clock or 155/622 MHz reference clock,
- Low jitter generation (< 0.005 UIrms),
- System and Line loopback modes,
- Loss of signal (LOS) detect input and loss of lock (LOL) detect output,
- FIFO reset input and FIFO error output,
- Serial 2.5-Gb/s CML and 4-bit 622-Mb/s LVDS interfaces with on-chip termination,
- Low power consumption of 1 W,
- Single +3.3 V power supply,
- CMOS/SOI technology,
- 100-pin plastic TQFP package.

<Application Block Diagram>



< Block Diagram >

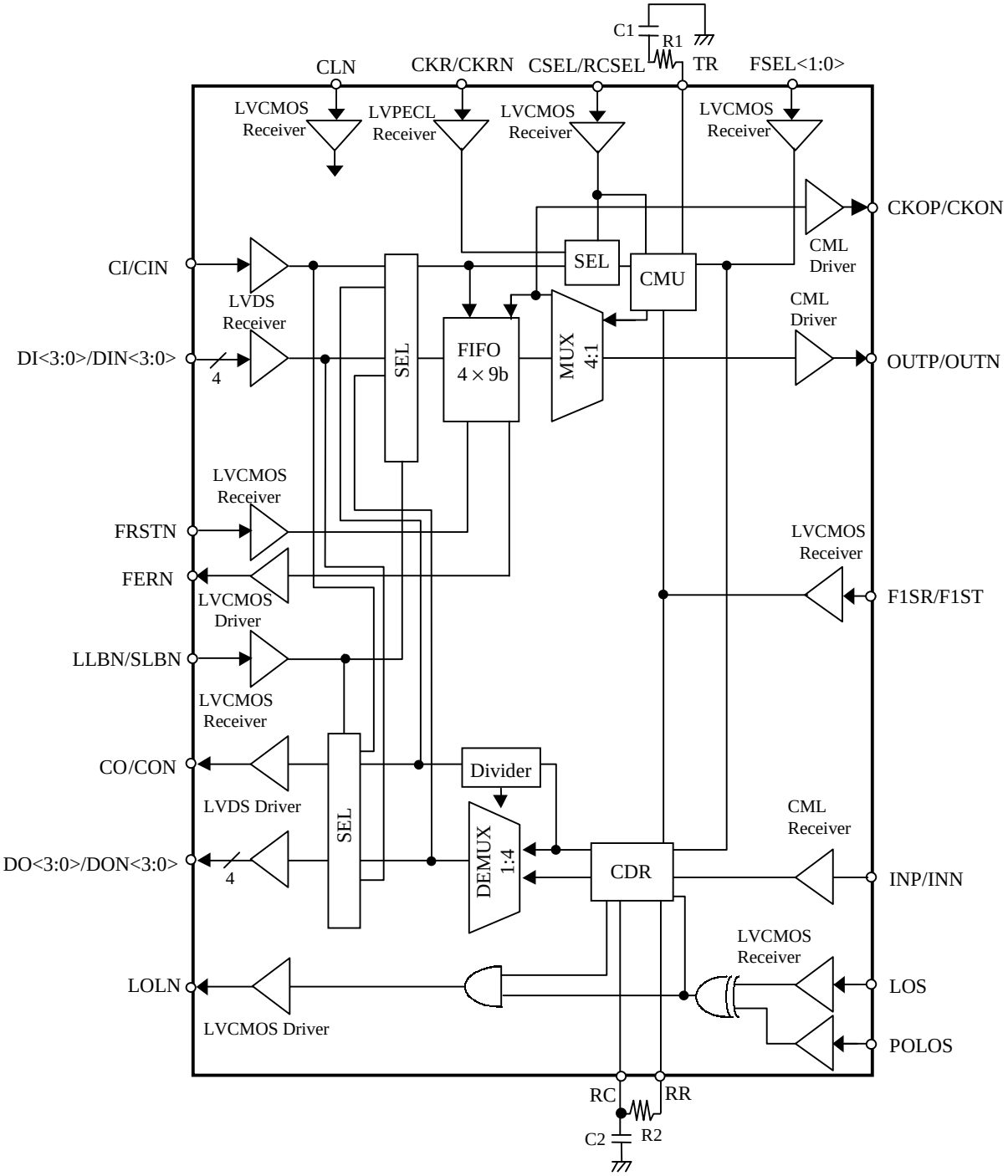


Figure 1 Functional Block Diagram

<Functional Description (Transmitter)>

1. Transmitter

The transmitter performs the SONET/SDH OC-48/12/3 and Gigabit Ethernet 4:1 serialization function. The transmitter 622.08-Mb/s (when the serial data rate is OC-48, 2.48832 Gb/s) × 4-bit parallel input data are latched into the FIFO with the transmitter low-speed input clock. The internal low-jitter 2.48832-GHz clock is generated from the external 155.52- or 622.08-MHz reference clock with the clock multiplication unit (CMU). The latched data in the FIFO are read out with the clock generated by dividing the low-jitter 2.48832-GHz clock by four in the multiplexer (MUX). The MUX serializes the 4-bit parallel to 1-bit serial data.

1-1. LVDS Parallel Input

The transmitter receives 622.08-Mb/s (for OC-48; for Gigabit Ethernet, OC-12, OC-3, or OC-48 with FEC, parallel data rate is 312.5 Mb/s, 155.52 Mb/s, 38.88 Mb/s, or 666.5 Mb/s, respectively) × 4-bit parallel data (DI/DIN). It also receives the parallel clock (CI/CIN) which has the same speed of the parallel data (input timing between DI/DIN and CI/CIN will be described later). The interface level is Low-Voltage Differential Signals (LVDS) and the LVDS receiver has an internal 100-Ω line-to-line termination resistor.

1-2. FIFO

The received 4-bit parallel data are written into the FIFO with the received parallel clock. The FIFO has a depth of 9 words. After the parallel data are written into the FIFO to the 5^{th} word, the data are read out with the low-jitter clock supplied from the MUX. Because the FIFO has ±4-word margin as against the 5^{th} word, the transmitter is tolerant of timing aberration of up to ±16 UI in serial data rate. When the number of the remaining word which can be read out from the FIFO or which can be written into the FIFO becomes one (empty state or full state, respectively), FIFO error output (FERN) goes to low. When FIFO reset input (FRSTN) or reset input (CLN) goes to low, the FIFO is reset and FERN returns to high. Once FERN goes to low, FERN remains low until FRSTN or CLN goes to low.

1-3. 4:1 Multiplexer (MUX)

The MUX operates with the low-jitter *f*-GHz clock (*f*: serial data rate) supplied from the CMU and generates the clock at a frequency of *f*/4 GHz. The *f*/4-GHz clock is used to read out 4-bit data from the FIFO, and is available for a upstream device like a framer through transmitter low-speed output clock (CKOP/CKON). The MUX serializes the 4-bit data to the serial data.

<Functional Description (Transmitter) continued>

1-4. Clock Multiplication Unit (CMU)

The clock multiplication unit generates the low-jitter *f*-GHz (*f*: serial data rate) clock using the internal VCO by multiplying the 155.52- or 622.08-MHz reference clock (CKR/CKRN) by 16 or 4, respectively, or by multiplying the *f*/4-MHz parallel input clock (CI/CIN) by 4. The generated low-jitter *f*-GHz clock is supplied to the MUX. The reference clock select input (CSEL) selects whether the CMU uses CKR/CKRN or CI/CIN as a reference clock. The reference clock rate select input (RCSEL) selects CKR/CKRN clock rate of 155.52 MHz or 622.08 MHz. The rate select inputs (FSEL0 and FSEL1) change the data rate. The transmitter FEC-rate select input (F1ST) changes the transmitter data rate from 2.48832 Gb/s to 2.666 Gb/s.

1-5. CML Serial Output

The *f*-Gb/s serial output data (OUTP/OUTN) are transmitted with the differential CML level. For the output, 100-Ω line-to-line termination is recommended.

1-6. Reference Clock and Reference Clock Select

The reference clock (CKR/CKRN) is 155.52- or 622.08-MHz differential LVPECL signal. The frequency of CKR/CKRN is set by RCSEL (H: 155.52 MHz, L: 622.08 MHz). When CSEL is high, the parallel input clock (CI/CIN) is selected as a reference clock instead of CKR/CKRN. When CSEL is low, CKR/CKRN is normally used for a reference clock. The interface level of RCSEL and CSEL is LVCMOS. The input of RCSEL has an internal 10-kΩ pull-up resistor and the input of CSEL has an internal 10-kΩ pull-down resistor. In order to meet the SONET/SDH jitter generation specifications, it is required that the accuracy of reference clock frequency is better than ±20ppm and the maximum reference clock phase noise is less than –140 dBc/Hz @50 kHz.

<Functional Description (Transmitter) continued>

1-7. Data-rate Select

The data-rate select inputs (FSEL0 and FSEL1) select the data rate of the NLD0442 as follows. The interface level of FSEL0 and FSEL1 is LVCMOS and each input has an internal 10-kΩ pull-up resistor.

Table 1 Data-rate Select

FSEL0	FSEL1	Data Rate	Units
H (or NC)	H (or NC)	2.48832	Gb/s
H (or NC)	L	1.25	Gb/s
L	H (or NC)	622.08	Mb/s
L	L	155.52	Mb/s

The FEC-rate select input (F1ST: transmitter side, F1SR: receiver side) changes the data rate of 2.48832 Gb/s to that of 2.666 Gb/s as follows. The interface level of F1ST is LVCMOS and the input has an internal 10-kΩ pull-up resistor.

Table 2 FEC-rate Select

F1ST	Data Rate	Units
H (or NC)	2.48832	Gb/s
L	2.66606	Gb/s

1-8. External Loop Filter

Recommended values of the external loop filter components are

C1 = 2.2 μF, R1 = 910 Ω (see Fig. 1).

1-9. Reset

Both the transmitter and receiver can be reset by inputting low to the reset input (CLN). By inputting low to the FIFO reset input (FRSTN), only FIFO can be reset. The interface level of CLN and FRSTN is LVCMOS and each input has an internal 10-kΩ pull-up resistor.

<Timing Characteristics (Transmitter)>

Table 3 High-speed Output Timing Characteristics

Parameter	Description	Min	Max	Units	Conditions
tr_to	OUTP/OUTN Rise Time	-	150	ps	20-80%
tf_to	OUTP/OUTN Fall Time	-	150	ps	20-80%

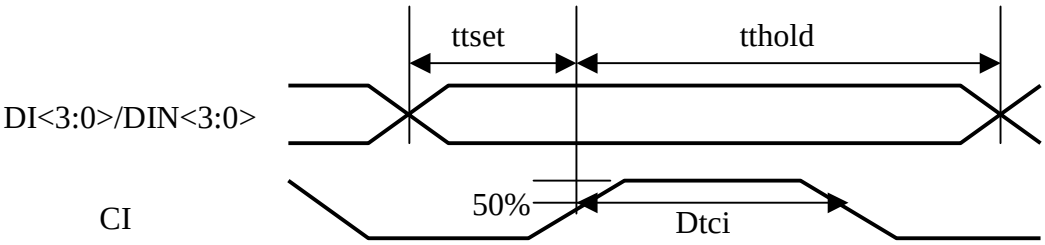


Figure 2 Low-speed Input Timing Waveforms

Table 4 Low-speed Input Timing Characteristics

Parameter	Description	Min	Max	Units	Conditions
ttset	DI/DIN Setup Time with respect to CI Rise Edge	200	-	ps	
tthold	DI/DIN Hold Time with respect to CI Rise Edge	200	-	ps	
Dtci	CI Duty Cycle Tolerance	40	60	%	

<Functional Description (Receiver)>

2. Receiver

The receiver performs the SONET/SDH OC-48/12/3 and Gigabit Ethernet 1:4 deserialization function. A 2.48832-GHz clock (when the serial data rate is OC-48, 2.48832 Gb/s) is generated from the receiver serial input data with the clock and data recovery (CDR). The serial input data are retimed by the recovered clock, and then the demultiplexer (DEMUX) deserializes the retimed data to 4-bit parallel data. The parallel data are retimed by the clock generated by dividing the 2.48832-GHz recovered clock by four. The characteristics of the CDR complies with SONET/SDH jitter specifications.

2-1. CML Serial Input

The receiver receives 2.48832-Gb/s (for OC-48; for Gigabit Ethernet, OC-12, OC-3, or OC-48 with FEC, data rate is 1.25 Gb/s, 622.08 Mb/s, 155.52 Mb/s, or 2.666 Gb/s, respectively) serial input data (INP/INN). The input has an internal 100-Ω line-to-line termination resistor and has an internal bias for AC coupling. When INP/INN is left open, the value of the serial input is indefinite.

2-2. Clock and Data Recovery

The clock and data recovery (CDR) extracts a clock at the same frequency as the serial bit rate from the incoming serial data (INP/INN). The serial data are retimed by the recovered clock in the CDR. Jitter characteristics meet the Bellcore GR-253-CORE and ITU-T G.958.

No reference clock is required for the CDR. The receiver has the loss-of-lock output (LOLN). LOLN goes to low when the serial input data are not present or the PLL in the CDR does not lock to the serial input data. LOLN signal is obtained from

LOLN = CLN and (LOS xor POLOS) and LOLN_cdr,

where LOLN_cdr is a loss-of-lock signal of the CDR and is active low. LOS is the loss-of-signal input connected to a O/E module or limiting amplifier IC. POLOS selects whether LOS is active high or active low. When ‘LOS xor POLOS’ is low, the receiver recognizes the serial input data are not present, and then the CDR provides a self-run clock of the VCO and low-level data. Therefore, even when LOS is active, the self-run clock is put out to the parallel output clock (CO/CON), though the parallel output data (DO/DON) remain low. LOLN is LVCMOS output, and LOS and POLOS are LVCMOS inputs. LOS has a pull-down resistor and POLOS has a pull-up resistor. Each resistance is 10 kΩ.

<Functional Description (Receiver) continued>

2-3. 1:4 Demultiplexer (DEMUX)

The DEMUX deserializes the *f*-GHz clock and *f*-Gb/s serial data (*f*: serial data rate) supplied from the CDR to *f*/4-GHz clock and *f*/4-Gb/s 4-bit parallel data.

2-4. LVDS Parallel Output

The *f*/4-Gb/s parallel data (DO/DON) and clock (CO/CON) from the DEMUX are transmitted to a downstream device like a framer with the LVDS drivers. The positive and negative outputs of the LVDS driver should be connected with a 100-Ω line-to-line termination resistor at a downstream device.

2-5. Reference Clock

No reference clock is required for the CDR.

2-6. Data-rate select

The serial data rate is selected by FSEL0 and FSEL1 inputs as follows. The interface level of FSEL0 and FSEL1 is LVCMOS and each input has an internal 10-kΩ pull-up resistor.

Table 5 Data-rate Select

FSEL0	FSEL1	Data Rate	Units
H (or NC)	H (or NC)	2.48832	Gb/s
H (or NC)	L	1.25	Gb/s
L	H (or NC)	622.08	Mb/s
L	L	155.52	Mb/s

The FEC-rate select input (F1ST: transmitter side, F1SR: receiver side) changes the data rate of 2.48832 Gb/s to that of 2.666 Gb/s as follows. The interface level of F1SR is LVCMOS. The input of F1SR has an internal 10-kΩ pull-up resistor.

Table 6 FEC-rate Select

F1SR	Data Rate	Units
H (or NC)	2.48832	Gb/s
L	2.66606	Gb/s

2-7. External Loop Filter

Recommended values of the external loop filter components are

C2 = 4.7 µF, R2 = 100 Ω (see Fig. 1).

<Functional Description (Receiver) continued>

2-8. Reset

The receiver and transmitter can be reset by inputting low to the reset input (CLN). When CLN is low, the parallel output data (DO/DON) and clock (CO/CON) go to low and LOLN also goes to low. (In contrast, when LOS is active, CO/CON is active and self-run clock of VCO is put out to CO/CON, as described in section 2-2.)

<Timing Characteristics (Receiver)>

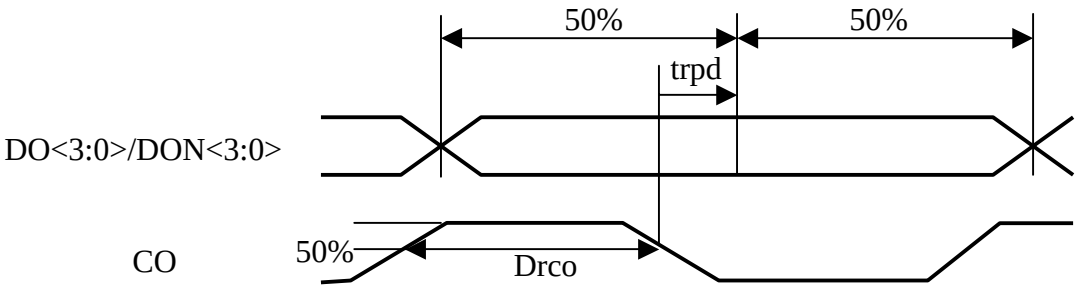


Figure 3 Low-speed Output Timing Waveforms

Table 7 Low-speed Output Timing Characteristics

Parameter	Description	Min	Max	Units	Conditions
trpd	Delay from CO Fall Edge to the Center of DO/DON Eye	-200	200	ps	
Drco	CO Duty Cycle	45	55	%	
tr_ro	Output Rise Time	-	300	ps	20-80%
tf_ro	Output Fall Time	-	300	ps	20-80%
tsro	DO<3:0> Channel Skew	-	TBD	ps	

<Functional Description (Other Operating Modes)>

3. Loopback Operation

The NLD0442 provides two loopback modes to facilitate line and system testing. The line loopback mode is enabled when LLBN is low. The system loopback mode is enabled when SLBN is low. Both enable pins are LVCMOS inputs. Each input has an internal 10-kΩ pull-up resistor.

3-1. Line Loopback

Serial input data of the receiver is looped back and transmitted to the serial output port of the transmitter. This loopback enables to test the line connections of serial signal. In this mode, the test signal is passed through the CML receiver, CDR, DEMUX, selector, FIFO, MUX, and CML driver.

3-2. System Loopback

Four-bit parallel input data of the transmitter are looped back and transmitted to the 4-bit parallel output ports of the receiver. This loopback enables to test the system connections of parallel signal. In this mode, Each test signal is passed through the LVDS receiver, selector, and LVDS driver.

4. On-chip Voltage Regulator

The NLD0442 integrates two types of on-chip bandgap voltage reference (BGR). The one is used for a reference voltage of the on-chip series regulator (SR) and the other is used for current control of the charge-pump and the VCO.

4-1. Series Regulator (SR)

The series regulator (SR) converts external 3.3-V power supply into 1.8-V for the core circuits. The 1.8-V output voltage of the SR has no dependence on temperature variation because the reference voltage provided by the BGR is temperature-independent. The SR enables the NLD0442 to operate at a single power supply of 3.3 V.

<Specifications>

Table 8 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Storage Temperature	Ts	-60	-	150	°C	
3.3 V Supply Voltage with respect to GND	VDD	-0.5	-	4.6	V	
Signal Pin Voltage with respect to GND	Vi	-0.5	-	VDD +0.5	V	
CMOS Output Current	Io	-	-	30	mA	
ESD Protection Voltage	Vesd	TBD	-	-	V	HBM

Table 9 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Ambient Temperature Under Bias	Ta	-40	20	85	°C	
Junction Temperature Under Bias	Tj	-20	40	105	°C	With recommended PKG
3.3 V Supply Voltage with respect to GND	VDD	3.135	3.3	3.465	V	±5%
3.3 V Supply Current	Ivdd	-	310	TBD	mA	

Table 10 Transmitter/Receiver Performance Specifications

VDD = 3.3 V±5%, Ta = -40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
Serial Data Rate (INP/INN, OUTP/OUTN)	Fdrate		2.48832		Gb/s	OC-48
			622.08		Mb/s	OC-12
			155.52		Mb/s	OC-3
			2.66606		Gb/s	OC-48with FEC
			1.25		Gb/s	GbE
Acquisition Time	Taq		2		ms	OC-48
Jitter Tolerance (INP/INN) (in OC-48 Operation)	Jtol	15			UIpp	Jitter Frequency: 600 Hz
		1.5				6 kHz
		1.5				100 kHz
		0.15				1 MHz
Reference Clock Frequency (When using CKR/CKRN)	Fref		155.52 or 622.08		MHz	w/o FEC
			166.63 or 666.51			with FEC
Reference Clock Frequency Tolerance	Freftol	-100		100	ppm	
		-20		20		for SONET/SDH
Reference Clock Duty Cycle	Dref	TBD		TBD	%	
Jitter Peaking (at Jitter Frequencies of up to Jitter Transfer Band Width)	Jpeak			0.1	dB	
Jitter Transfer Band Width	BWj			1.8	MHz	OC-48
Jitter Generation	Jgen		0.005	0.008	UIrms	Using 12k-20MHz
			0.05	0.08	UIpp	Bandpass Filter.

<Interface Specifications>

Table 11 LVDS Receiver/Driver DC Characteristics

VDD = 3.3 V±5%, Ta = -40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
LVDS Receiver						
Input High Voltage	VIH	-	-	1650	mV	
Input Low Voltage	VIL	750	-	-	mV	
Input Differential Threshold	Vidth	-100	-	100	mV	
Differential Input Impedance	Rin	80	-	120	Ω	
LVDS Driver						
Output High Voltage	VOH	-	-	1600	mV	100 Ω line to line
Output Low Voltage	VOL	800	-	-	mV	100 Ω line to line
Output Differential Voltage	|Vod|	200	-	600	mV	100 Ω line to line
Output Offset Voltage	Vos	1000	-	1400	mV	100 Ω line to line

Table 12 CML Receiver/Driver DC Characteristics

VDD = 3.3 V±5%, Ta = -40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
CML Receiver						
Input High Voltage	VIH	VDD -0.90	-	VDD -0.15	V	
Input Low Voltage	VIL	VDD -1.70	-	VDD -0.60	V	
Input Differential Voltage	|Vid|	200	-	950	mV	
Differential Input Impedance	Rin	80	-	120	Ω	
CML Driver						
Output High Voltage (Data)	VOH	VDD -0.80	-	VDD -0.20	V	100 Ω line to line
Output Low Voltage (Data)	VOL	VDD -1.60	-	VDD -0.65	V	100 Ω line to line
Output Differential Voltage (Data)	|Vod|	350	-	800	mV	100 Ω line to line
Output High Voltage (Clock)	VOH	VDD -1.00	-	VDD -0.20	V	100 Ω line to line
Output Low Voltage (Clock)	VOL	VDD -1.90	-	VDD -0.65	V	100 Ω line to line
Output Differential Voltage (Clock)	|Vod|	350	-	800	mV	100 Ω line to line

<Interface Specifications continued>

Table 13 LVCMOS Receiver/Driver DC Characteristics

VDD = 3.3 V±5%, Ta = -40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
LVCMOS Receiver						
Input High Voltage	VIH	2.0	-	VDD +0.3	V	
Input Low Voltage	VIL	-0.3	-	0.8	V	
LVCMOS Driver						
Output High Voltage	VOH	VDD -0.2	-	-	V	IOH = -100 µA
Output Low Voltage	VOL	-	-	0.2	V	IOL = 100 µA

Table 14 LVPECL Receiver DC Characteristics

VDD = 3.3 V±5%, Ta = -40 to 85 °C

Parameter	Symbol	Min	Typ	Max	Units	Conditions
LVPECL Receiver						
Input High Voltage	VIH	VDD -1.165	-	VDD -0.88	V	
Input Low Voltage	VIL	VDD -2.02	-	VDD -1.475	V	

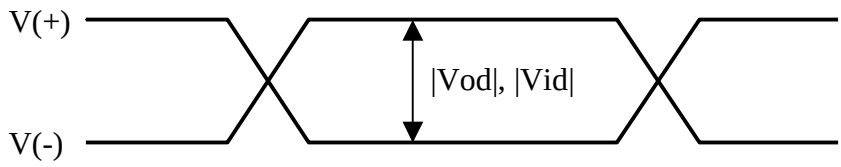
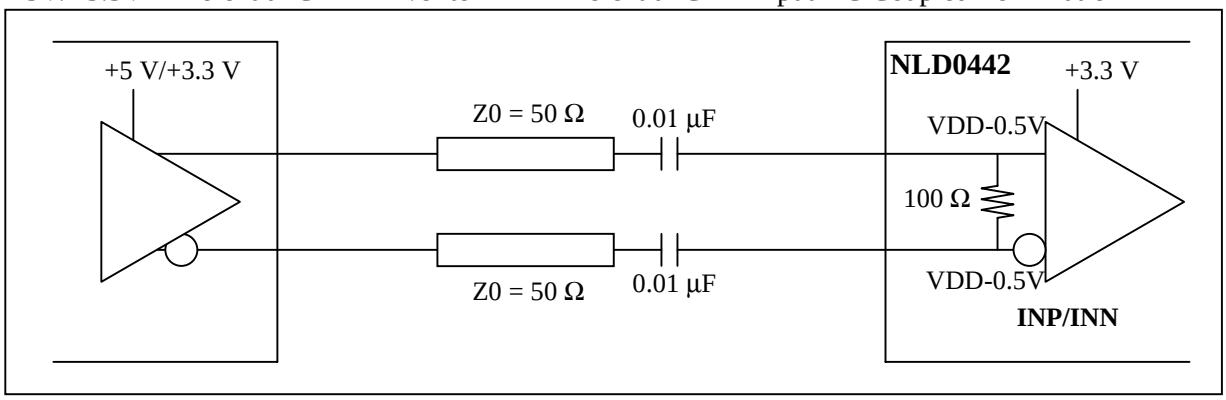


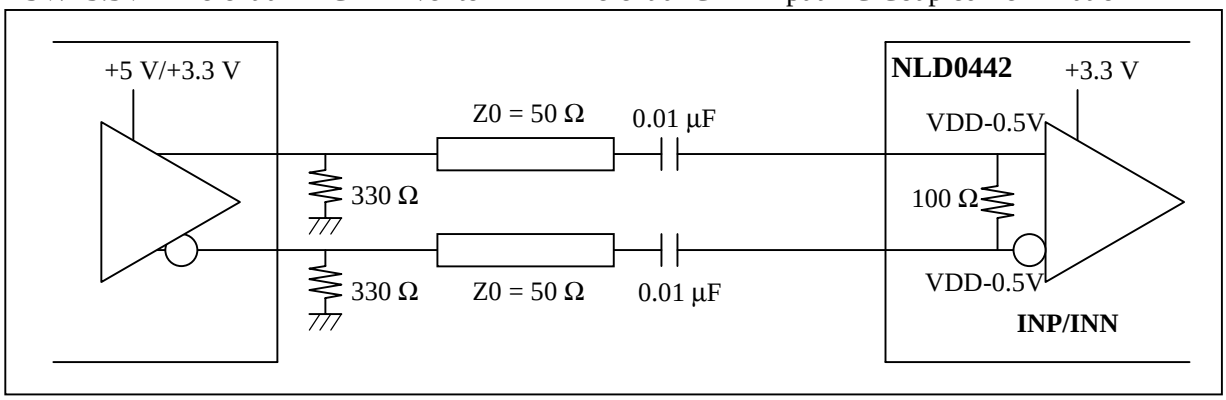
Figure 4 Differential Voltage

<Interface Connections>

+5V/+3.3V Differential CML Driver to TRx Differential CML Input AC Coupled Termination



+5V/+3.3V Differential PECL Driver to TRx Differential CML Input AC Coupled Termination



+3.3V Differential CML Driver to TRx Differential CML Input DC Coupled Termination

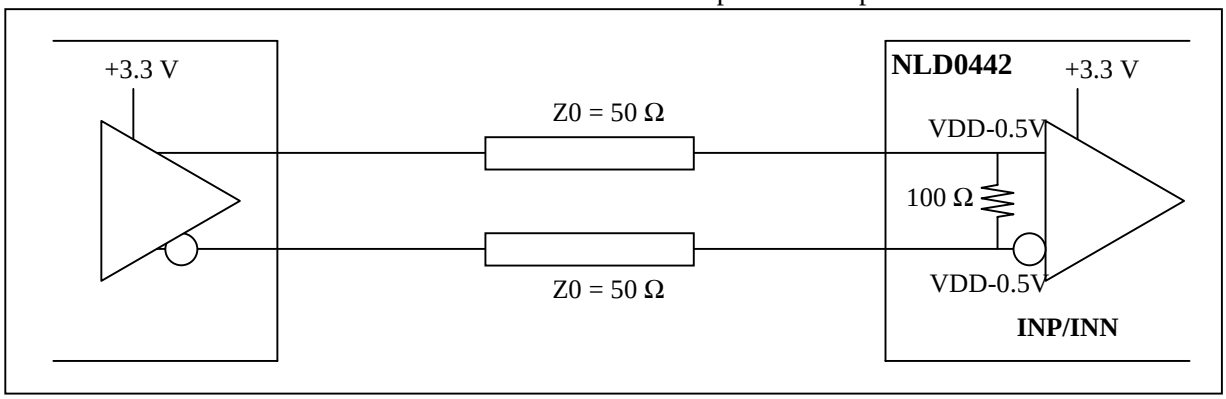
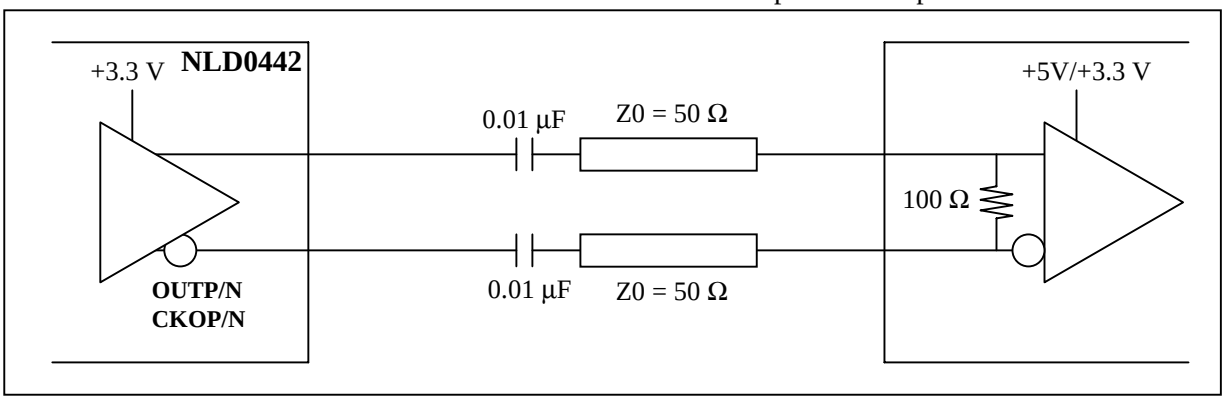
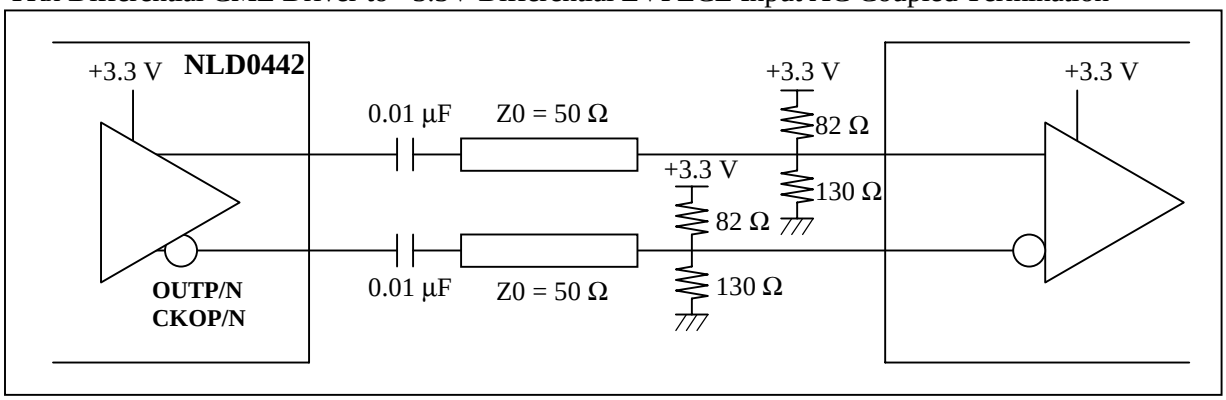


Figure 5 CML Receiver Termination

TRx Differential CML Driver to +5V/+3.3V Differential CML Input AC Coupled Termination



TRx Differential CML Driver to +3.3V Differential LVPECL Input AC Coupled Termination



TRx Differential CML Driver to +3.3V Differential CML Input DC Coupled Termination

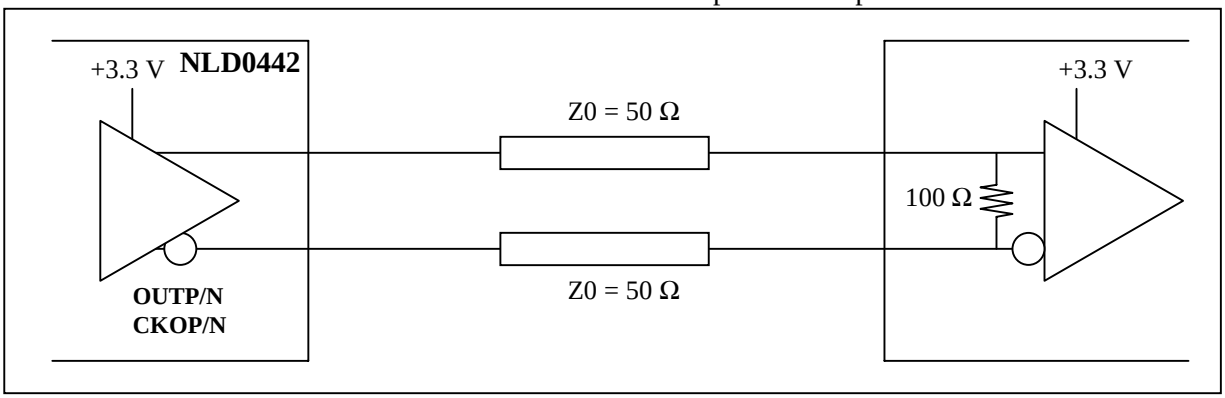


Figure 6 CML Driver Termination

TRx Differential CML Driver to LVDS Input AC Coupled Termination

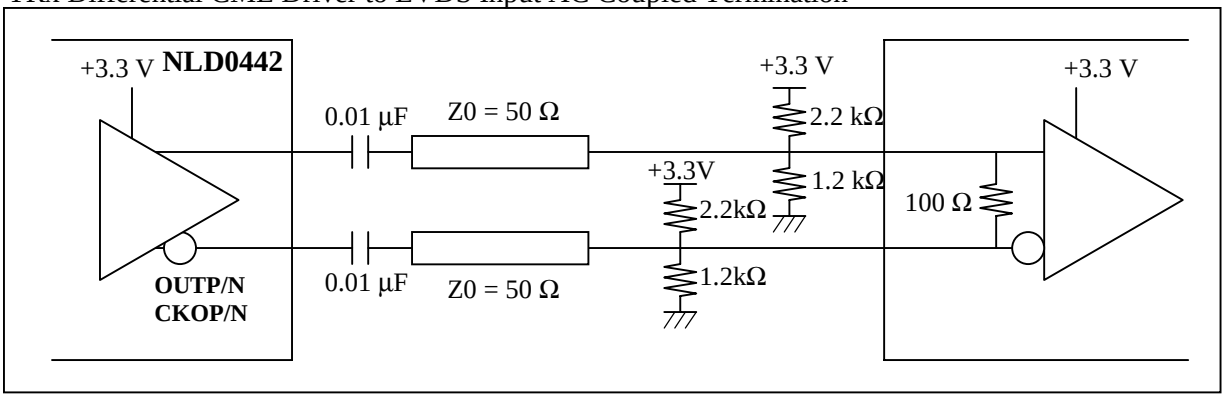
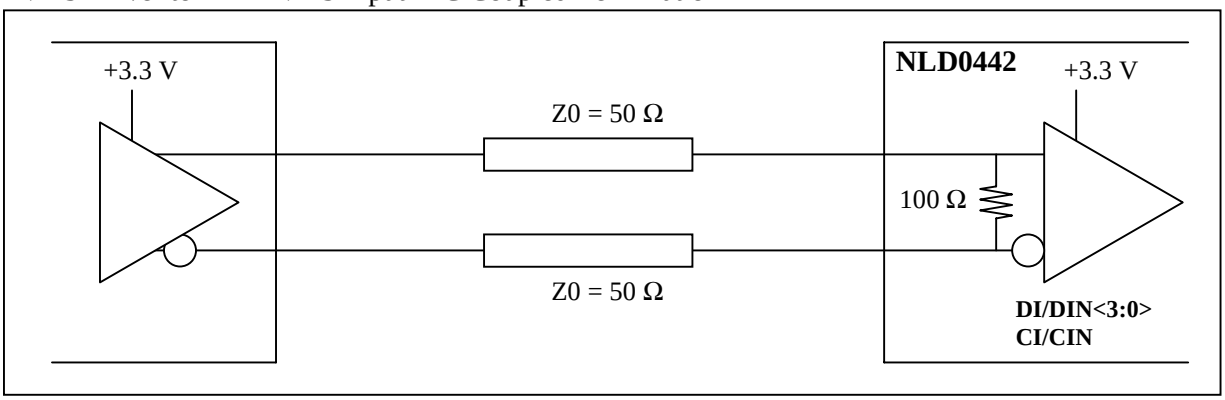


Figure 6 CML Driver Termination (continued)

LVDS Driver to TRx LVDS Input DC Coupled Termination



+3.3V Differential LVPECL Driver to TRx LVDS Input AC Coupled Termination

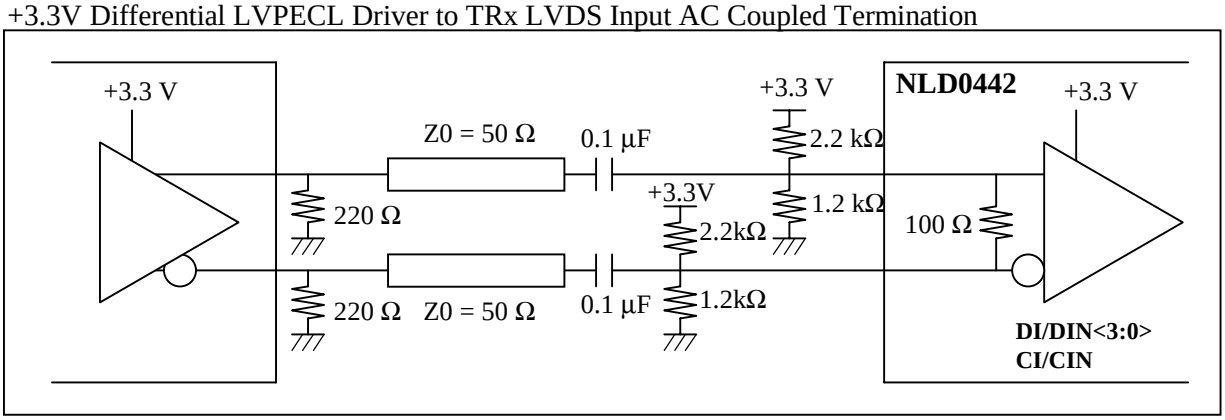
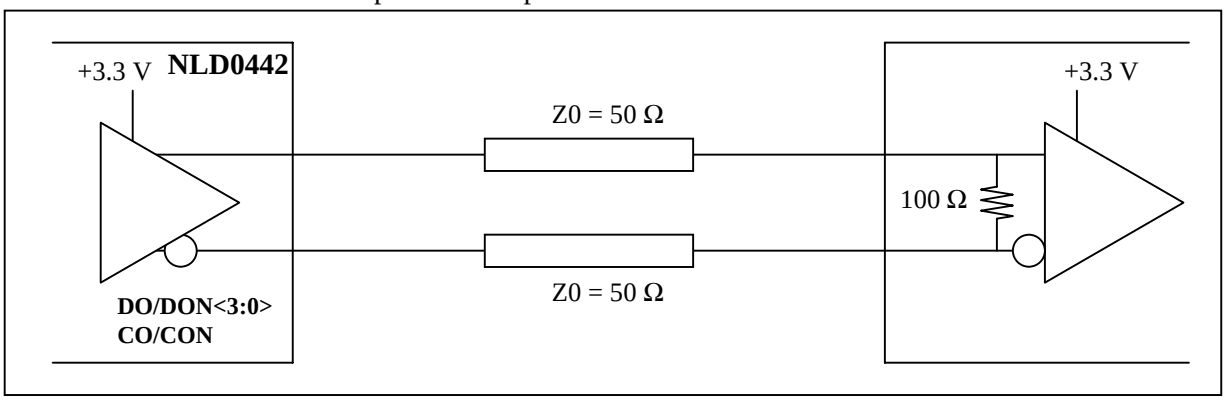


Figure 7 LVDS Receiver Termination

TRx LVDS Driver to LVDS Input DC Coupled Termination



TRx LVDS Driver to +3.3V Differential LVPECL Input AC Coupled Termination

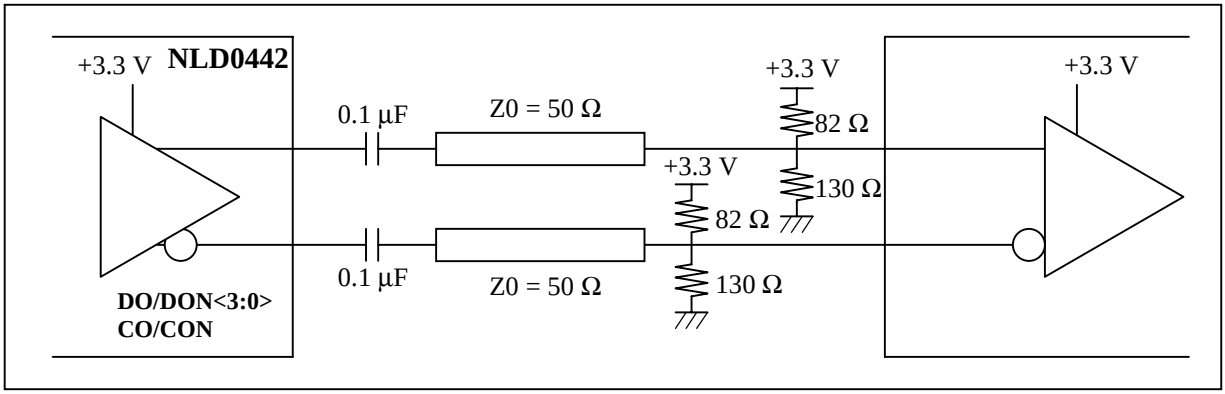


Figure 8 LVDS Driver Termination

+3V Differential LVPECL Driver to TRx Differential LVPECL Input DC Coupled Termination

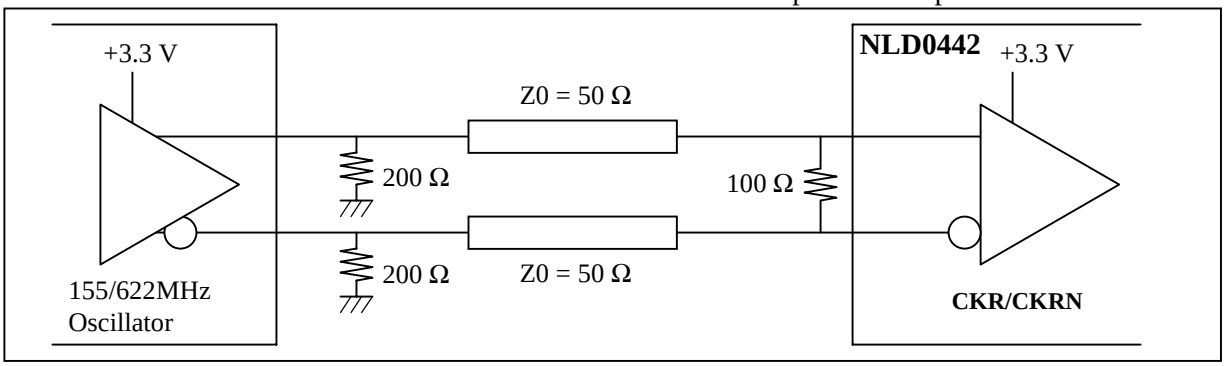
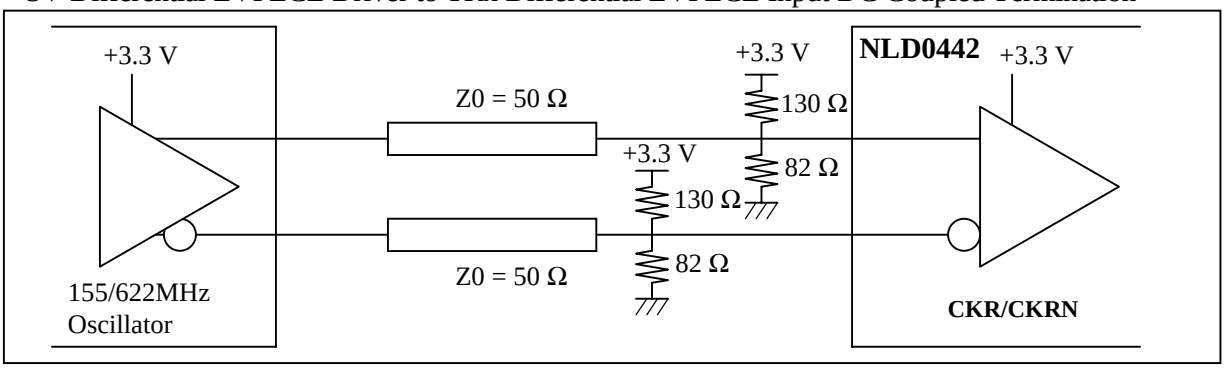
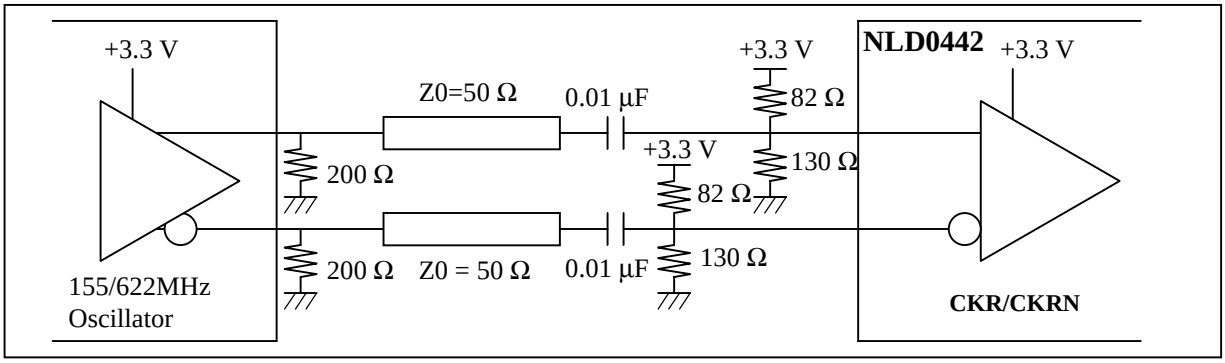


Figure 9 LVPECL Receiver Termination

+3V Differential LVPECL Driver to TRx Differential LVPECL Input DC Coupled Termination



+3V Differential LVPECL Driver to TRx Differential LVPECL Input AC Coupled Termination



+5V Differential PECL Driver to TRx Differential LVPECL Input AC Coupled Termination

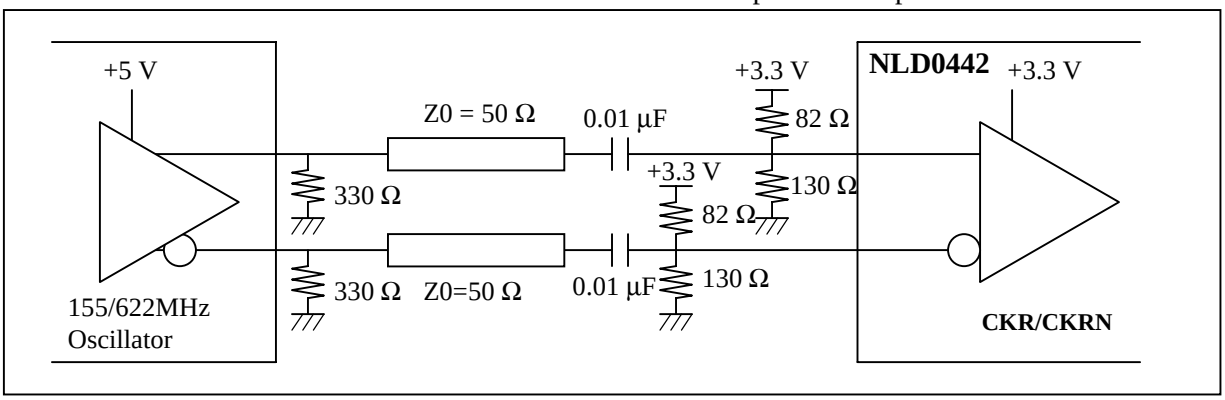


Figure 9 LVPECL Receiver Termination (continued)

TRx LVCMOS Driver to +3.3V LVCMOS Input

Figure 10 LVCMOS Driver Connection

+3.3V LVCMOS Driver to TRx LVCMOS Input (with an Internal Pull-down Resistor)

+3.3V LVCMOS Driver to TRx LVCMOS Input (with an Internal Pull-up Resistor)

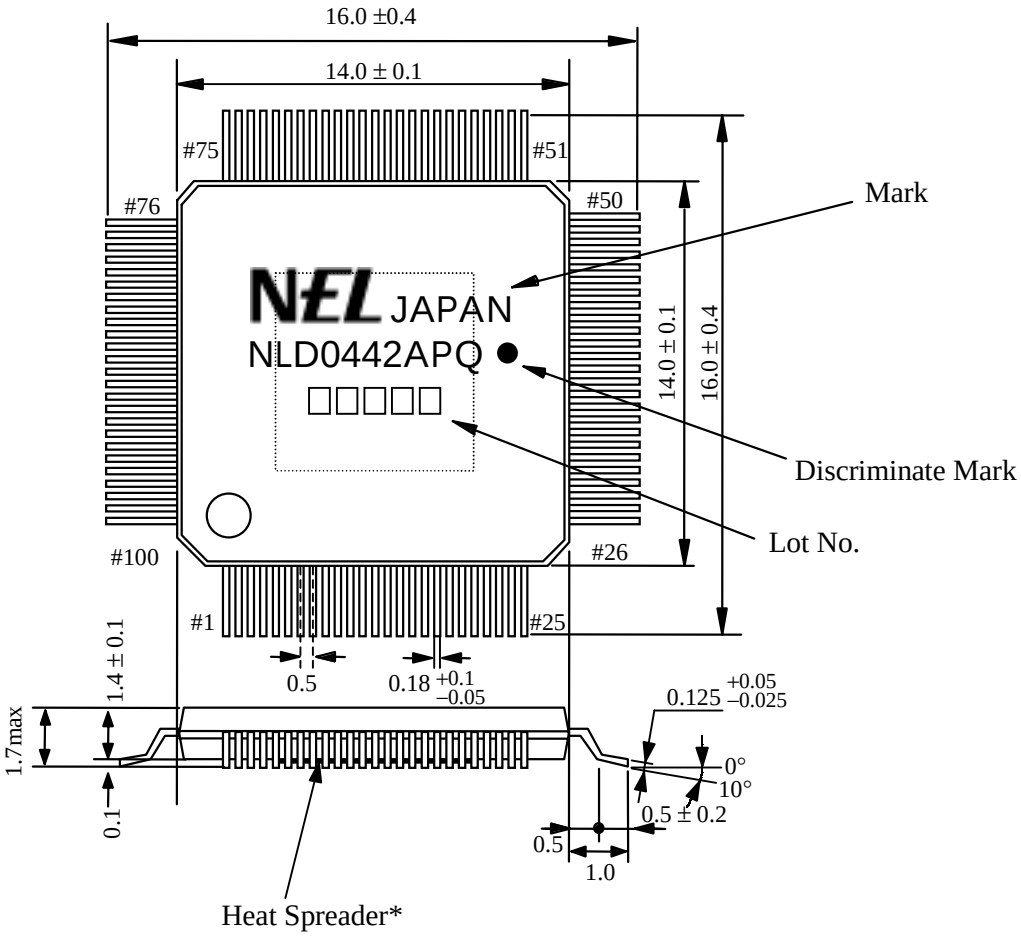
Figure 11 LVCMOS Receiver Connection

<Pin Configuration>

Table 15 Pin Configuration

Pin No.	Pin Name	I/O	Level	Pin No.	Pin Name	I/O	Level
1	NC	-	-	51	DON<0>	O	LVDS
2	CSEL	I	LVCMOS	52	DO<0>	O	LVDS
3	VDD16	PWR	3.3V	53	DON<1>	O	LVDS
4	CKON	O	CML	54	DO<1>	O	LVDS
5	CKOP	O	CML	55	DON<2>	O	LVDS
6	VSS16	PWR	0V	56	DO<2>	O	LVDS
7	VSS98	PWR	0V	57	DON<3>	O	LVDS
8	VDD9	PWR	3.3V	58	DO<3>	O	LVDS
9	OUTN	O	CML	59	CON	O	LVDS
10	OUTP	O	CML	60	CO	O	LVDS
11	VSS9	PWR	0V	61	FRSTN	I	LVCMOS
12	VSS1	PWR	0V	62	CLN	I	LVCMOS
13	RCSEL	I	LVCMOS	63	VSS10	PWR	0V
14	LLBN	I	LVCMOS	64	DIN<0>	I	LVDS
15	SLBN	I	LVCMOS	65	DI<0>	I	LVDS
16	VSS8	PWE	0V	66	DIN<1>	I	LVDS
17	VDM8	(Monitor)	-	67	DI<1>	I	LVDS
18	VDD8	PWE	3.3V	68	DIN<2>	I	LVDS
19	INN	I	CML	69	DI<2>	I	LVDS
20	INP	I	CML	70	DIN<3>	I	LVDS
21	VDD7	PWR	3.3V	71	DI<3>	I	LVDS
22	LOS	I	LVCMOS	72	CIN	I	LVDS
23	POLOS	I	LVCMOS	73	CI	I	LVDS
24	VSS7	PWR	0V	74	VDD10	PWR	3.3V
25	VSSH	PWR	0V	75	VSS10	PWR	0V
26	FCDR	I	LVCMOS	76	FSEL0	I	LVCMOS
27	NC	-	-	77	FSEL1	I	LVCMOS
28	NC	-	-	78	FERN	O	LVCMOS
29	NC	-	-	79	CKRN	I	LVPECL
30	F1SR	I	LVCMOS	80	CKR	I	LVPECL
31	VDD14	PWR	3.3V	81	F1ST	I	LVCMOS
32	NC	-	-	82	VSS1	PWR	0V
33	VSS14	PWR	0V	83	VDM1	(Monitor)	-
34	VDD4	PWR	3.3V	84	VDD1	PWR	3.3V
35	VDM4	(Monitor)	-	85	VSS12	PWR	0V
36	VSS4	PWR	0V	86	NC	-	-
37	VSS4	PWR	0V	87	VDD12	PWR	3.3V
38	RC	AC	-	88	VSS6	PWR	0V
39	RR	AC	-	89	VDM6	(Monitor)	-
40	VDD15	PWR	3.3V	90	VDD6	PWR	3.3V
41	NC	-	-	91	TR	AC	-
42	VSS15	PWR	0V	92	VSS13	PWR	0V
43	VDD3	PWR	3.3V	93	NC	-	-
44	VDM3	(Monitor)	-	94	VDD13	PWR	3.3V
45	VSS3	PWR	0V	95	VSS5	PWR	0V
46	LOLN	O	LVCMOS	96	VDM5	(Monitor)	-
47	VDD2	PWR	3.3V	97	VDD5	PWR	3.3V
48	VSS2	PWR	0V	98	NC	-	-
49	NC	-	-	99	NC	-	-
50	VSS1	PWR	0V	100	VSS99	PWR	0V

<Package Diagram>



*The heat spreader should be soldered to a 9-mm × 9-mm ground pad on the board.

Figure 12 Package Diagram (100-pin Plastic TQFP)

<Pin Assignment and Description>

Table 16 Output Pin Assignment and Descriptions

Pin No.	Name	I/O	Level	Description
4 5	CKON CKOP	O	Differential CML	Transmitter low-speed output clock. A quarter-rate clock is generated by dividing the internal bit clock by four. It can be used to coordinate 4-bit wide transfers between upstream logic and the NLD0442.
9 10	OUTN OUTP	O		Transmitter serial output data normally connected to an optical transmitter (E/O) module.
51 52 53 54 55 56 57 58	DON<0> DO<0> DON<1> DO<1> DON<2> DO<2> DON<3> DO<3>	O	LVDS	Receiver low-speed parallel output data. DO<0> is the least significant bit corresponding to the last bit received. The fall edge of the CO is centered about DO<3:0>.
59 60	CON CO	O		Receiver low-speed output clock. A quarter-rate clock that is aligned to DO<3:0>.
46	LOLN	O	LVCMOS	CDR loss-of-lock signal. Active low. LOLN goes to low when CDR does not lock to the serial input data, LOS (loss-of-signal) is active, or CLN is low.
78	FERN	O		FIFO error signal. FERN goes to low when FIFO becomes full or empty.

Table 17 Input Pin Assignment and Descriptions

Pin No.	Name	I/O	Level	Description
19 20	INN INP	I	Differential CML	Receiver serial input data normally connected to an optical receiver (O/E) module. Internally biased and terminated
79 80	CKRN CKR	I	Differential LVPECL	Transmitter reference clock. CKR/CKRN are connected to a crystal oscillator supplying reference 155.52/622.08 MHz clock.
64 65 66 67 68 69 70 71	DIN<0> DI<0> DIN<1> DI<1> DIN<2> DI<2> DIN<3> DI<3>	I	LVDS	Transmitter low-speed parallel input data. DI<0> is the least significant bit corresponding to the last bit transmitted. The rise edge of the CI samples DI<3:0>. Internally terminated.
72 73	CIN CI	I		Transmitter low-speed input clock. A quarter-rate clock, to which DI<3:0> is aligned. Internally terminated.
14	LLBN	I	LVCMOS	Line loopback enable. Active Low. When active, INP/INN is presented at OUTP/OUTN. Internal pull-up resistor.
15	SLBN	I		System loopback enable. Active Low. When active, DI<3:0> is presented at DO<3:0>. Internal pull-up resistor.
2	CSEL	I		Reference clock select input. High: CI/CIN is used as a reference clock, Low: CKR/CKRN is used as a reference clock. Internal pull-down resistor.
13	RCSEL	I		Reference clock rate select input. High: 155.52 MHz, Low: 622.08 MHz. Active when CSEL is Low. When CSEL is high, RCSEL is don't care. Internal pull-up resistor.
22	LOS	I		Loss-of-signal input. LOS is connected to O/E module or Limiting amplifier IC LOS/SD output. When active, CDR operates at the VCO self-run frequency and LOLN goes to low. Internal pull-down resistor.
23	POLOS	I		LOS active polarity select input. When POLOS is high, LOS is active high. When POLOS is low, LOS is active low. Internal pull-up resistor.
26	FCDR	I		Connect to Ground.
30	F1SR	I		Receiver FEC-rate select. High: 2.488 Gb/s, Low: 2.666 Gb/s. Internal pull-up resistor.
81	F1ST	I		Transmitter FEC-rate select. High: 2.488 Gb/s, Low: 2.666 Gb/s. Internal pull-up resistor.
76 77	FSEL0 FSEL1	I		Rate select. FSEL0/FSEL1 is HH: 2.488 Gb/s, LH: 1.25 Gb/s, HL: 622 Mb/s, LL: 156 Mb/s. Internal pull-up resistor.
61	FRSTN	I		FIFO reset. Active low. Internal pull-up resistor.
62	CLN	I		Reset. Active low. Internal pull-up resistor.
38	RC	I	Analog	Receiver CDR loop filter.
39	RR	I		Receiver CDR loop filter.
91	TR	I		Transmitter CMU loop filter.

Table 18 Common Pin Assignment and Descriptions

Pin No.	Name	I/O	Level	Description
84 47 43 34 97 90 21 18 8 74 87 94 31 40 3	VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD12 VDD13 VDD14 VDD15 VDD16	-	VDD 3.3V	Positive power supply pins.
12, 50, 82 48 45 36, 37 95 88 24 16 11 63, 75 85 92 33 42 6 7 100 25	VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS12 VSS13 VSS14 VSS15 VSS16 VSS98 VSS99 VSSH	-	GND	Ground pins.
83 44 35 96 89 17	VDM1 VDM3 VDM4 VDM5 VDM6 VDM8	-	(Monitor)	Internal voltage monitor pins.
1, 27, 28, 29, 32, 41, 49, 86, 93, 98, 99	NC	-	-	No connect, must leave floating.

<Application Note>

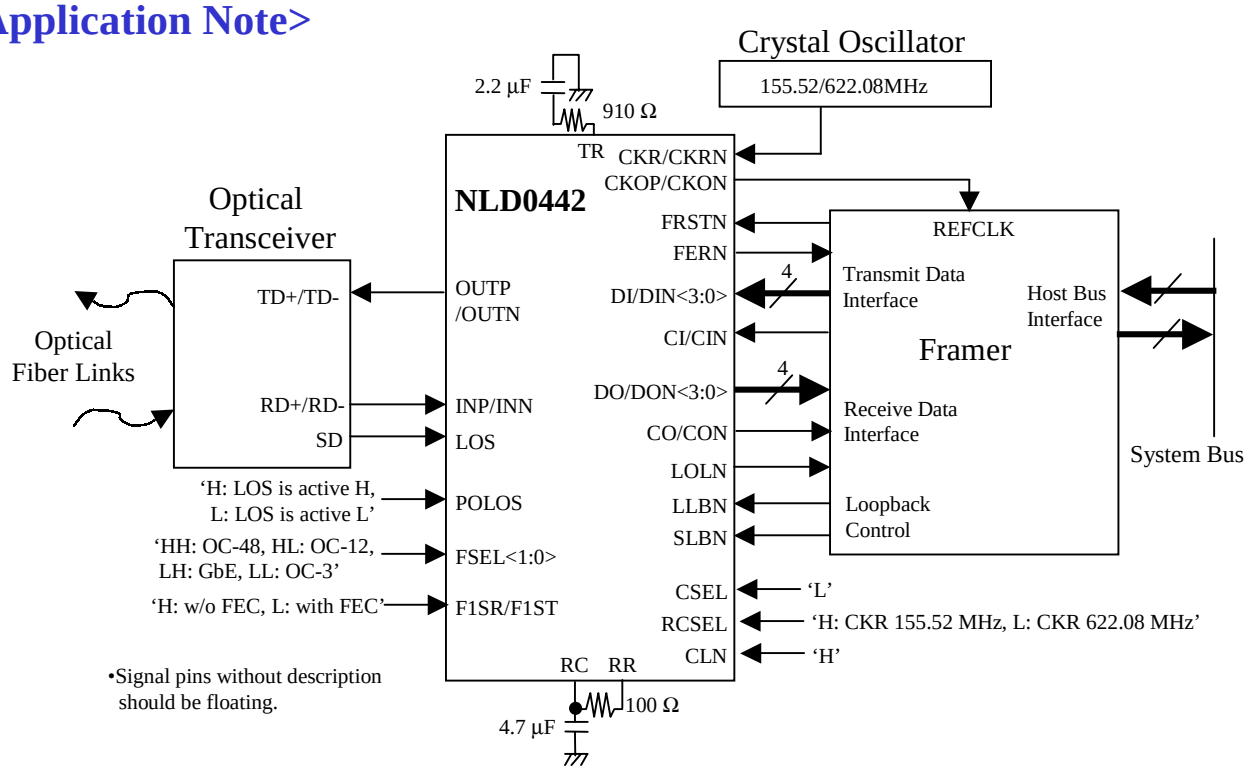


Figure 13 NLD0442 System Connection

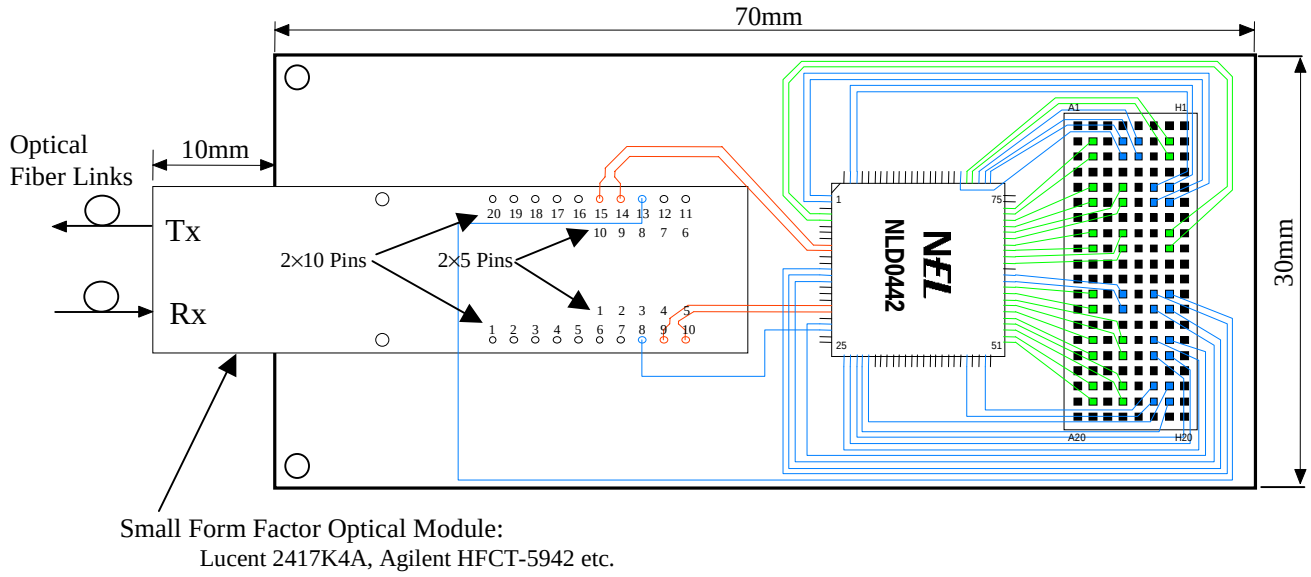


Figure 14 Compact and Low-power Transponder using NLD0442

Low-power Multi-rate (OC-48/12/3/GbE/FEC) SONET/SDH Transceiver

NLD0442

PRELIMINARY

NTT Electronics Corporation
Electronics Business Group
Sales Department, 1st Sales Department
1841-1, Tsuruma, Machida-shi, Tokyo
194-0004, Japan
Phone: +81-42-799-8537
Fax: +81-42-799-8534
www.nel-world.com