NWK935

100Base-TX Ethernet Physical Coding Sublayer

DS4409 - 1.3 May 1996

The NWK935 implements the Physical Coding Sublayer of the 100Mb/s Ethernet Physical Layer. It interfaces directly to the GPS NWK914 Transceiver and clock and data recovery device to provide a complete solution for the 100Mb/s Ethernet Physical Layer as defined in the 802.3u standard. The interface from the NWK935 to the Reconciliation level of the Data Link Layer is across a standard Media Independant Interface (MII) complying with 802.3u MII definition.

The NWK935 is manufactured on Zarlink Semiconductors' 0.8µm CMOS process. The device will be available in a QFP package.

FEATURES

- 100BASE-TX PCS Function complying to IEEE 802.3 Supplement u
- MII to Data Link Layer complying to IEEE 802.3 Supplement u
- Offers a 2-chip solution to the complete Ethernet 100Mb/s PHY
- Loop Back Test Mode Control
- LED Support for Status Indications
- Support for full and half Duplex Operations
- Support for Repeater Mode

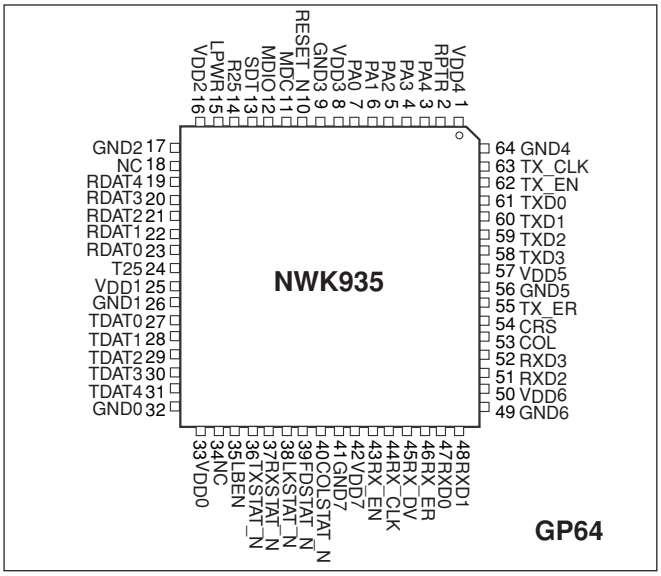


Fig.1 PCS pin description

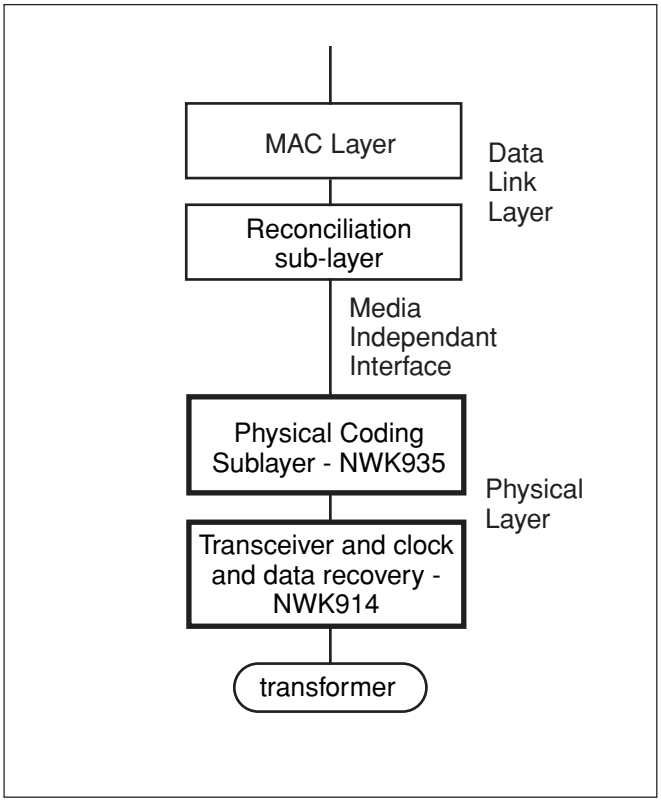


Fig.2 The PCS chip in a network application

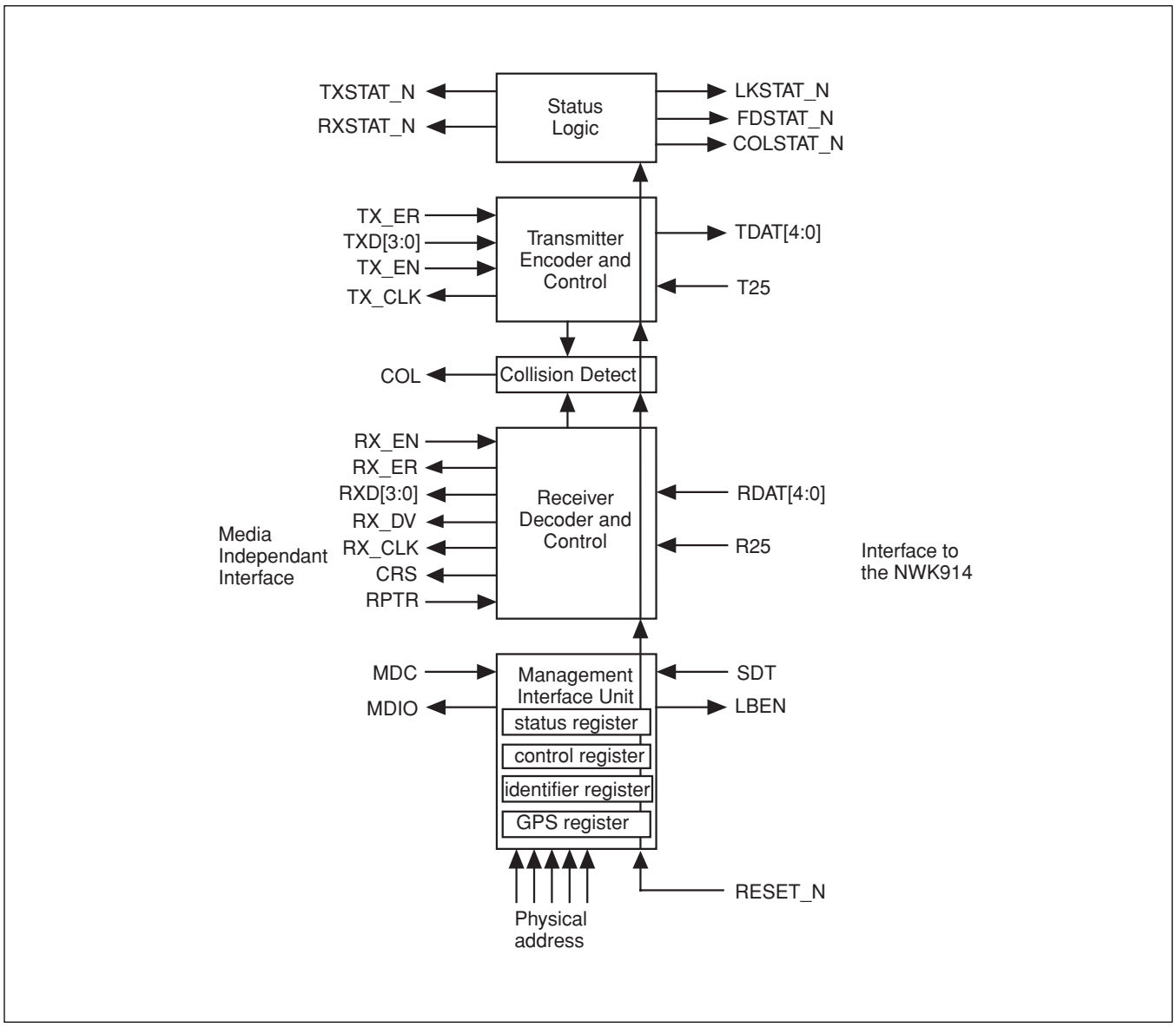


Fig. 3 Internal architecture of the NWK935

1.0 FUNCTIONAL DESCRIPTION

1.1 Data Exchange

The Data Link Layer (DLL) outputs data to the NWK935 on the TXD[3:0] bus of the MII. This data is synchronised to the rising edge of TX_CLK. To indicate that there is valid data for transmission on the MII, the DLL sets the TX_EN signal active. This forces the NWK935 device to take in the data on the TXD[3:0] bus and replaces the first octet of the MAC preamble with 2x4bit Start-of-Stream Delimiters (SSD) to indicate the start of the Physical Layer Stream. When the data transfer across the MII is complete, the DLL deasserts the TX_EN signal and the NWK935 adds 2x4bit End-of-Stream Delimiters (ESD) onto the end of the data stream. The complete data stream (the Physical Layer Stream) is then encoded from 4 bits into 5 bits, scrambled and output to the NWK914 for transmission on the cable.

If no data is being transmitted from the DLL, the NWK935 outputs an idle code of 11111(appropriately scrambled) that ensures that the link partner's receiver will remain synchronised

Data received from the cable is processed through the NWK914 and then input to the NWK935 on the RDAT[4:0] bus as 5 bit parallel, scrambled data. This is descrambled and decoded into 4 bit data by the NWK935 which then asserts the RX_DV signal whilst the SSD is on the MII, in order to inform the DLL that valid data is available. This data is sampled by the DLL on the rising edge of RX_CLK. When the NWK935 detects the ESD, it deasserts the RX_DV signal.

1.2 Receive Errors

When there is no activity on the cable, the receiver will see only the idle code of 1's. If activity is seen, (2 non-consecutive zeroes within 10 received bits) the receiver looks for the SSD so that it can align the incoming message for decoding. If the first half of the SSD is detected, and this is followed by anything other than the correct completion of the SSD, a false carrier indication is signalled to the MII by asserting RX_ER and setting RXD[3:0] to 1110 whilst keeping RX_DV inactive. The remainder of the message is ignored until 10 1's are detected.

If any data is decoded after a SSD which is neither a valid data code nor an ESD, then an error is flagged by setting RX_ER active whilst the RX_DV signal is active. This also happens if an idle code is detected before a valid ESD has been received. The states of RX_DV and RX_ER are summarised in Table 1. RX_ER is clocked on the falling edge of RX_CLK, and will remain active for at least 1 period of RX_CLK.

RX_DV	RX_ER	RXD[3:0]	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001 though 1101	Reserved
0	1	1110	False carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

Table 1: Receive error states

1.3 Transmit Errors

If the NWK935 detects that the TX_ER signal has gone active whilst the TX_EN signal is active, then it will propagate the detected error onto the cable by transmitting the data word "00100" (appropriately scrambled) to the NWK914. Table 2 shows the meaning of the different states of TX_EN and TX_ER. TX_ER is sampled inside the NWK935 on the rising edge of TX_CLK.

TX_EN	TX_ER	TXD[3:0]	Indication
0	X	0000 through 1111	Transmit idle code
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Table 2: Transmit error states

1.4 MII Management Interface

The management interface is a 2 wire serial interface connecting a PHY to a management entity. The management unit will control the PHY and will gather information on the status of the PHY. It will do this via 2 registers - register 0 (the control register) and register 1 (the status register).

1.4.1 The Control Register, Register 0

This register has 9 used bits and 7 reserved. They are defined in the 802.3u standard as in Table 3.The control register is defined in the NWK935 as follows:

1.4.1.1 Reset

Setting bit 15 of the control register to 1 will initiate the reset of the PHY. Bit 15 will remain at logic 1 until the reset is complete. This will be within 0.5 seconds of bit 15 being set. The action of resetting the device will ensure that the control and status registers are set to their default values. The control register will hold a value of 001000000 after initialisation. The status register will hold a value of 0110000001000000 (See Table 4)

The reset can be applied at any time, and may interrupt data communication.

1.4.1.2 Loop Back

When bit 14 is set to 1, the LBEN signal from the NWK935 into the NWK914 is set high. This ensures that the PHY receive and transmit circuitry is isolated from the network.

When the TX_EN signal is active, the data from the MII shall be passed from the transmit circuitry, into the NWK914 via the TDAT[4:0] bus, back into the NWK935 via the RDAT[4:0] bus, and out onto the MII on the RXD[3:0] bus. This ensures that much of the PHY can be tested in this mode. If bit 7 of the PCS control register is at logic zero, the COL signal will remain inactive at all times through the loop back test. If bit 7 is set to one, COL will behave as defined for the collision test.

1.4.1.3 Speed Selection

This is not applicable for the NWK935 as the device can only operate with 100Mb/s Ethernet. This bit will always be set high.

1.4.1.4 Auto- Negotiation Enable

This does not apply to the NWK935 as this device only operates with 100Mb/s Ethernet. This bit will always be set low.

Bit 15: Reset	1 = PHY reset
	0 = normal operation
Bit 14: Loop back	1 = enable loop back mode
	0 = disable loop back mode
Bit 13: Speed	1 = 100Mb/s
	0 = 10Mb/s
Bit 12: Auto-neg	1 = enable auto-neg process
	0 = disable auto-neg process
Bit 11: Power	1 = power down
down	0 = normal operation
Bit 10: Isolate	1 = isolate PHY from MII
	0 = normal operation
Bit 9: Restart	1 = restart auto-neg process
auto-neg	0 = normal operation
Bit 8: Duplex	1 = full duplex
mode	0 = half duplex
Bit 7: Collision	1 = enable COL signal test
Test	0 = disable COL signal test
Bit 6:0 Reserved	Write as 0
	Read as 0, but ignored

Table 3: 802.3u control register

All the control bits can be written and read. Bit 15 is self-clearing after a reset. Bits 10 and 11 must both be zero for normal operation.

1.4.1.5 Power Down

When this bit is set high,the NWK935 goes into low power mode. The TX_CLK and RX_CLK are stopped and the LPWR output from the NWK935 goes high.

1.4.1.6 Isolate

When bit 10 is set high in the control register, the PHY becomes electrically isolated from the MII. This means that there will be no response from the PHY to the TXD[3:0], TX_EN and TX_ER inputs. The PHY outputs, RX_CLK, TX_CLK, RX_DV, RX_ER, RXD[3:0], COL and CRS will be high impedance. For any NWK935 which is connected as one of multiple PHYs on a single MII this bit should be set to logic 1 to avoid having multiple drivers on the same signal simultaneously.

1.4.1.7 Restart Auto-Negotiation

This bit is always zero as auto-negotiation is not possible on the NWK935.

1.4.1.8 Duplex Mode

This bit is set to 1 to indicate that the device is working in full duplex mode, and that the collision detect logic is disabled and CRS goes high only to indicate receiver activity. The default value, zero, sets the device to work in half duplex mode with collision detect enabled.

1.4.1.9 Collision Test

When bit 7 is set high in the control register, the NWK935 will assert the COL signal active high within 512 BT (Bit Time) of TX_EN being asserted. COL will stay high until TX_EN goes low. COL will then be de-asserted within 4 BT.

1.4.2 The Status Register

The status register is a read only register which informs the management entity of the status of the PHY. The 802.3u standard defines the status register as shown in Table 4. The NWK935 definition of the status register is shown below:

1.4.2.1 100BASE-T4

This bit will be set low in the NWK935 to indicate that the device does not have this capability.

1.4.2.2 100BASE-X Full duplex

This bit is set high to indicate that the NWK935 is capable of working in full duplex mode. In this mode, the collision detect logic is disabled and the COL output remains low.

1.4.2.3 100BASE-X Half Duplex

This bit is set high to indicate that the NWK935 is capable of working in half duplex mode. In this mode, the collision detect logic may be active.

1.4.2.4 10Mb/s Full Duplex

This bit will always be set low as the NWK935 does not have a 10Mb/s capability.

1.4.2.5 10Mb/s Half Duplex

This bit will always be set low as the NWK935 does not have a 10Mb/s capability.

1.4.2.6 Auto-Negotiation Complete

The bit will always be set low as the NWK935 does not do auto-negotiation.

Bit 15: 100Base-T4	1 = Able to perform 100BASE-T4
	0 = Unable to perform 100BASE-T4
Bit 14: 100BASE-X Full Duplex	1 = Able to perform full duplex 100BASE-X
	0 = Unable to perform full duplex 100BASE-X
Bit 13: 100BASE-X Half Duplex	1 = Able to perform half duplex 100BASE-X
	0 = Unable to perform half duplex 100BASE-X
Bit 12: 10Mb/s Full Duplex	1 = Able to operate at 10Mb/s in full duplex mode
	0 = Unable to operate at 10Mb/s in full duplex mode
Bit 11: 10Mb/s Half Duplex	1 = Able to operate at 10Mb/s in half duplex mode
	0 = Unable to operate at 10Mb/s in half duplex mode
Bit 10:7 Reserved	Read as zero, but ignored.
Bit 6: MF Preamble Supression	1 = PHY accepts management frames with preamble supressed
	0 = PHY does not accept management frames with preamble supressed
Bit 5: Auto-Negotiation Complete	1 = Auto-negotiation process completed
	0 = Auto-negotiation process is not complete
Bit 4: Remote Fault	1 = Remote fault condition detected
	0 = No remote fault condition detected
Bit 3: Auto-Negotiation Ability	1 = Able to perform auto-negotiation
	0 = Unable to perform auto-negotiation
Bit 2: Link Status	1 = Link is up
	0 = Link is down
Bit 1: Jabber Detect	1 = jabber condition is detected
	0 = No jabber condition is detected
Bit 0: Extended Capability	1 = Extended register capability
	0 = Basic register set capabilities only

Table 4: 802.3u definition of status register

1.4.2.7 Remote Fault

This is not implemented in the NWK935 and so this bit is always set to zero in the status register.

1.4.2.8 Auto-Negotiation Ability

This bit will always be zero as the NWK935 has no auto-negotiation facility.

1.4.2.9 Link Status

This bit reflects the SDT pin from the NWK914. It will be set to 1 to indicate that the link is operational. When the SDT pin goes low to indicate that the signal level has fallen below a limit for reliable operation, the link bit is set low in the register. This link bit will remain low until the status register is read, even if the SDT pin returns high. Ref. 2.2.7.

1.4.2.10 Jabber Detect

This bit is always set to zero on the NWK935 as jabber detect is not implemented in the PHY layer for the 100BASE-TX.

1.4.2.11 Extended Capability

This bit is set high to indicate that the NWK935 has extended register capability.

1.5 PHY Identifier Register

Registers 2 and 3 provide a 32-bit identifier register. This holds the GPS OUI, 00A087, in bits 2:15 through to 3:10. 3:9 to 3:4 hold the model number, which is 1 for the NWK935. 3:3 to 3:0 hold the revision number.

1.6 Configuration Register

This is an 8-bit register at address 0x18. The bits are assigned as follows:

bit 0 - ERROR CODE: Changes the error code on receipt of a receive error from 0110 (error code 0) to 0101 (error code 1).

bit 1 - BPSCR: If this bit is set high, the scrambler and de-scrambler are by-passed.

bit 2 - BPENC: If this bit is set high, the encoder and decoder are by-passed.

bit 3 - BPALIGN: If this bit is set high, the align function on the received data is by-passed.

bit 4 - MF: If this bit is set high, the preamble on a management data frame can be ommitted if required. The preamble must be present if this bit is zero.

bits 5:7 - RESERVED: These bits must be driven low.

2.0 PIN DESCRIPTIONS

2.1 Media Independant Interface

2.1.1 TX_EN

The DLL drives this signal high when the first nibble of data is being presented on the TXD bus. The signal remains high until all the data has crossed the MII. TX_EN changes synchronously with TX_CLK and is ignored in ISOLATE mode.

2.1.2 TXD[3:0]

TXD[3:0] is the data bus from the DLL to the PHY. The data is sampled on the rising edge of TX_CLK and is considered valid by the PHY when the TX_EN signal is asserted. The TXD bus is ignored in ISOLATE mode.

2.1.3 TX_ER

Any erroneous conditions detected by the DLL will set this signal active high. When the NWK935 sees a high on this input and the TX_EN signal is high, it forces an error code of 00100 which is scrambled onto the TDAT bus. Any receiver will then detect this corruption and know an error condition has occurred. TX_ER is ignored in ISOLATE mode.

2.1.4 TX_CLK

This 25MHz clock is output from the NWK935 to the MII to provide the timing reference for the Reconciliation sublayer to produce the TXD, TX_ER and TX_EN signals. It is generated from the T25 clock from the NWK914. TX_CLK is stopped when the NWK935 is in low power mode and is high impedance when the device is in ISOLATE mode.

2.1.5 RX_DV

This Received Data Valid signal is driven by the NWK935 and goes active high to indicate that there is valid data present on the RXD[3:0] bus. RX_DV must be high by the time any start of frame delimiter is presented and goes low before any end of frame delimiter is passed across the MII or when an IDLE code is detected (An error condition is flagged if the an IDLE code is detected before the ESD). The RX_DV signal is clocked out on the RX_CLK. RX_DV is high impedance in ISOLATE mode.

2.1.6 RXD[3:0]

When RX_DV is high, received decoded data is presented on the RXD bus synchronously to RX_CLK.If RX_DV is low, RXD may be used to indicate a false carrier when RX_ER is high and the data is set to 1110. See Table 1 for all the possible combinations. The RXD bus is high impedance in ISOLATE mode.

2.1.7 RX_ER

RX_ER goes high to indicate that an error has occurred somewhere in the frame currently being passed on the RXD bus, from the PHY to the DLL. RX_ER is high impedance in ISOLATE mode.

2.1.8 RX_CLK

RX_CLK is nominally a 25MHz clock sourced by the NWK914. It is used to provide a timing reference for the RX_DV, RX_ER and RXD signals from the PHY to the Reconciliation sublayer. RX_CLK becomes high impedance in ISOLATE mode.

2.1.9 RX_EN

RX_EN high enables the drive on the RXD[3:0], RX_CLK, RX_DV and RX_ER outputs. If RX_EN is low, these outputs are all tri-stated.

2.1.10 CRS

The Carrier Sense output is an asynchronous signal which goes high when the NWK935 is either transmitting or receiving data in half-duplex mode and RPTR is low, or is receiving data in full-duplex mode or RPTR is high. CRS goes high when 2 non-consecutive zeroes are detected within 10 data bits. If these are not part of a SSD, then an error is flagged. CRS returns low when 10 consecutive high data bits (2 IDLE codes) are detected. CRS is high impedance in ISOLATE mode.

2.1.11 COL

The Collision Detect output goes high when the NWK935 is both transmitting and receiving data at the same time in half-duplex mode. In full-duplex mode, the COL output is disabled and remains low. COL is an asynchronous signal which is high impedance in ISOLATE mode.

2.1.12 MDC

The MDC signal is the management data clock, sourced by the PHY controller, to act as a timing reference for the transfer of data on the MDIO pin. This clock has a maximum frequency of 2.5MHz.

2.1.13 MDIO

MDIO is a bi-directional signal between the NWK935 and its controller. Control information passes to the NWK935 and status information passes from the NWK914. This signal should have a pull-up resistor on it if it is connected to the MII via a detachable connector.

2.1.14 RPTR

If RPTR is driven high, the device is set to work in repeater mode rather than NIC mode. This affects the CRS output only. In repeater mode CRS goes high when there is activity on the receiver only. When RPTR is low, the behaviour of CRS depends on whether the device is running in full or half duplex mode.

2.2 Interface to NWK914

2.2.1 TDAT[4:0]

This bus connects directly to the TDAT[4:0] bus on the NWK914. It is an output bus from the NWK935 and carries the sampled, encoded data. TDAT is clocked out by the 25MHz clock, T25.

2.2.2 RDAT[4:0]

This bus connects directly to the RDAT[4:0] bus on the NWK914. It is an input bus to the NWK935 and carries the encoded data. This data will be sampled by the R25 clock and decoded, before being output to the MII.

2.2.3 T25

This clock comes from the NWK914 and is input to a Schmitt trigger for noise protection. It is used to sample out the TDAT bus, and to generate the TX_CLK signal.

2.2.4 R25

This clock comes from the NWK914 and is input to the NWK935 via a Schmitt trigger for noise protection. It is used to generate the RX_CLK signal and to clock out the data on the RDAT bus.

2.2.5 LPWR

This output signal goes active high to indicate low power mode. When in low power mode, the internal transmitter clock and the RX_CLK and TX_CLK outputs are inhibited in a low state.

2.2.6 LBEN

This output is set by writing a logic one to bit 14 of the control register. The signal is input to the NWK914 to define the mode of operation, either loopback or normal.

2.2.7 SDT

This input, driven by the NWK914, goes high to indicate the presence of a valid signal on the cable. If the signal level received by the NWK914 falls below a limit for reliable operation, SDT goes low. SDT is fed into the status register in order to record the link status of the cable. Once the link status bit has gone low in the status register, it cannot be set high again until the status register has been read. Once SDT has been low, it must then stay high for a period of 650usecs before the link status of the device is reset and the device will be able to recognise the data on the receiver as valid. SDT is also used to generate the LKSTAT_N output.

2.3 MISC

2.3.1 PA[4:0]

The physical address bits, PA[4:0], are hardwired to inform the NWK935 of the address to which it must respond, on the management interface.

2.3.2 TXSTAT_N

This output pulses low to indicate that the NWK935 is transmitting data. It will remain low for a minimum of 600 usecs. This output can be used to drive an LED if required.

2.3.3 RXSTAT_N

This output pulses low to indicate that the NWK935 is receiving data. It will remain low for a minimum of 600 usecs and can be used to drive an LED if required.

2.3.4 LKSTAT_N

LKSTAT_N is normally low to indicate that the link is up. If the link goes down, LKSTAT_N will pulse high for a minimum of 30 msecs. This can be used to drive an LED if required.

2.3.5 FDSTAT_N

This output goes low to indicate that the device is in full duplex mode. It can be used to drive an LED if required.

2.3.6 COLSTAT_N

This output pulses low to indicate that a collision has been detected. It will remain low for a minimum of 600 usecs and can be used to drive an LED if required.

2.3.7 RESET_N

This input resets the device when it goes active low.

3.0 RATINGS AND CHARACTERISTICS

Clock	Frequency Rating	Duty Cycle
T25	25MHz +/-100ppm	45% to 55%
TX_CLK	25MHz +/-100ppm	40% to 60%
R25	nominal 25MHz	45% to 55%
RX_CLK	nominal 25MHz	40% to 60%
MDC	Maximum 2.5MHz	min 160ns high / low

Table 5: Clock ratings

ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

DC Electrical Characteristics

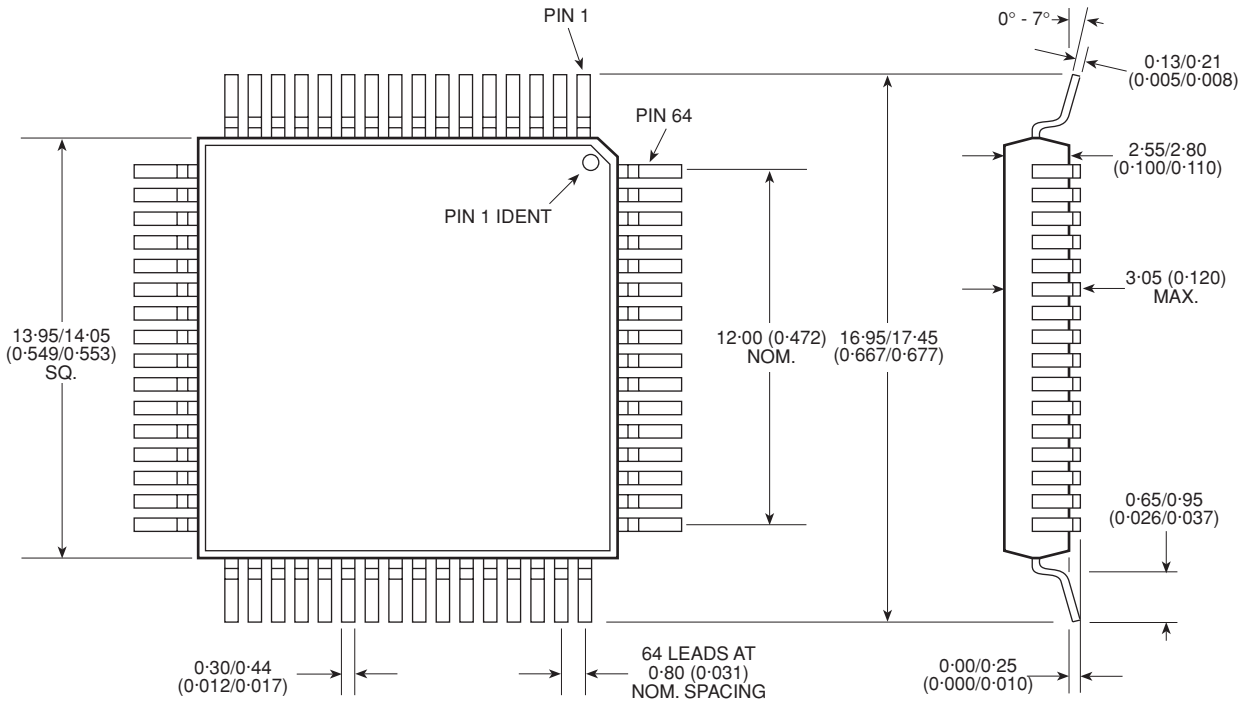
Characteristic	Symbol	Pin Type	Min	Max	Units	Conditions
Supply Voltage	Vcc	-	4.75	5.25	V	
Supply Current	Icc	-	-	150	mA	
Input high voltage	Vih	I, I/O	2.4	-	V	
Input low voltage	Vil	I, I/O	-	0.4	V	
Leakage current	Iih, Iozh	I, I/O	-	-2	uA	
Leakage current	Iil, Iozl	I, I/O	-	2	uA	
Output high voltage	Voh	o/p to 914	Vcc - 0.5	-	V	Ioh = -20uA
		stat o/p	Vcc - 0.5	-	V	
		o/p to MII	Vcc - 0.5	-	V	Ioh = -4mA
Output low voltage	Vol	o/p to 914	-	0.5	V	Iol = 400uA
		stat o/p	-	0.5	V	Iol = 1mA
		o/p to MII	-	0.5	V	Iol = 4mA

AC Electrical Characteristics

Parameter	Description	Min	Max	Units
T1	TXD[3:0] setup to TX_CLK rising	10	-	ns
T2	TXD[3:0] hold after TX_CLK rising	0	-	ns
T3	TX_EN setup to TX_CLK rising	10	-	ns
T4	TX_EN hold after TX_CLK rising	0	-	ns
T5	TX_ER setup to TX_CLK rising	10	-	ns
T6	TX_ER hold after TX_CLK rising	0	-	ns
T7	RXD[3:0] delay from RX_CLK falling	0	4	ns
T8	RX_DV delay from RX_CLK falling	0	4	ns
T9	RX_ER delay from RX_CLK falling	0	4	ns
T10	MDIO (input) setup to MDC rising	5	-	ns
T11	MDIO (input) hold after MDC rising	5	-	ns
T12	MDIO (output) delay after MDC rising	0	50	ns
T13	TX_CLK valid after T25	0	20	ns
T14	RX_CLK valid after T25	0	20	ns
T15	TDAT[4:0] after T25 rising	0	15	ns
T16	RX-EN low to outputs hi -Z	0	10	ns
T17	RX-EN high to outputs driven	0	15	ns

PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

64-LEAD PLASTIC QUAD FLATPACK – GP64

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