NWK937

10/100 Fast Ethernet Transceiver to MII

Advance Information

Supersedes June 1998 Edition

DS4843 - 3.1 Sept 1998

The NWK937 is a single chip CMOS physical layer solution from MII to the magnetics. It is designed for 10BASE-T and 100BASE-TX Ethernet, based on the IEEE 802.3 specifications.

The NWK937 is compatible with the Auto Negotiation section of IEEE 802.3u and provides all the support needed for the 802.3x Full duplex specification. The NWK937 has multiple operating modes as described in the control section.

FEATURES

- Integrated 10/100 Mbps Ethernet in a Single Chip Solution
- Half duplex and full duplex in both 10BASE-T and 100BASE-TX
- IEEE 802.3 compliant MII interface
- Link Status Change Interrupt
- Extended Register Set
- Integrated 10BASE-T Transceivers and Receive / Transmit Filters
- Integrated Adaptive Equaliser and Base Line Wander Correction
- Full Auto Negotiation Support for 10BASE-T and 100BASE-TX both Half and Full Duplex
- Low Dynamic Current
- Low Power Mode
- Internal Power on Reset
- 64 pin QFP Package
- Available in 64 Thin PQFP package
- Single Magnetics for 10BASE-T and 100BASE-TX Operation for a Single RJ45 Connector

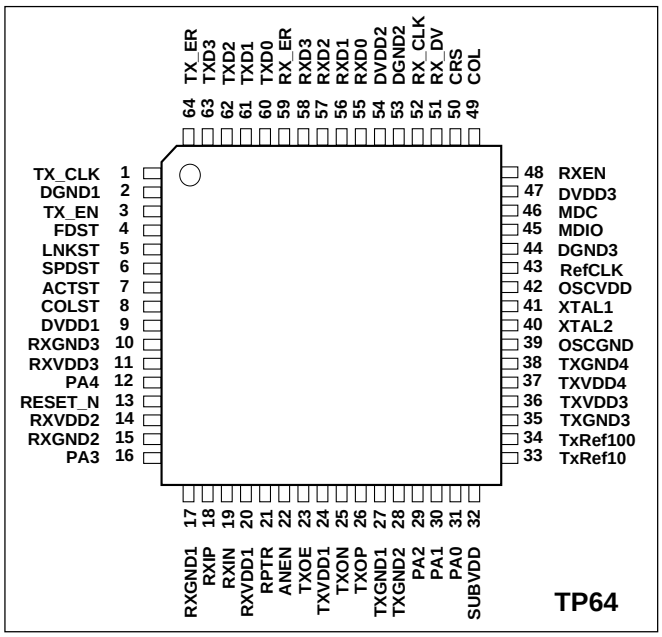

Fig.1 Pin connections - top view

- Support for Flow Control 802.3x Specification
- Integrated 5 LED Driver
- Low External Component Count

ORDERING INFORMATION

NWK937/CG/TP1N

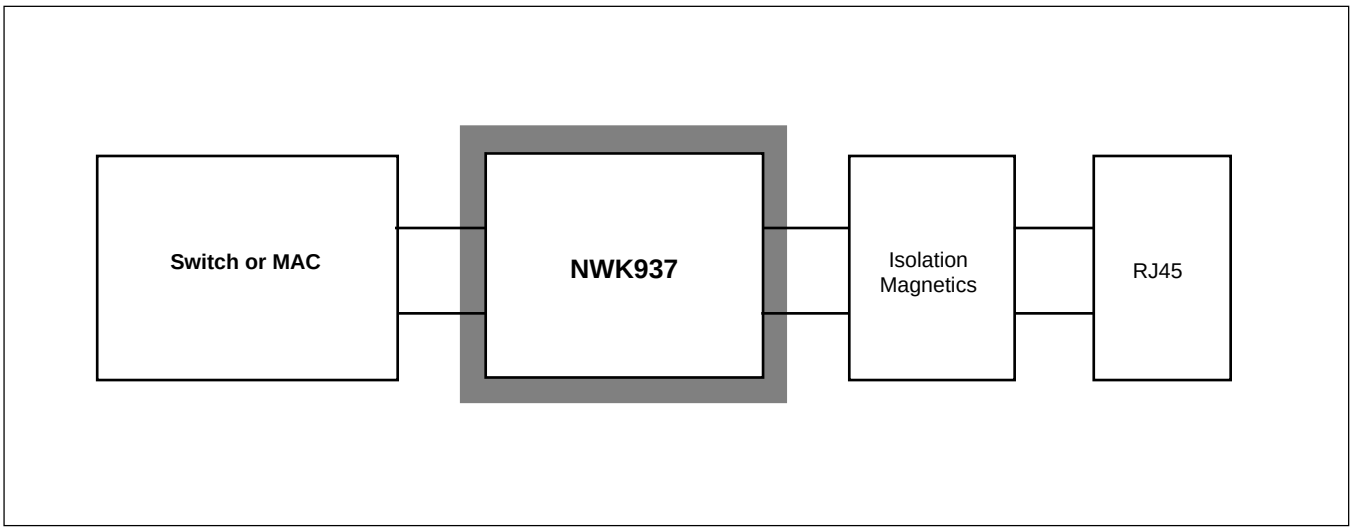

Fig.2 System block diagram

FUNCTIONAL DESCRIPTION

The NWK937 has three basic operating modes: 10BASE-T mode, 100BASE-TX mode and LOW-POWER mode. The modes are selected by bits 11 and 13 respectively in register 0.The Control block is designed to manage these modes by starting and stopping the two transceivers in a well-controlled manner such that no spurious signals are output on either the MII or twisted-pair interfaces. Furthermore, it continuously monitors the behaviour of the transceivers and takes corrective action if a fault is detected.

25MHZ REFERENCE CLOCK

The NWK937 requires a 25MHz +/-100ppm timing reference for 802.3 compatible operation. This may be supplied either from the integrated oscillator or from an external source. When the integrated oscillator is used, a suitable crystal must be connected across the XTAL1 & XTAL2 pins (see “External Components”). When an external source is used, it must be input to the REFCLK pin and XTAL1 must be tied high. XTAL2 must be unconnected.

10BASE-T OPERATION

10Mb/s Data Transfer on the MII

10Mb/s data is transferred across the MII with clock speeds of 2.5MHz. The MAC outputs data to the NWK937 via the MII interface, on the TXD[3:0] bus. This data is synchronised to the rising edge of TX_CLK. To indicate that there is valid data for transmission on the MII, the MAC sets the TX_EN signal active. This forces the NWK937 device to take in the data on the TXD[3:0] bus. This is serialised and directly encoded as Manchester data, before being output on the TXOP/TXON differential output for transmission through 1:1 magnetics and onto the twisted-pair.

The Pulse Shaper & Filter employs a digital finite impulse response filter (FIR) to pre-compensate for line distortion and to remove high frequency components in accordance with the 802.3 Standard. The transmit current is governed by the current through the TXREF10 pin, which must be grounded through a resistor as described in “External Components”.

RX10 Clock Recovery

The NWK937 employs a digital delay line controlled by the 100MHz Synthesizer DLL to derive a sampling clock from the incoming signal. The recovered clock runs at twice the data rate (nominally 20MHz). When a signal is received from the Signal Detect block, it is used to strobe Link Pulses and Manchester encoded serial data.

The Manchester data stream will be decoded into a 4-bit parallel data bus, RXD[3:0]. The RXD bus is clocked out on RX_CLK rising. The NWK937 must detect the first 4 bits of pre-amble before RX_DV is set high. With RX_DV is high, any Manchester coding violation will set RX_ER high. RX_DV is reset by a continuous sequence of zeroes, or by the end-of-packet IDLE terminator (11 11 00 00). Whilst RX_DV is low, the data on the RXD bus is always zero.

100MHz Synthesizer

This synthesizer employs a delay-locked loop (DLL) to generate a 100MHz timing reference from the 25MHz reference clock. This 100MHz reference is used by the 10BASE-T transmit and receive functions and is divided by 5 to provide a 20MHz data strobe. The 20MHz clock is used to derive the 2.5 MHz TX_CLK in 10BASE-T mode. The synthesizer is disabled when not in 10BASE-T mode.

TX10 Pulse Shaper & Filter

The Pulse Shaper & Filter employs a digital finite impulse response filter (FIR) to pre-compensate for line distortion and to remove high frequency components in accordance with the 802.3 Standard. The Pulse Shaper & Filter is disabled when not in 10BASE-T mode.

TX10 Latency

When connected to appropriate magnetics the latency through the TX10 path is less than 2BT (200ns) for data transmissions. This timing is measured from the falling edge of TX_CLK to the output of the transmit magnetics. The TX10 path will not transmit the first two Manchester encoded bits of a data transmission, as permitted by the 802.3 Standard.

RX10 Filter & RX10 Signal Detect

These blocks work in unison to remove noise and to block signals that do not achieve the voltage levels specified in 802.3. Signals that do not achieve the required level are not sampled in the Clock Recovery block and are not passed to the outputs.

RX10 Latency

When connected to appropriate magnetics the latency through the RX10 path is less than 6BT (600ns). This timing is measured from the input of the receive magnetics to the falling edge of RX_CLK. The RX10 path may ignore up to three Manchester encoded bits at the start of data reception (802.3 allows up to 5 bits).

100BASE-TX OPERATION

100Mb/s Data Exchange on the MII Interface

100Mb/s data is transferred across the MII using a 25MHz clock signal. The MAC outputs data to the NWK937 via the MII interface, on the TXD[3:0] bus. This data is synchronised to the rising edge of TX_CLK. To indicate that there is valid data for transmission on the MII, the MAC sets the TX_EN signal active. This forces the NWK937 device to take in the data on the TXD[3:0] bus and replace the first octet of the MAC preamble with Start-of-Stream Delimiter (SSD) symbols to indicate the start of the Physical Layer Stream.

When the data transfer across the MII is complete, the MAC deasserts the TX_EN signal and the NWK937 adds End-of-Stream Delimiters (ESD) symbols onto the end of the data stream. The complete data stream (the Physical Layer Stream) is encoded from 4 bits into 5 bits, scrambled, converted to MLT3 and driven to the TXOP and TXON pin differentially.

The TX100 path is disabled when not in 100BASE-TX mode and, with the exception of the RX100 Signal Detect, the RX100 Receive Path is disabled when not in 100BASE-TX mode.

125MHz Synthesizer

This synthesizer employs a phase-locked loop (PLL) to generate a 125MHz timing reference from the 25MHz reference clock. This 125MHz reference is used by the 100BASE-TX transmit function and is divided by 5 to provide a 25MHz data strobe on TX_CLK. TX_CLK is frequency and phase locked to the 25MHz reference with a small phase offset. The synthesizer is disabled when not in 100BASE-TX mode.

TX100 PISO, Encoder and Scrambler

The TX100 PISO, Encoder and scrambler loads data from the MII on the rising edge of TX_CLK, and converts them to serial MLT3 for outputting to the TX100 Driver. The TXD[3] bit is output first. The PISO & Encoder do not operate until the 125MHz Synthesizer is locked to the 25MHz reference. This avoids transmission of spurious signals onto the twisted-pair.

TX100 Driver

The TX100 Driver outputs the differential signal onto the TXOP and TXON pins. It operates with 1:1 magnetics to provide impedance matching and amplification of the signal in accordance with the 802.3 specifications. The transmit current is governed by the current through the TXREF100 pin, which must be grounded through a resistor as described in “External Components”. The TX100 driver is disabled in 10BASE-T mode and in loop back mode.If no data is being transmitted from the MAC, the NWK937 outputs idle symbols of 11111 (suitably scrambled).

TX100 Latency

The transmit latency from the first TX_CLK rising when TX_EN is high to the first bit of the “J” symbol on the cable is 8BT.

RX100 Equalizer & Base-line Wander Correction

The RX100 Equalizer compensates for the signal attenuation and distortion resulting from transmission down the cable and through the isolation transformers. The Equalizer is self-adjusting and is designed to restore signals received from up to 10dB cable attenuation (at 16MHz). When the Equalizer is active it adjusts to the incoming signal within 1ms. Thereafter, the Equalizer will continuously adjust to small variations in signal level without corrupting the received data.

The 100BASE-TX MLT3 code contains significant low frequency components which are not passed through the isolation transformers and cannot be restored by an adaptive equalizer. This leads to a phenomenon known as base-line wander which will cause an unacceptable increase in error rate if not corrected. The NWK937 employs a quantized feedback technique to restore the low frequency components and thus maintain a very low error rate even when receiving signals such as the “killer packet” described in the TP_PMD spec.

RX100 Clock Recovery

The RX100 Clock Recovery circuit uses a Phase-Locked Loop (PLL) to derive a sampling clock from the incoming signal. The recovered clock runs at the symbol bit rate rate (nominally 125MHz) and is used to clock the MLT3 decoder and the Serial to Parallel converter (SIPO). The recovered clock is divided by 5 to generate the receive clock (RX_CLK) which is used to strobe received data across the MII interface. When no signal is detected in 100BASE-TX mode, the PLL is locked to the reference clock and runs at 125MHz. This ensures that RX_CLK runs continuously at 25MHz in 100BASE-TX mode. When a signal is present, the Clock Recovery PLL remains locked to the reference until the equalizer has adjusted, then it requires up to 1ms to phase lock to the incoming signal. No data is passed to the MII interface until lock is established.

RX100 SIPO, Decoder and Descrambler

The RX100 SIPO, Decoder and descrambler convert the received signal from serial MLT3 to 4-bit wide parallel receive data on the MII. This appears on the RXD[3:0] bus which is clocked out on the rising edge of RX_CLK. When a frame starts the NWK937 decodes the SSD symbols and then asserts the RX_DV signal, in order to inform the MAC that valid data is available. When the NWK937 detects the ESD, it deasserts the RX_DV signal.

RX100 Latency

The latency from the first bit of the “J” symbol on the cable to CRS assertion is between 11 and 15BT. The latency from the first bit of the “T” symbol on the cable to CRS de-assertion is between 19 and 23BT.

100Mb/s Transmit Errors

If the NWK937 detects that the TX_ER signal has gone active whilst the TX_EN signal is active, then it will propagate the detected error onto the cable by transmitting the symbol “00100” . Figure 3 shows the meaning of the different states of TX_EN and TX_ER. TX_ER is sampled inside the NWK937 on the rising edge of TX_CLK.

TX_EN	TX_ER	TXD [3:0]	Indication
0	X	ignored	Normal inter frame data
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Fig 3. 100Mb/s transmit error states

100Mb/s Receive Errors

When there is no data on the cable, the receiver will see only the idle code of scrambled 1’s. If a non idle symbol is detected, the receiver looks for the SSD so that it can align the incoming message for decoding. If any 2 non consecutive zeros are detected within 10 bits, but are not the SSD symbols a false carrier indication is signalled to the MII by asserting RX_ER and setting RXD[3:0] to 1110 whilst keeping RX_DV inactive. The remainder of the message is ignored until 10 bits of 1’s are detected.

If any data is decoded after a SSD which is neither a valid data code nor an ESD, then an error is flagged by setting RX_ER active whilst the RX_DV signal is active. This also happens if 2 idle codes are detected before a

valid ESD has been received or descramble synchronisation is lost during packet reception. The states of RX_DV and RX_ER are summarised in Figure 4. RX_ER is clocked on the falling edge of RX_CLK, and will remain active for at least 1 period of RX_CLK.

RX_DV	RX_ER	RXD [3:0]	Indication
0	0	0000 through 1111	Normal inter frame
0	1	1110	False carrier indication
1	0	0000 through 1111	Normal data reception
1	1	0101 or 0110	Data reception with errors

Fig 4. 100Mb/s receive error states

CONTROLS

Initialization, mode selection and other options are governed by the control inputs and register as described in the following paragraphs.

Initialization (RESET_N)

The NWK937 incorporates a power-on-reset circuit for self-initialization on power-up. During power-on the RESET_N pin is driven low by the NWK937, all outputs are disabled and all blocks are held in their reset states. Once power -on reset has completed, RESET_N is released and must be pulled up with a 5KOhm resistor. Should RESET_N be held externally low at this point, initialisation of the NWK937 stalls. Once RESET_N goes high then initialisation of the NWK937 transceivers and digital PCS begins. The NWK937 will now respond to MDI serial interface commands, however data transmission and reception will not commence until the NWK937 has fully initialised. Whilst the initialisation sequence is in progress the NWK937 reports its reset status - bit 15 of register 0 - as a logic 1. Once initialisation has completed, register 0 bit 15 is set to a logic 0.

It will not normally be necessary for the user to reset the NWK937 because it is designed to automatically recover from fault conditions. However if required, the user may perform a full initialisation by asserting the RESET_N pin low. A reset to only the PCS sub-layer of the device may be achieved by writing bit 15 of register 0 to a logic 1.

Reset Mode

There are two types of reset in the NWK937 - hardware and software. The hardware reset is activated by setting the RESET_N pin to logic 0, and holding it low for at least 100ns. This mode causes an over-all reset in the NWK937 - both analog and digital circuitry are reset. Whilst RESET_N is low, the SPDST and FDST pins are inputs, and are used to determine the speed and duplex capability which will be advertised during auto-neg. A low on SPDST advertises 100M capability. A high on FDST advertises full duplex capability. The software reset is activated by setting bit 15 in register 0 high. This bit is a self clear bit and causes a partial reset of the device.

Following is a table summerising the different blocks to be reset and which reset will affect them:

Block	HW Reset	SW reset
management register	yes	yes
PCS state machine (RCV, XMT, ANEG)	yes	yes
XMT scrambler	yes	yes
RCV scramble	yes	yes
937 control state machine	yes	No
937 analog	yes	No

Note: Holding RESET_N low will hold the device in a static, low power state.

During both hardware and software resets, the ACTST, COLST and LNKST LED's will turn on for the duration of the reset and stay on for at least 1ms after the reset event has ended.

Low-Power Mode

This function is set via the management interface. Using MDC / MDIO, Bit 11 of register 0 is written high to put the NWK937 into Low-Power mode. In this mode the 10BASE-T and 100BASE-TX transceivers are disabled. This mode is intended to conserve power when the network connection is not required and the TXOP/TXON output is undriven.The oscillator continues to run. Both RX_CLK and TX_CLK are stopped, the RXD bus is held low and TXD, TXEN, and TXER are ignored. MDC and MDIO are still active for new commands.

Loopback Mode

Diagnostic loopback may be selected at any time by asserting setting Bit 14 in register 0. In 10BASE-T mode transmission to the TXOP/ TXON output will be stopped and the RX10 Clock Recovery will receive input from the TX10 transmit path rather than from the RXIP/RXIN inputs. In 100BASE-TX mode transmission to the TXOP/TXON output will be stopped and the RX100 Clock Recovery will receive input from the TX100 transmit path.

Repeater mode

Setting the RPTR pin high puts the NWK937 into repeater mode. In this mode the CRS will be active on receive only. In 100Mbps RPTR mode, the NWK937 is able to perform a disconnect function from the MII. This function is enabled by bit 24 in register 0. The default of this bit is 1 (enable) for repeater mode. (Note: if RPTR is low, this bit has no effect). The NWK937 will disconnect from the MII if it receives two consecutive false CRS events with no good frame in between them or if a false CRS event is longer then 480 +/- 4 bit time. If the NWK937 receives a good carrier event (480 +/- 4 bit time) or a good idle event (idle symbols for a period of 25000 to 30000 bit time) it will resume frame transfer to the MII.

A false CRS event happens if, at the beginning of a carrier event, the JK symbols are not received correctly.

When the NWK937 is in 100M mode it will count all false CRS events in register 27 bits 7:0. This counter is self cleared upon read. If a disconnect event occurs between the consecutive reads of register 27, bit 15 in the register will set high.

ICFG - Interrupt

The NWK937 offers an MII interrupt output (MINT) which can be used to interrupt the host whenever a change in link status occurs - this output is multiplexed onto either the ACTST or COLST pins, determined by the state of the ICFG input. When ICFG is high MINT replaces COLST on pin 8 and the collision LED is lost. With ICFG low MINT replaces ACTST on pin 7 and activity is now indicated on the LINKST pin 15 as follows:-

No Link - LNKST High
Link, no Activity - LNKST Low
Link, Activity - LNKST Toggles (for flashing LED)

MINT is active low by default, but may be inverted by writing bit 12 of register 24.

MINT will be asserted whenever a change in link status occurs (loss of link / gaining link). MINT will remain asserted until the controller acknowledges the interrupt by writing to register 21 (any data pattern will be accepted).
Should one or more link status changes occur between the assertion of MINT and an acknowledge then a further interrupt will be deasserted and then reasserted (min deassertion time 100ns, max 150ns).

Only a single interrupt event may be queued at any one time. Multiple status changes between acknowledge events will generate only a single queued interrupt**.**

Auto-Negotiation Enable (ANEN)

Auto-negotiation may be disabled by setting the ANEN pin low or by setting bit 12 of register 0 to zero. If auto-neg is disabled, the NWK937 will lose the link, and link will be re-established only after the 937 control state machine has determined the speed.

MII Management Interface

The management interface is the 802.3 standard 2 wire serial interface between the PHY and a management entity. The management unit controls the PHY and gathers information on the status of the PHY. It does this via the implemented registers

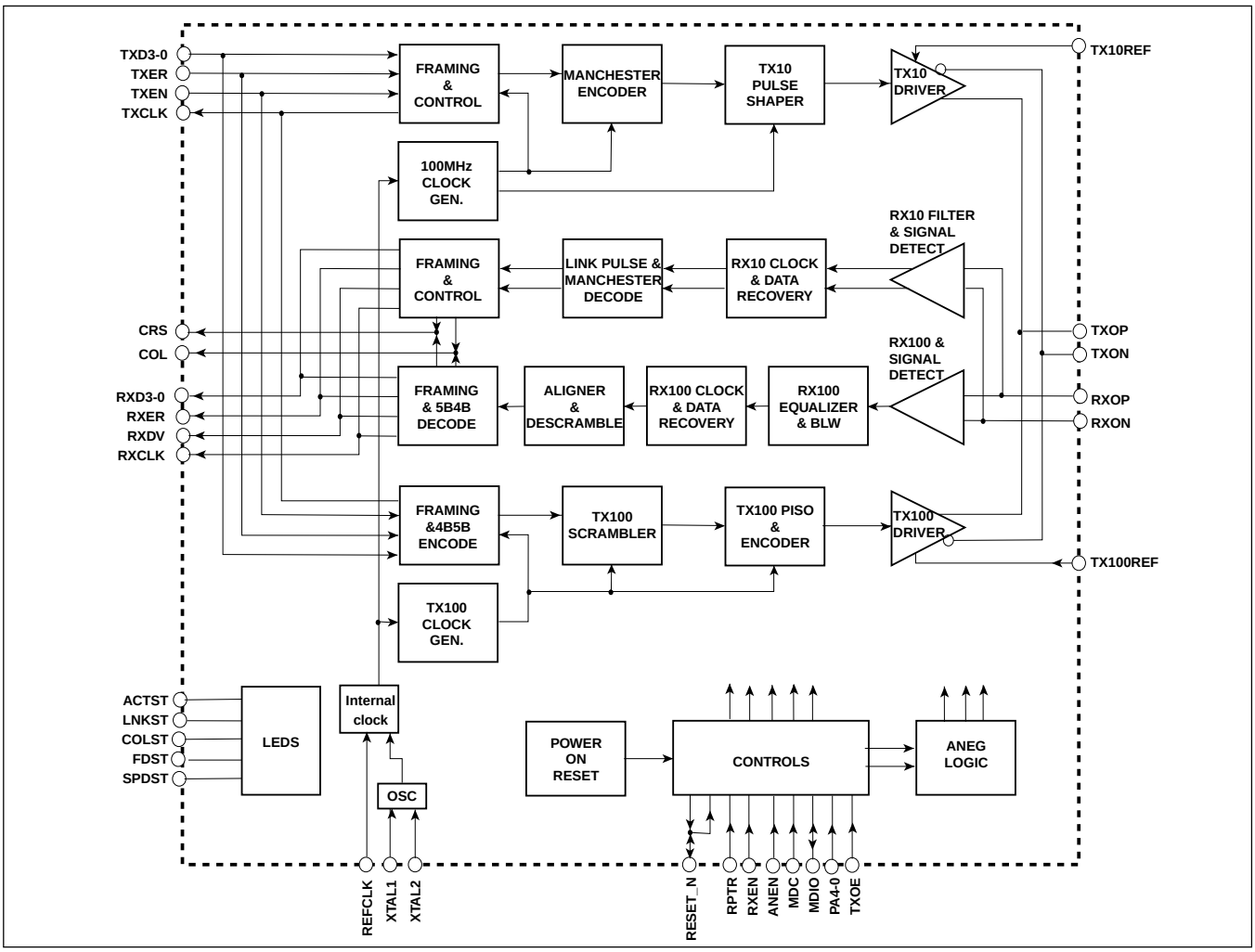

Fig.5 NWK937 block diagram

NWK937

PIN LIST

Pin #	Name	Type	Description
19	RXIN	Input	Differential receive pair from magnetics (-)
18	RXIP	Input	Differential receive pair from magnetics (+)
25	TXON	Output	100 Differential transmit pair to magnetics (-)
26	TXOP	Output	100 Differential transmit pair to magnetics (+)
33	TXREF10	Input	10BASE-T transmitter current setting pin
34	TXREF100	Input	100BASE-TX transmitter current setting pin
13	RESET_N	IOput	Active low, power on reset output and external reset input
41	XTAL1	Input	25MHz crystal input. Pull high when using REFCLK.
40	XTAL2	Input	25MHz crystal input. Leave unconnected when using REFCLK.
46	MDC	Input	Management interface clock (up to 2.5MHz)
45	MDIO	IOput	Management data
52	RX_CLK	Output	Receive clock (2.5MHz for 10, 25MHz for 100)
55, 56, 57, 58	RXD[0:4]	Output	Receive data MII interface
51	RX_DV	Output	Receive data valid. Active high.
59	RX_ER	Output	Receive error. Active high.
43	REFCLK	Input	Reference clock. Pull high when using crystal.
1	TX_CLK	Output	Transmit clock (2.5MHz for 10, 25MHz for 100)
60, 61, 62, 63	TXD[0:4]	Input	Transmit Data MII interface
3	TX_EN	Input	Transmit Enable. Active high.
64	TX_ER	Input	Transmit Error. Active high.
50	CRS	Output	Carrier sense signal. Active high.
49	COL	Output	Collision signal. Active high.
22	ANEN	Input	Auto Negotiation enable. Active high.
48	RXEN	Input	Receive enable. Active high.
21	RPTR	Input	Repeater enable. Active high.
7	ACTST / MINT	Output	Active low Receive/Transmit activity indication (LED interface) if ICFG = 1. If ICFG = 0, output is MINT and activity is indicated on the LNKST output.
8	COLST / MINT	Output	Active low collision indication (LED interface) if ICFG = 0. If ICFG = 1, output is MINT and collision indication is lost.
4	FDST	IOput	Full duplex indication when RESET_N high (LED interface). Active low. Input when RESET_N is low. High input means 937 advertises full duplex capability.
5	LNKST	Output	Active low LED interface to indicate link. If ICFG = 0, LNKST flashes to indicate activity
6	SPDST	IOput	Speed indication when RESET_N high (LED interface). High for 100Mb/s mode. Input when RESET_N is low. Low input means 937 advertises 100Mb/s.
31,30,29,16,12	PA[0:4]	Input	Phy address
23	ICFG	Input	Interrupt configuration. MINT on pin 8 when high and on pin 7 when low.
7 or 8	MINT	Output	Link status change interrupt. Default active low. Set register 24, bit 12=1 for active high interrupt

MANAGEMENT

General

The following is the register set that is implemented in the NWK937 device:

The interface to these registers is via the MDC and MDIO signals. The address of the NWK937 is specified by the PA<4:0> static inputs The MD command is issued by the MAC and can be read or write:

command	preamble	start data	op code	phy address	reg number	TA	Data
READ	32 bits of 1	01	10	5 bits	5 bits	Z0	16 bit from phy
WRITE	32 bits of 1	01	01	5 bits	5 bits	10	16 bit from MAC

SC = Self clear
RO = read only
RW = read or write
LL = latch low until register read
LH = latch high until register read

REGISTER SET

reg 0 - control register

Bit	Bit name	description	Default	R/W
0.15	Reset	1 = PHY reset 0 = Normal operation	0	RW SC
0.14	Loopback	1 = Loopback mode active 0 = Normal operation	0	RW
0.13	Speed selection	1 = 100 Mbps 0 = 10 Mbps	1	RW
0.12	ANEG enable	1 = Enable ANEG process 0 = Disable ANEG process	1	RW
0.11	Power down	1 = Power down active 0 = Normal operation	0	RW
0.10	Isolation	1 = isolation in process 0 = Normal operation	0	RW
0.9	Restart ANEG	1 = Restart the ANEG process 0 = Normal operation	0	RW SC
0.8	Duplex selection	1= Full Duplex mode 0 = Half duplex mode	1	RW
0.7	Collision test	1 = Collision test active 0 = Normal operation	0	RW
0.6:0	Reserved	Write as 0 ignore on read.		

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reg 1- status register

Bit	Bit name	description	Default	R/W
1.15	100BaseT4	1 = PHY able to perform 100BaseT4 0 = PHY not able to perform 100BaseT4	0	RO
1.14	100BASE-TX - FDX	1 = PHY able to perform 100BASE-TX 0 = PHY not able to perform 100BASE-TX	1	RO
1.13	100BASE-TX - HDX	1 = PHY able to perform 100BASE-TX 0 = PHY not able to perform 100BASE-TX	1	RO
1.12	10BASE-T - FDX	1 = PHY able to perform 10BASE-T 0 = PHY not able to perform 10BASE-T	1	RO
1.11	10BASE-T - HDX	1 = PHY able to perform 10BASE-T 0 = PHY not able to perform 10BASE-T	1	RO
1.10	100BaseT2 - FDX	1 = PHY able to perform 100BaseT2 0 = PHY not able to perform 100BaseT2	0	RO
1.9	100BaseT2 - HDX	1 = PHY able to perform 100BaseT2 0 = PHY not able to perform 100BaseT2	0	RO
1.8:7	Reserved	ignore when read	0	RO
1.6	MF preamble suppression	1= Phy accept management frames with short preamble 0 = normal preamble only	0	RO
1.5	ANEG complete	1 = ANEG process completed 0 = ANEG process not completed or not active	0	RO
1.4	Remote fault	1= Remote fault condition detected 0 = no Remote fault condition detected	0	RO LH
1.3	ANEG able	1 = Phy is able to perform ANEG 0 = Phy is not able to perform ANEG	1	RO
1.2	Link status	1= Link is up 0 = Link is down	0	RO LL
1.1	Jabber detect	1 = jabber condition detected 0 = normal operation	0	RO
1.0	Extended regs	1 = extended register capability 0 = no extended registers	1	RO

reg 2/3- NWK937 Identifier register

Bit	Bit name	description	Default	R/W
2.15:0	OUI	Mitel OUI bits	0282	RO
3.15:0	OUI/device ID	Mitel OUI bits and device code	1C53	RO

reg 4- ANEG advertisement register

Bit	Bit name	description	Default	R/W
4.15	NP	Next page able - the NWK937 is not able to perform next page	0	RO
4.14	reserved		0	RO
4.13	remote fault	0 = no remote fault detected 1= a remote fault been detected	0	R/W
4.12:10	reserved		0	R/W
4.9:5	Technology	T4, 100Fdx, 100Hdx, 10Fdx, 10Hdx	0F	R/W
4.4:0	selector field		01	R/W

reg 5- ANEG link partner ability register

Bit	Bit name	description	Default	R/W
5.15	NP	partner is next page capable	0	RO
5.14	ACK	partner sent an acknowledge bit	0	RO
5.13	remote fault	partner detected a remote fault	0	RO
5.12:5	ability	partner's technology ability	0	RO
5.4:0	selector field	partner selector field	0	RO

reg 6- ANEG expansion register

Bit	Bit name	description	Default	R/W
6.15:5	reserved		0	RO
6.4	parallel detect fault	1 = a fault has been detected 0 = aneg process finished. no fault detected	0	RO LH
6. 3	link partner next page able	0 = Link partner is not next page able 1 = Link partner is next page able	0	RO
6.2	next page able	0 = NWK937 is not able for next page	0	RO
6.1	Page received	0 = no new page been received 1= a new page has been received and is in reg 5	0	RO LH
6.0	link partner aneg able	0 = Link partner is not aneg able 1 = Link partner is aneg able	0	RO

reg 16-TX100 test reg

Bit	Bit name	description	Default	R/W
16.15:0	reserved	test mode only	0000	res

reg 17-RX100 test reg

Bit	Bit name	description	Default	R/W
17.15:0	reserved	test mode only		

reg 18-TX10 test reg

Bit	Bit name	description	Default	R/W
18.15:0	reserved	test mode only	0000	res

reg 19-RX10 test reg

Bit	Bit name	description	Default	R/W
19.15:0	reserved	test mode only	0000	res

reg 20-CONTROL test reg

Bit	Bit name	description	Default	R/W
20.15:0	reserved	test mode only	0000	res

reg 21-Interrupt Handshake Reg

Bit	Bit name	description	Default	R/W
21.15.0	clear INT	clears MINT output	0000	WO

reg 24- NWK937 specific register

Bit	Bit name	description	Default	R/W
24.15: 14	test access	reserved Mitel test access only	00	RW
24.13:	LED control	0 = COLST active on Collision 1 = COLST active on Sync/polarity	0	RW
24. 12	MINT POL	0 = MINT output active low 1 = MINT output active high	0	RW
24.11	Pol Dis	disable 10BASE-T autopolarity correction	0	RW
24.10	SQE disable	0 = SQE generation (normal operation) 1 = no SQE generation	0	RW
24.9	JAB disable	0 = in case of jabber the 10BASE-T will cut the frame (normal operation) 1 = Jabber function disable	0	RW
24. 8	loop 10	disable loopback of TX to RX in 10BASE-T half duplex	0	RW
24.7	Force RX	Force reception regardless of link	0	RW
24.6	Force TX	Force transmission regardless of link	0	RW
24.5	CRS_CTL	CRS behavior in FDX - 0 = CRS is active during transmission only 1= CRS active during reception and transmission	0	RW
24.4	MF	0 = normal operation 1 = disable the MD preamble function	0	RW
24.3	Byp ALIGN	0 = normal operation 1 = bypass the aligner function	0	RW
24.2	Byp ENC	0 = normal operation 1 = bypass the 4B5B encoder function	0	RW
24.1	Byp SCR	0 = normal operation 1 = bypass the scrambler function	0	RW
24.0	DISCEN	disconnect mechanism enable	0 - DTE 1- RPT	

reg 25 - ANEG status

Bit	Bit name	description	Default	R/W
25.15	reserved	test mode only - do not set high	0	RW
25.14	reserved	test mode only - do not set high	0	RW
25.13	Pol	10BASE-T polarity sense	0	RO
25.12:8	PA	PHY address	PA<4:0>	RO
25.7	aneg complete	0 = aneg completed 1 = aneg did not complete (same as 1.5)	0	RO
25.6	Duplex	ANEG result - duplex operation 0 = HDX, 1 = FDX	0	RO
25.5	speed	ANEG result - speed of operation 0 = 10, 1 = 100	0	RO
25.4	ability mtc	1 = abilities matched	0	RO
25.0:3	ANEG state	ANEG state machine current state	0	RO

reg 26 - Symbol error counter

Bit	Bit name	description	Default	R/W
26.15:0	RX_ERR counter	number of RX_ERR events since last read - clears either in change of speed or read of this reg.	0	RO SC

reg 27 - False carrier event counter

Bit	Bit name	description	Default	R/W
27.15	disconnect	the disconnect mechanism status	0	RO LH
27.14:8	reserved		0	RO
27.7:0	false CRS counter	number of False CRS events since last read. Active only in repeater 100 mode.	0	RO SC

reg 28 - Counter test register

Bit	Bit name	description	Default	R/W
28.15:0	reserved	test mode only	0000	res

OPERATING CONDITIONS

Supply voltage	+4.75V to 5.25V
Ambient temperature	0°C to +70°C

DC ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Value Max.	Units	Conditions
DC parameters - input					
High level input voltage	V_{IH}	2	V_{DD}	V	
High level input voltage	V_{IL}	V_{SS}	0.8	V	
High level input current	I_{IH}	-	1	µA	
High level input current	I_{IL}	-	–1	µA	no pull up
Pin capacitance to ground		-	8	pF	including package
DC parameters - output -6mA buffers					
High level output voltage	V_{OH}	4	V_{DD}	V	
High level output voltage	V_{OL}	V_{SS}	0.4	V	
High level output current	I_{OH}	-	–6	mA	
High level output current	I_{OL}	-	6	mA	
Rise time		-	4	nS	0.4V to 2.4V into 20pF load
Fall time		-	4	nS	0.4V to 2.4V into 20pF load
Pin capacitance to ground		-	8	pF	

DIFFERENTIAL OUTPUT

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min.	Value Max.	Units	Conditions
High level		2	-	V	
Zero level		–50	50	mV	
Low level		-	–2	V	
Slew rate		-	0.5	V/ns	

AC ELECTRICAL CHARACTERISTICS

Recommended operating conditions apply except where stated.

Characteristic	Symbol	Value Min	Value Max	Units	Conditions
REFCLK					
Frequency		25±100ppm		MHz	
Duty cycle		45	55	%	
RXCLK					
Frequency		25±100ppm		MHz	100Mbs mode
Duty cycle		40	60	%	100Mbs mode
Frequency		2.5±100ppm		MHz	10Mbs mode
Duty cycle		40	60	%	10Mbs mode
TXCLK					
Frequency		25±100ppm		MHz	100Mbs mode
Duty cycle		40	60	%	100Mbs mode
Frequency		2.5±100ppm		MHz	10Mbs mode
Duty cycle		40	60	%	10Mbs mode
MDC					
Frequency		-	2.5	MHz	
Minimum high/low		160	- ns		
Supply Current		**Max**			
10 Base-T Idle		90		mA	Measured at
10 Base-T Active		180		mA	5V, Room Temperature
100 Base TX mode		120		mA	These Figures include the
Auto Negotiation		90		mA	current flowing in the
Low Power		35		mA	Transmit load resistors

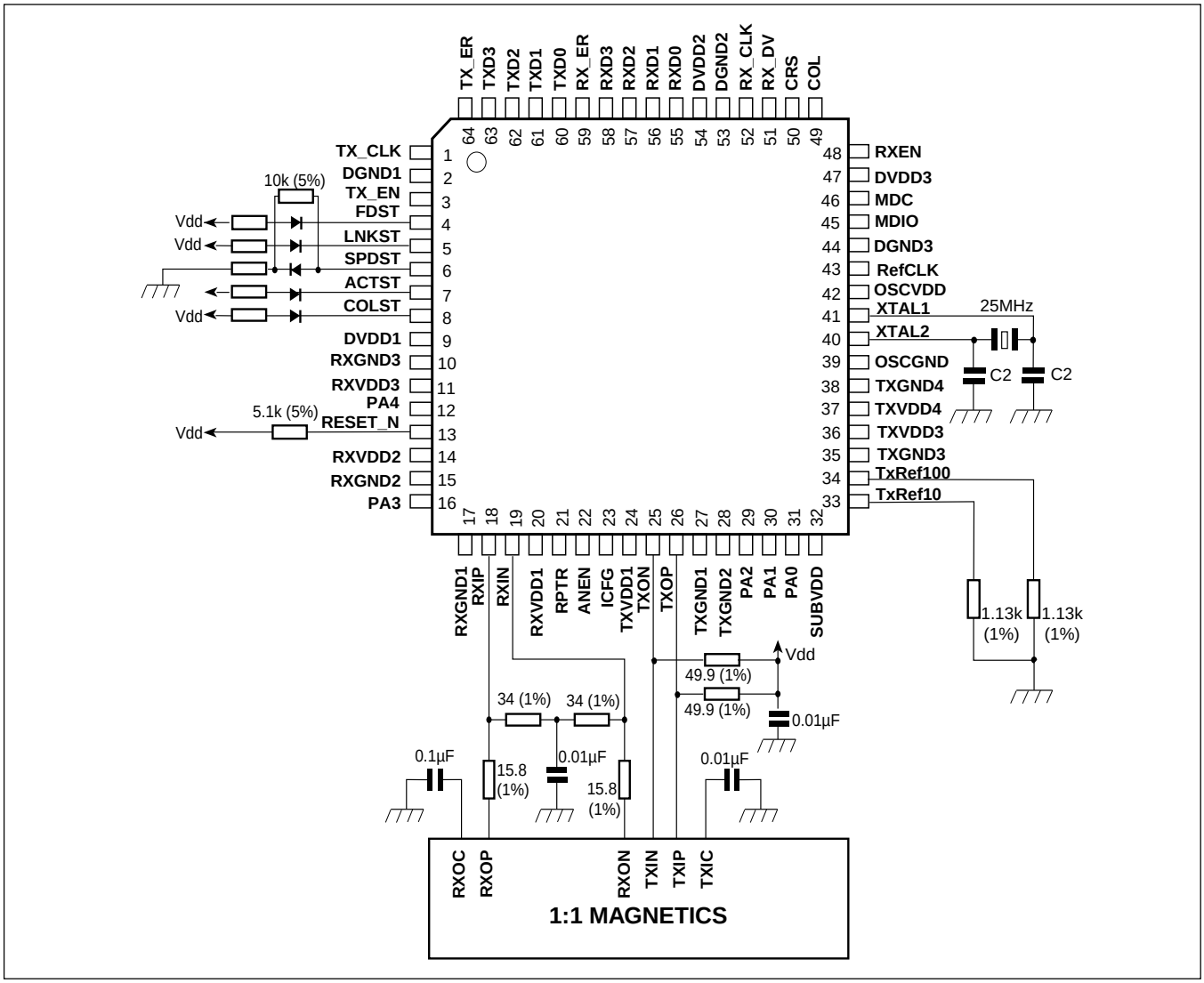

Fig.6 External components

EXTERNAL COMPONENTS

Connecting an External 25MHz Reference

If an external clock is used then it should be driven into the REFCLK input, and XTAL1 must be connected to OSCVDD. XTAL2 must be left unconnected.

RESET_N Pull-up Resistor

This resistor is required regardless of whether RESET_N is used externally.

RX Input Decoupling

The method of using a split input load resistor and de-coupling the centre tap reduces common mode noise.

Crystal Oscillator

For IEEE802.3 compliance the oscillator must run at 25MHz ±100ppm. The NWK937 on-chip circuitry contributes less than 40ppm variability to the oscillator frequency, therefore the crystal must be specified to 60ppm. This must include variations due to temperature and ageing. The crystal must be capable of dissipating 500uW of power.

External capacitors are required on the XTAL1 & XTAL2 pins. These should be chosen according to the crystal manufacturer's recommendations.

Tracking to the crystal and the capacitors must be as short as possible. Other signal paths must not cross the area.

The NWK937 is supported by magnetics from the following vendors:

VENDOR	MAGNETICS
Bel	S558-5999-46
Pulse	H1012
Valor	ST6118

For more information about all Zarlink products visit our Web Site at

www.zarlink.com