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Advance

512Kx16bit Ultra-Low Power Asynchronous Static RAM

Overview

The N08T16xxC2A, is a family of integrated memory devices containing a low power 8 Mbit SRAM built using a self-refresh DRAM array organized as 524,288 words by 16 bits. It is designed to be identical in operation and interface to standard 6T SRAMS. The device is designed for low standby and operating current and includes a power-down feature to automatically enter standby mode. The device is designed with a separate Vcc and VccQ power structure for the I/O to be run from a separate power supply from the device core. The VFBGA package offers an extremely thin, low-profile size for today's space conscience applications.

Features

- **Voltage Ranges:**
  1.70 to 2.25 Volts - N08T1618C2A
  2.30 to 2.70 Volts - N08T1625C2A
  2.70 to 3.30 Volts - N08T1630C2A
- **Extended Temperature Range:**
  -25 to +85 ^{o}C
- **Fast Cycle Time:**
  T_{ACC} < 55 nS @ 2.75V
  T_{ACC} < 70 nS @ 2.3V
  T_{ACC} < 85 nS @ 1.70V
- **Low Operating Current:**
  I_{CC} < 25 mA at 55nS
  I_{CC} < 20 mA at 70nS
  I_{CC} < 15 mA at 100nS
- **Low Standby Current:**
  I_{SB} < 30 uA at 1.8V
  I_{SB} < 50 uA at 2.5V
- **48-Pin VFBGA package or wafer level die**
- **Dual rail operation**
  V_{CCQ} and V_{SSQ} for separate I/O power rail

FIGURE 1: Pin Description

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CE2/$\overline{ZZ}$
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CE1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SSQ}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CCQ}	I/O_{12}	DNU	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	A_{18}	A_8	A_9	A_{10}	A_{11}	NC

48 Pin VFBGA (top)
6 x 8 mm

Two options:
1) Two CE - ball A6 is CE2
2) One CE with sleep mode - ball A6 is $\overline{ZZ}$

TABLE 1: Pin Descriptions

Pin Name	Pin Function
A_0 - A_{18}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CE1}$, CE2	Chip Enable Inputs
$\overline{ZZ}$	Deep Sleep Mode
$\overline{OE}$	Output Enable Input
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
I/O_0 - I/O_{15}	Data Inputs/Outputs
V_{CC}/V_{CCQ}	Core Power / IO Power
V_{SS}/V_{SSQ}	Ground / IO Ground
DNU	Do Not Use (or connect to V_{SS})

FIGURE 3: Functional Block Diagram

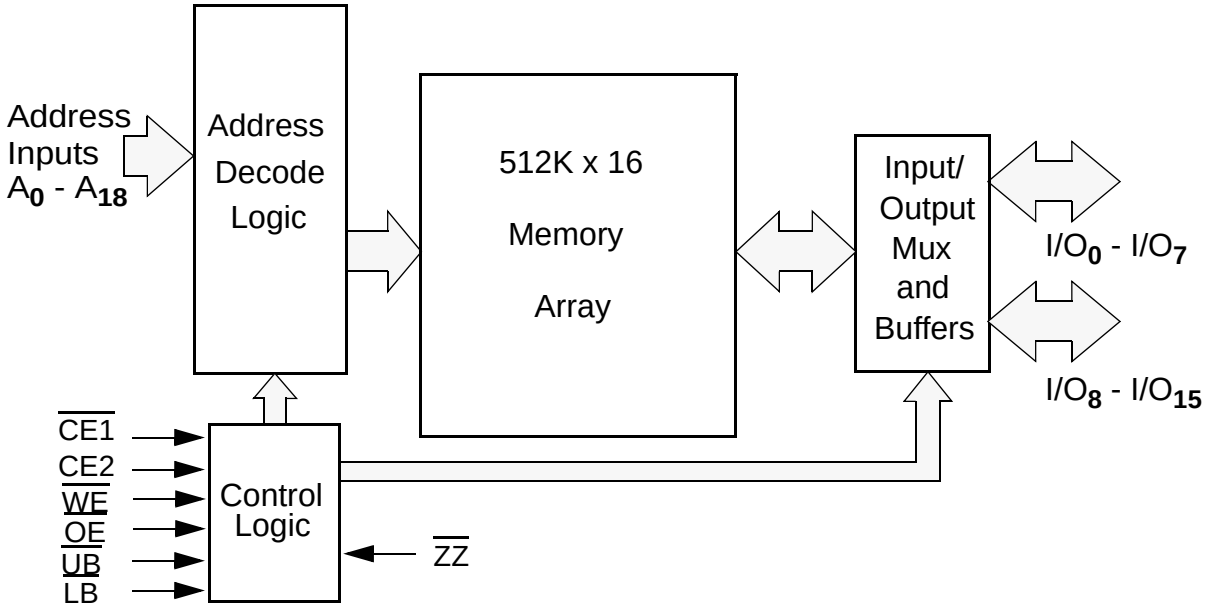


TABLE 2: Functional Truth Table

$\overline{CE1}$	CE2 [1]	$\overline{WE}$	$\overline{OE}$	$\overline{UB}/\overline{LB}$	$\overline{ZZ}$ [2]	I/O[3]	MODE	POWER
H	X	X	X	X	H	High Z	Standby[4]	Standby
X	L	X	X	X	H	High Z	Standby[4]	Standby
X	X	X	X	H	H	High Z	Standby[4]	Standby
L	H	L	X[5]	L[3]	H	Data In	Write[5]	Active -> Standby[6]
L	H	H	L	L[3]	H	Data Out	Read	Active -> Standby[6]
L	H	H	H	L[3]	H	High Z	Active	Standby[6]
X	-	X	X	X	L	High Z	Deep Sleep	Deep Sleep

1. Only on the two-CE option device.
2. Only on the one-CE option device with sleep mode.
3. When $\overline{UB}$ and $\overline{LB}$ are in select mode (low), I/O_0 - I/O_{15} are affected as shown. When $\overline{LB}$ only is in the select mode only I/O_0 - IO_7 are affected as shown. When $\overline{UB}$ is in the select mode only I/O_8 - I/O_{15} are affected as shown. If both $\overline{UB}$ and $\overline{LB}$ are in the deselect mode (high), the chip is in a standby mode regardless of the state of $\overline{CE1}$ or CE2.
4. When the device is in standby mode, control inputs ($\overline{WE}$, $\overline{OE}$, $\overline{UB}$, and $\overline{LB}$), address inputs and data input/outputs are internally isolated from any external influence and disabled from exerting any influence externally.
5. When $\overline{WE}$ is invoked, the $\overline{OE}$ input is internally disabled and has no effect on the circuit.
6. The device will consume active power in this mode whenever addresses are changed. Data inputs are internally isolated from any external influence.

TABLE 3: Capacitance*

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF
I/O Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		8	pF

* These parameters are verified in device characterization and are not 100% tested

TABLE 4: Absolute Maximum Ratings*

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	$V_{IN,OUT}$	–0.3 to V_{CC}+0.3	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	–0.3 to +4.0	V
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	-40 to +125	^oC
Operating Temperature	T_A	-25 to +85	^oC
Soldering Temperature and Time	T_{SOLDER}	240 ^oC, 10sec(Lead only)	^oC

* Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 5: Operating Characteristics (Over specified Temperature Range)

Item	Symbol	Test Conditions	Device	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		N08T1618C2A	1.70	1.80	2.25	V
			N08T1625C2A	2.3	2.5	2.7	
			N08T1630C2A	2.7	3.0	3.3	
Data Retention Voltage	V_{DR}			1.7		3.3	V
Input High Voltage	V_{IH}			1.4		V_{CC}+0.5	V
Input Low Voltage	V_{IL}			–0.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = 0.2mA		0.8V_{CC}			V
Output Low Voltage	V_{OL}	I_{OL} = -0.2mA				0.2V_{CC}	V
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}				0.5	µA
Output Leakage Current	I_{LO}	$\overline{OE}$ = V_{IH} or Chip Disabled				0.5	µA
Read/Write Operating Supply Current[1]	I_{CC1}	V_{IN} = V_{IH} or V_{IL} Chip Enabled, Iout = 0 f= fmax				25	mA
Read/Write Quiescent Operating Current[2]	I_{CC3}	V_{IN} = V_{CC} or 0V Chip Enabled, Iout = 0 f = 0				150	µA
Standby Current [2]	I_{SB30}	V_{IN} = V_{CC} or 0V Chip Disabled, t_A= 30^oC	N08T1618C2A			tbd	µA
			N08T1625C2A			tbd	
			N08T1630C2A			tbd	
Max Standby Current[2]	I_{SB85}	V_{IN} = V_{CC} or 0V Chip Disabled, t_A= 85^oC	N08T1618C2A			30	µA
			N08T1625C2A			50	
			N08T1630C2A			70	

1. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.
2. This device assumes a standby mode if the chip is disabled ($\overline{CE1}$ high or CE2 low or $\overline{UB}$ and $\overline{LB}$ high). It will also automatically go into a standby mode whenever all input signals are quiescent (not toggling) regardless of the state of $\overline{CE1}$, CE2, $\overline{UB}$ and $\overline{LB}$. In order to achieve low standby current all inputs must be within 0.2 volts of either VCC or VSS.
3. The Chip is Disabled when $\overline{CE1}$ is high or CE2 is low or when both $\overline{UB}$ and $\overline{LB}$ are high. The Chip is Enabled when $\overline{CE1}$ is low and CE2 is high and $\overline{UB}$ or $\overline{LB}$ are low.

TABLE 6: Timing Test Conditions

Item	
Input Pulse Level	$0.1V_{CC}$ to $0.9\ V_{CC}$
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	$0.5\ V_{CC}$
Operating Temperature	-10 to +85 ^{o}C

FIGURE 4: Output Load Circuit

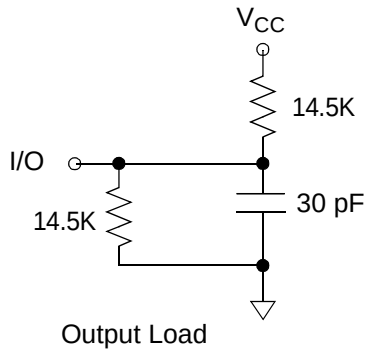


TABLE 7: Read Cycle Timing (1) $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2, $\overline{WE}$ = V_{IH}

Item	Symbol	1.8		2.5		3.0		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		70		55		nS
Address Access Time	t_{AA}		85		70		55	nS
Output Hold from Address Change	t_{OH}	5		5		5		nS

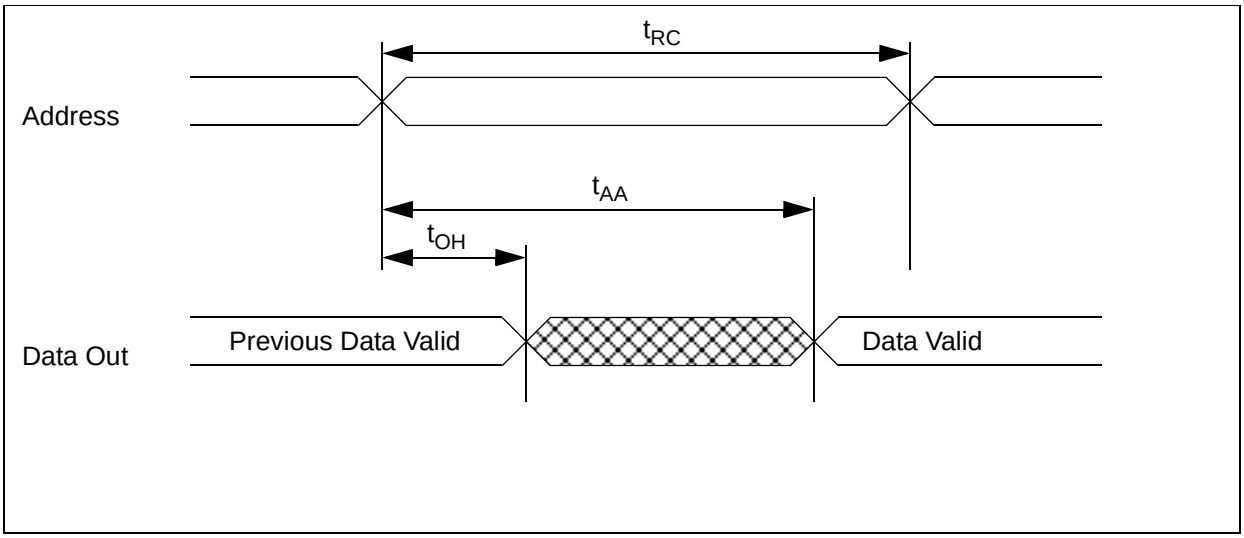


FIGURE 5: Timing Waveform of Read Cycle (2) ($\overline{WE}$ = V_{IH})

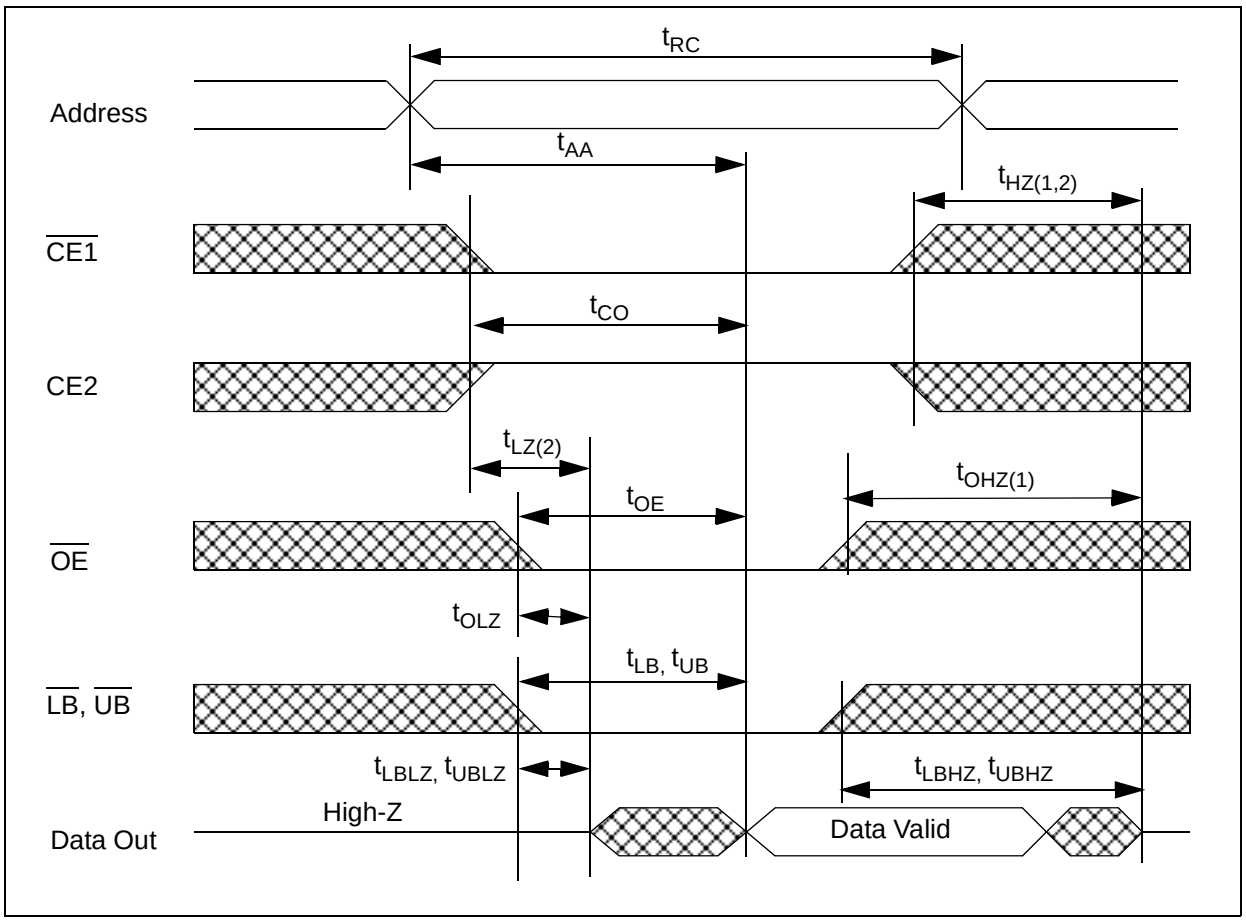


TABLE 8: Read Cycle Timing (2) WE = V_{IH}

Item	Symbol	1.8		2.5		3.0		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85	-	70	-	55	-	nS
Address Access Time	t_{AA}	-	85	-	70	-	55	nS
Chip Enable to Valid Output	t_{CO}	-	85	-	70	-	55	nS
Output Enable to Valid Output	t_{OE}	-	15	-	15	-	15	nS
Byte Select to Valid Output	t_{LB}, t_{UB}	-	85	-	70	-	55	nS
Chip Enable to Low-Z output	t_{LZ}	10	-	10	-	10	-	nS
Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	5	-	nS
Byte Select to Low-Z Output	t_{LBZ}, t_{UBZ}	10	-	10	-	10	-	nS
Chip Enable to High-Z Output	t_{HZ}	0	20	0	20	0	20	nS
Output Disable to High-Z Output	t_{OHZ}	0	20	0	20	0	20	nS
Byte Select Disable to High-Z Output	t_{LBHZ}, t_{UBHZ}	0	20	0	20	0	20	nS
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	nS

FIGURE 6: Timing Waveform of Write Cycle (1) ($\overline{WE}$ control)

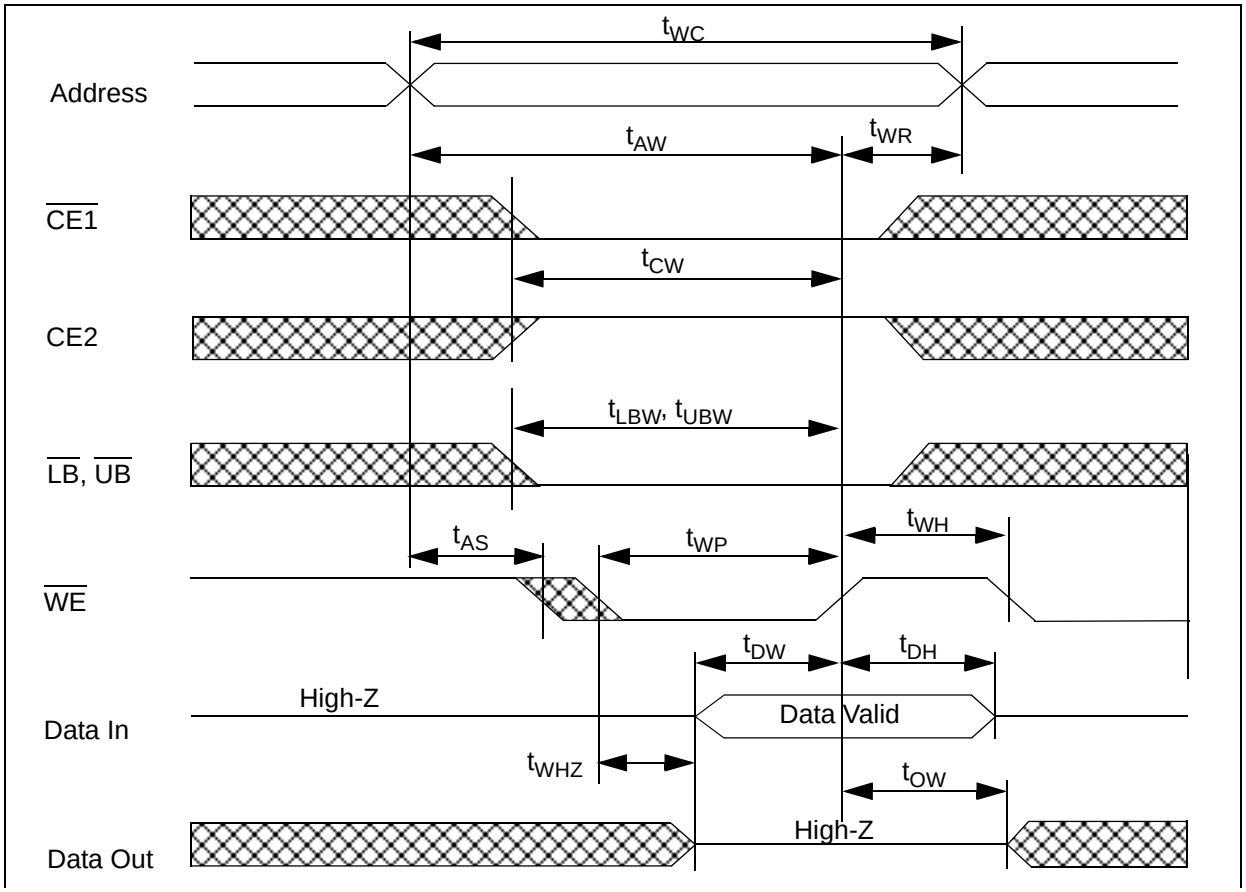
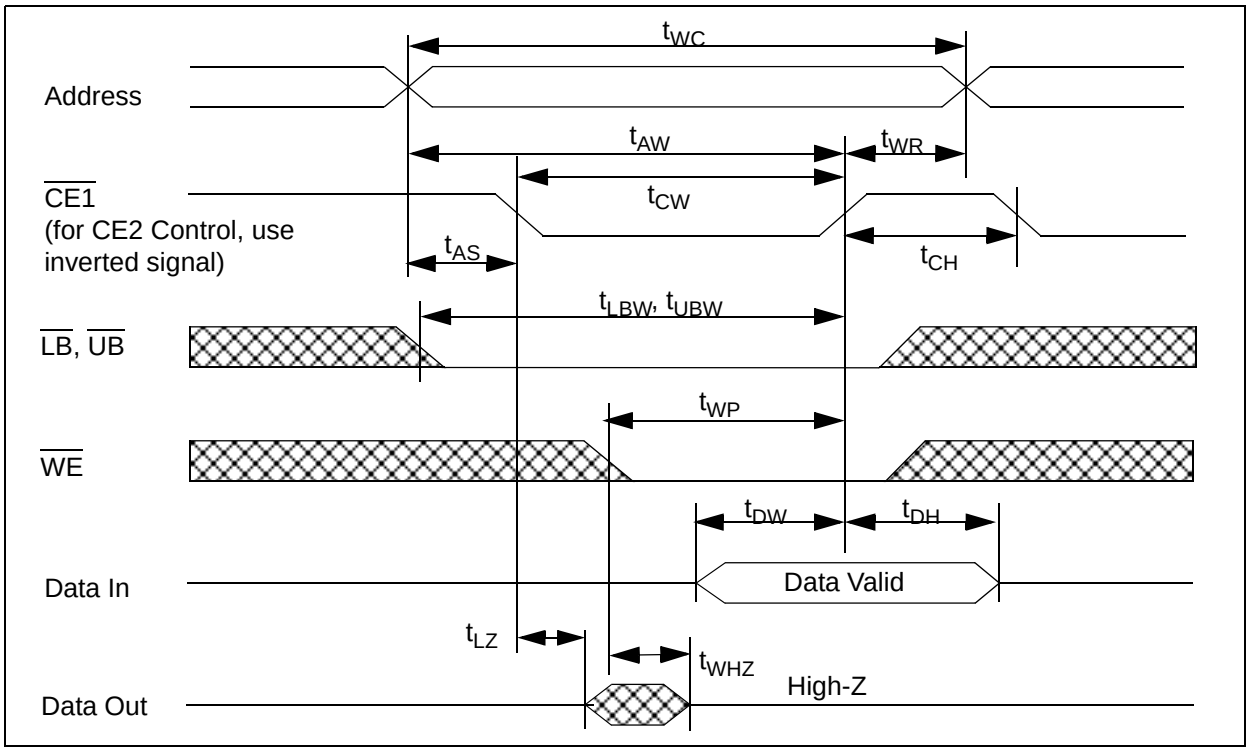


TABLE 9: Write Cycle Timing

Item	Symbol	1.8		2.5		3.0		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85	-	70	-	55	-	nS
Chip Enable to End of Write	t_{CW}	85	-	70	-	55	-	nS
Chip Enable High	t_{CH}	5		5		5		
Address Valid to End of Write	t_{AW}	85	-	70	-	55	-	nS
Byte Select to End of Write	t_{LBW}, t_{UBW}	85	-	70	-	55	-	nS
Write Pulse Width	t_{WP}	65	1000	55	1000	45	1000	nS
Write Pulse High	t_{WH}	5		5		5		
Write Recovery Time	t_{WR}	0	-	0	-	0	-	nS
Write to High-Z Output	t_{WHZ}	-	20	-	20	-	20	nS
Address Setup Time	t_{AS}	0	-	0	-	0	-	nS
Data to Write Time Overlap	t_{DW}	25	-	25	-	25	-	nS
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	nS
End Write to Low-Z Output	t_{OW}	5	-	5	-	5	-	nS

FIGURE 7: Timing Waveform of Write Cycle (2) ($\overline{CE1}$ Control)



Power Savings Mode

The N08T16xxC2A contains an optional power savings mode, deep sleep mode.

Deep Sleep Mode

This power savings mode is available only on the single CE device, which has a $\overline{ZZ}$ (Deep Sleep Mode) input pin.

In this mode of operation, the internal refresh is turned off and all data integrity of the array is lost. Deep Sleep is entered by bringing $\overline{ZZ}$ low. The device will remain in this mode as long as $\overline{ZZ}$ remains low. Timings are defined to enter and exit the deep sleep mode of operation.

FIGURE 8: Deep Sleep Mode - Entry/Exit Timings

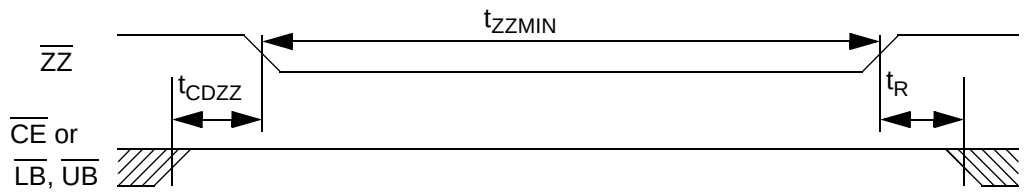
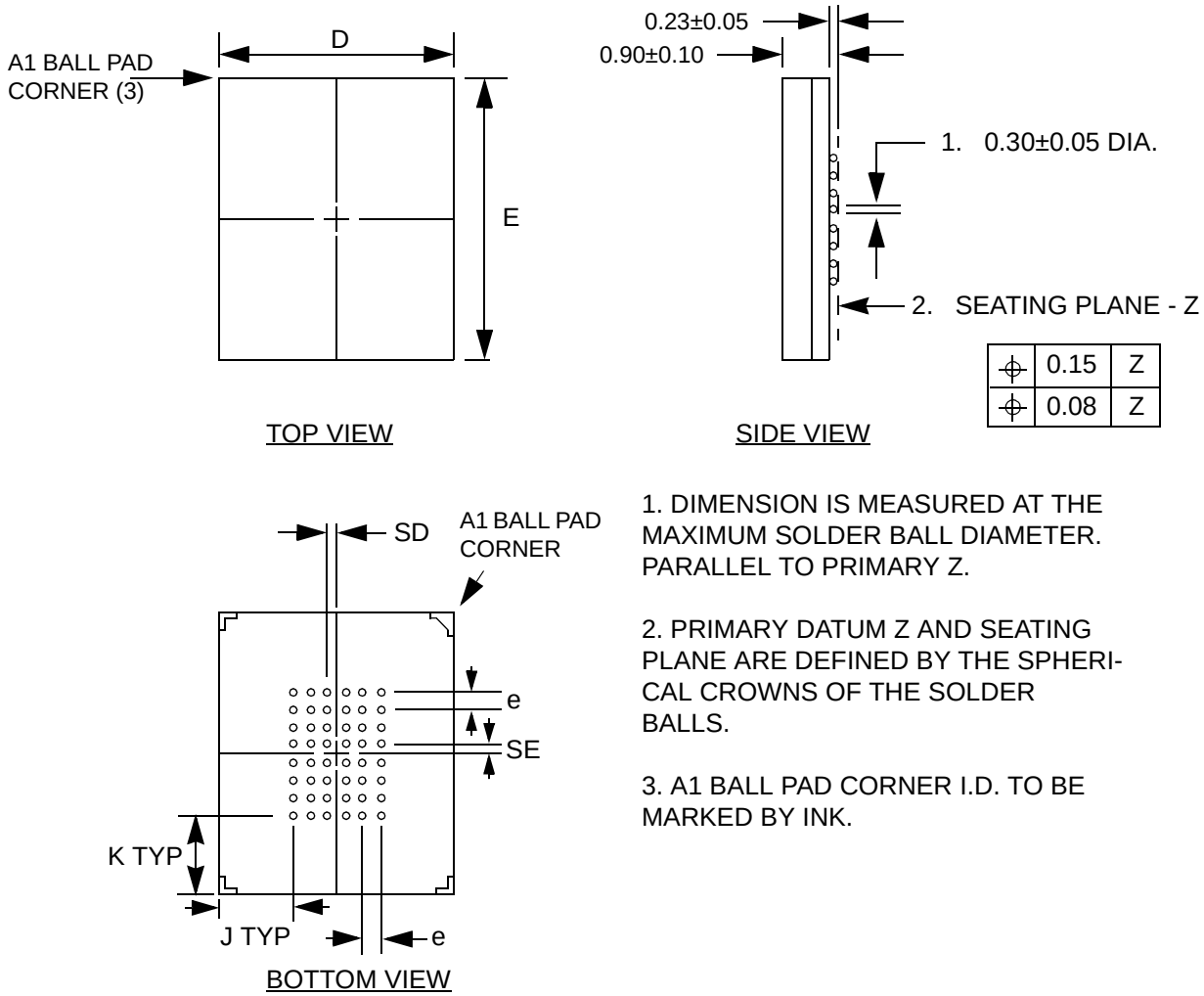


Table 10: Deep Sleep Timings and Current

Item	Symbol	Min	Max	Unit
Chip ($\overline{CE}$, $\overline{UB}$/$\overline{LB}$) deselect to ZZ low	t_{cdzz}	0		ns
Deep Sleep Mode	t_{zzmin}	10		us
Deep Sleep Recovery	t_r	200		us
Deep Sleep Current	I_{ZZ}		10	uA

FIGURE 9: BALL GRID ARRAY PACKAGING



1. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER. PARALLEL TO PRIMARY Z.

2. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

3. A1 BALL PAD CORNER I.D. TO BE MARKED BY INK.

TABLE 11: Dimensions (mm)

D	E	e = 0.75				BALL MATRIX TYPE
		SD	SE	J	K	
6±0.10	8±0.10	0.375	0.375	1.125	1.375	FULL

TABLE 12: Revision History

Revision	Date	Change Description
A	5/15/2002	Initial 8Mb datasheet

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