NanoAmp Solutions, Inc.
1982 Zanker Road, San Jose, CA 95112
ph: 408-573-8878, FAX: 408-573-8877
www.nanoamp.com

N02C1630E1AM

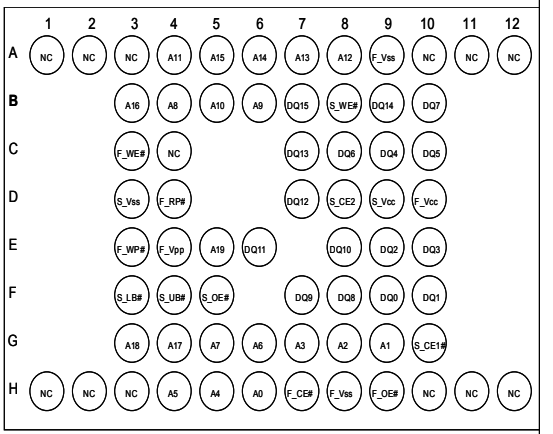
Low Voltage, Extended Temperature

FLASH AND SRAM COMBO MEMORY

FEATURES

- Organization: 1,048K x 16 (Flash)
  128K x 16 (SRAM)
- Basic configuration:
  Flash
  Thirty-nine erase blocks
  – Eight 4K-word parameter blocks
  – Thirty-one 32K-word main memory blocks
  SRAM
  2Mb SRAM for data storage
  – 128K-words
- F_V_{CC}, F_V_{PP}, S_V_{CC} voltages
  2.7V (MIN)/3.3V (MAX) F_V_{CC} read voltage
  2.7V (MIN)/3.3V (MAX) S_V_{CC} read voltage
  1.8V (TYP) F_V_{PP} (in-system PROGRAM/ERASE)
  12V ±5% (HV) F_V_{PP} (production programming compatibility)
  1.0V (MIN) S_V_{CC} (SRAM data retention)
- Asynchronous access time
  Flash access time: 90ns @ 2.7V F_V_{CC}
  SRAM access time: 85ns @ 2.7V S_V_{CC}
- Low power consumption
- Enhanced WRITE/ERASE suspend option
- Read/Write SRAM during program/erase of Flash
- 128-bit chip OTP protection register for security purposes
- Cross-compatible command set support
- PROGRAM/ERASE cycles
  100,000 WRITE/ERASE cycles per block

BALL ASSIGNMENT
66-Ball FBGA (Top View)



OPTIONS — MARKING

- Timing
  90ns — -9
- Boot Block
  Top — T
  Bottom — B
- Operating Temperature Range
  Industrial Temperature (-40°C to +85°C) — I

Part Number Example:
N02C1630E1AM-9TI

GENERAL DESCRIPTION

The N02C1630E1AM, a combination of Flash and SRAM memory, provides a compact, low-power solution for systems where PCB real estate is at a premium. The device contains a nonvolatile, electrically block-erasable (flash), programmable, read-only memory containing 16,777,216 bits organized as 1,048,576 words (16 bits).

The device also provides soft protection for blocks by configuring soft protection registers with dedicated command sequences. A 128-bit (OTP)one time programmable register is provided.

The embedded WORD WRITE and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). The WSM simplifies these operations and relieves the system processor of secondary tasks. An on-chip status register, can be used to monitor the WSM status to determine the progress of a PROGRAM/ERASE command.

The erase/program suspend functionality allows compatibility with existing EEPROM emulation software packages.

The device takes advantage of a dedicated power source for the Flash device (F_V_{CC}) and a dedicated power source for the SRAM device (S_V_{CC}), both at 2.7V–3.3V for optimized power consumption and improved noise immunity. The separate S_V_{CC} pin for the SRAM provides the data retention capability whenever required. The data retention S_V_{CC} is specified as low as 1.0V. The device supports two V_{PP} voltages; in-circuit V_{PP} of 1.65V–3.3V and production compatibility of 12V ±5%. The 12V ±5% V_{PP} is supported for a maximum of 100 cycles and 10 cumulative hours.

The N02C1630E1AM contains an asynchronous 2Mb SRAM organized as 128K-words by 16 bits. This device is fabricated using an advanced CMOS process and high-speed/ultra-low-power circuit technology.

The N02C1630E1AM is packaged in a 66-ball FBGA package with 0.80mm pitch.

PART NUMBERING INFORMATION

NanoAmp's low-power devices are available with several different combinations of features. Valid combinations of features and their corresponding part numbers are listed in Table 1.

Part Number Chart

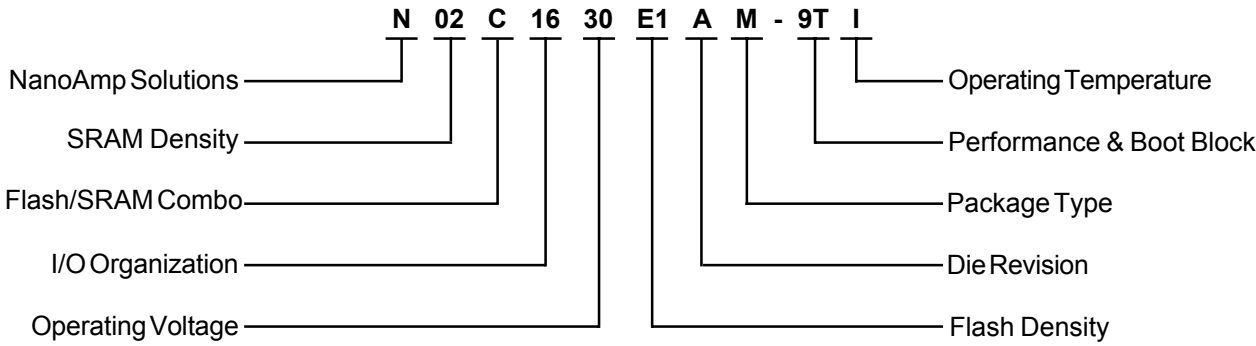
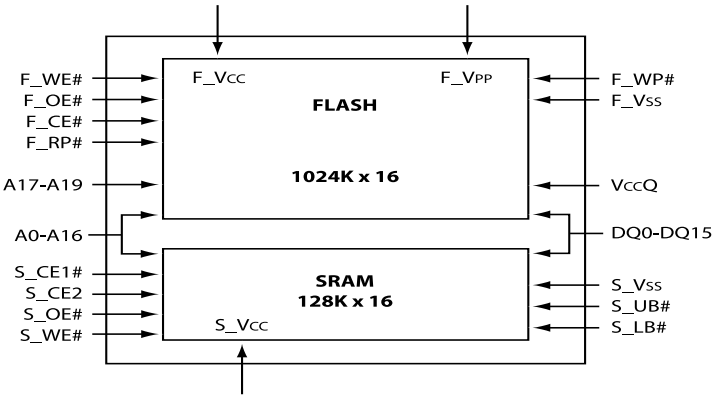


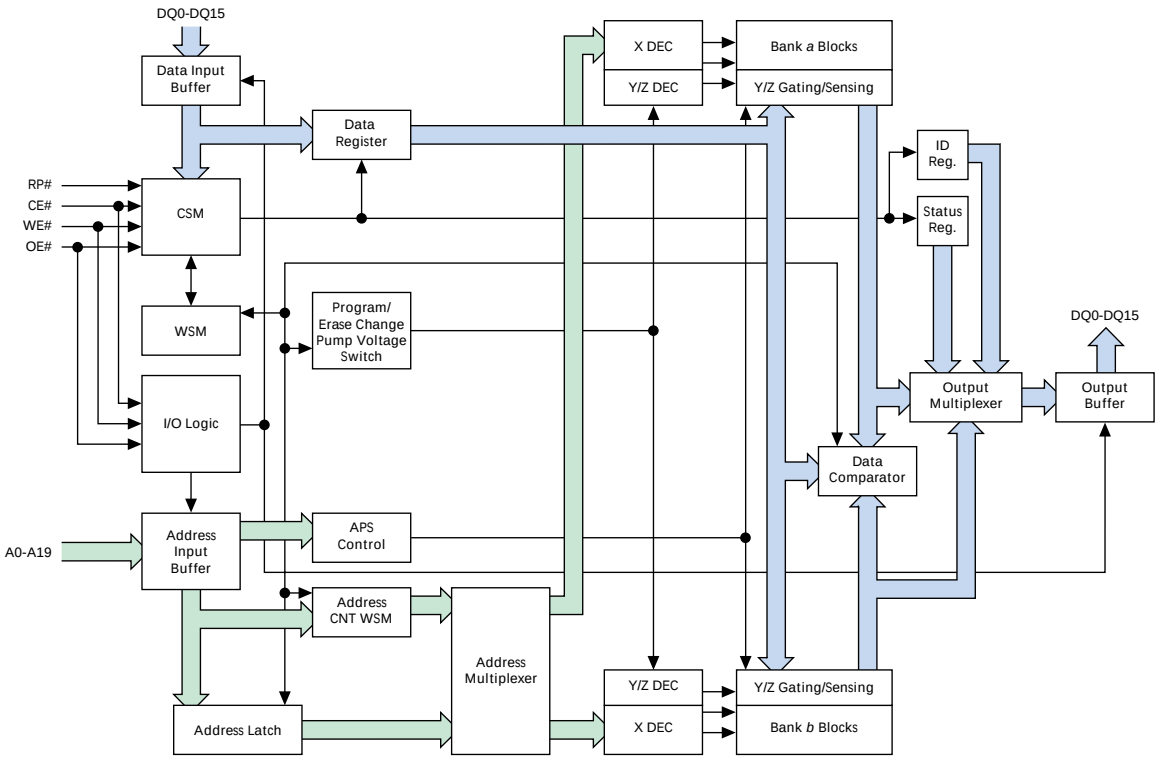
Table 1
Valid Part Number Combinations

PART NUMBER	ACCESS TIME (ns)	BOOT BLOCK	OPERATING TEMPERATURE RANGE
N02C1630E1AM-9BI	90	Bottom	-40°C to +85°C
N02C1630E1AM-9TI	90	Top	-40°C to +85°C

BLOCK DIAGRAM



FLASH FUNCTIONAL BLOCK DIAGRAM



BALL DESCRIPTIONS

66-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
A4, A5, A6, A7, A8, B3, B4, B5, B6, E5, G3, G4, G5, G6, G7, G8, G9, H4, H5, H6	A0–A19	Input	Address Inputs: Inputs for the addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. Flash: A0–A19; SRAM: A0–A16.
H7	F_CE#	Input	Flash Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
H9	F_OE#	Input	Flash Output Enable: Enables flash output buffers when LOW. When F_OE# is HIGH, the output buffers are disabled.
C3	F_WE#	Input	Flash Write Enable: Determines if a given cycle is a flash WRITE cycle. F_WE# is active LOW.
D4	F_RP#	Input	Reset. When F_RP# is a logic LOW, the device is in reset, which drives the outputs to High-Z and resets the WSM. When F_RP# is a logic HIGH, the device is in standard operation. When F_RP# transitions from logic LOW to logic HIGH, the device resets all blocks to locked and defaults to the read array mode.
E3	F_WP#	Input	Flash Write Protect. Controls the lock down function of the flexible locking feature.
G10	S_CE1#	Input	SRAM Chip Enable1: Activates the SRAM when it is LOW. HIGH level deselects the SRAM and reduces the power consumption to standby levels.
D8	S_CE2	Input	SRAM Chip Enable2: Activates the SRAM when it is HIGH. LOW level deselects the SRAM and reduces the power consumption to standby levels.
F5	S_OE#	Input	SRAM Output Enable: Enables SRAM output buffers when LOW. When S_OE# is HIGH, the output buffers are disabled.
B8	S_WE#	Input	SRAM Write Enable: Determines if a given cycle is an SRAM WRITE cycle. S_WE# is active LOW.
F3	S_LB#	Input	SRAM Lower Byte: When LOW, it selects the SRAM address lower byte (DQ0–DQ7).
F4	S_UB#	Input	SRAM Upper Byte: When LOW, it selects the SRAM address upper byte (DQ8–DQ15).
B7, B9, B10, C7, C8, C9, C10, D7, E6, E8, E9, E10, F7, F8, F9, F10	DQ0–DQ15	Input/ Output	Data Inputs/Outputs: Input array data on the second CE# and WE# cycle during PROGRAM command. Input commands to the command user interface when CE# and WE# are active. Output data when CE# and OE# are active.

(continued on next page)

BALL DESCRIPTIONS (continued)

66-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTION
E4	F_V_{PP}	Input/ Supply	Flash Program/Erase Power Supply: [1.65V–3.3V or 11.4V–12.6V]. Operates as input at logic levels to control complete device protection. Provides backward compatibility for factory programming when driven to 11.4V–12.6V. Lower F_V_{PP} voltages are available; consult factory for availability.
D10	F_V_{CC}	Supply	Flash Power Supply: [2.7V–3.3V]. Supplies power for device operation.
A9, H8	F_V_{SS}	Supply	Flash Specific Ground: Do not float any ground pin.
D9	S_V_{CC}	Supply	SRAM Power Supply: [2.7V–3.3V]. Supplies power for device operation.
D3	S_V_{SS}	Supply	SRAM Specific Ground: Do not float any ground pin.
A1, A2, A3, A10, A11, A12, C4, H1, H2, H3, H10, H11, H12	NC	–	No Connect: Lead is not internally connected; it may be driven or floated.

TRUTH TABLE – FLASH

MODES	FLASH SIGNALS				SRAM SIGNALS						MEMORY OUPUT		NOTES
	F_RP#	F_CE#	F_OE#	F_WE#	S_CE1#	S_CE2	S_OE#	S_WE#	S_UB#	S_LB#	MEMORY BUS CONTROL	DQ0–DQ15	
Read	H	L	L	H	SRAM must be High-Z						Flash	DOUT	1, 2, 3
Write	H	L	H	L							Flash	DIN	1
Standby	H	H	X	X	SRAM any mode allowable						Other	High-Z	4, 5
Output Disable	H	L	H	H							Other	High-Z	4, 6
Reset	L	X	X	X							Other	High-Z	4, 7

TRUTH TABLE – SRAM

MODES	FLASH SIGNALS				SRAM SIGNALS						MEMORY OUPUT		NOTES
	F_RP#	F_CE#	F_OE#	F_WE#	S_CE1#	S_CE2	S_OE#	S_WE#	S_UB#	S_LB#	MEMORY BUS CONTROL	DQ0–DQ15	
Read													
DQ0–DQ15	Flash must be High-Z				L	H	L	H	L	L	SRAM	DOUT	1, 3
DQ0–DQ7					L	H	L	H	H	L	SRAM	DOUT LB	8
DQ8–DQ15					L	H	L	H	L	H	SRAM	DOUT UB	9
Write													
DQ0–DQ15					L	H	H	L	L	L	SRAM	DIN	1, 3
DQ0–DQ7					L	H	H	L	H	L	SRAM	DIN LB	10
DQ8–DQ15					L	H	H	L	L	H	SRAM	DIN UB	11
Standby	Flash any mode allowable				H	X	X	X	X	X	Other	High-Z	4, 5
					X	L	X	X	X	X	Other	High-Z	4, 5
Output Disable					L	H	H	H	X	X	Other	High-Z	4, 5
Data Retention					Same as standby						Other	High-Z	4, 6

NOTES: 1. Two devices may not drive the memory bus at the same time.
2. Allowable flash read modes include read array, read configuration, and read status.
3. Outputs are dependent on a separate device controlling bus outputs.
4. Modes of the Flash and SRAM can be interleaved so that while one is disabled, the other controls outputs.
5. The SRAM may be placed into data retention mode by lowering S_VCC to the VDR range, as specified.
6. SRAM is enabled and/or disabled with the logical function: S_CE1# or S_CE2.
7. Simultaneous operations can exist, as long as the operations are interleaved such that only one device attempts to control the bus outputs at a time.
8. Data output on lower byte only; upper byte High-Z.
9. Data output on upper byte only; lower byte High-Z.
10. Data input on lower byte only.
11. Data input on upper byte only.

ARCHITECTURE AND MEMORY ORGANIZATION

The Flash memory array is segmented into 31 blocks of 32K words, along with eight 4K-word parameter blocks. The device is available with block architecture mapped in either of the two configurations: the parameter blocks located at the top or at the bottom of the memory array, as required by different microprocessors. The N02C1630E1AM top boot configuration with the blocks and address ranges is shown in Figure 1 and the bottom boot configuration in Figure 2.

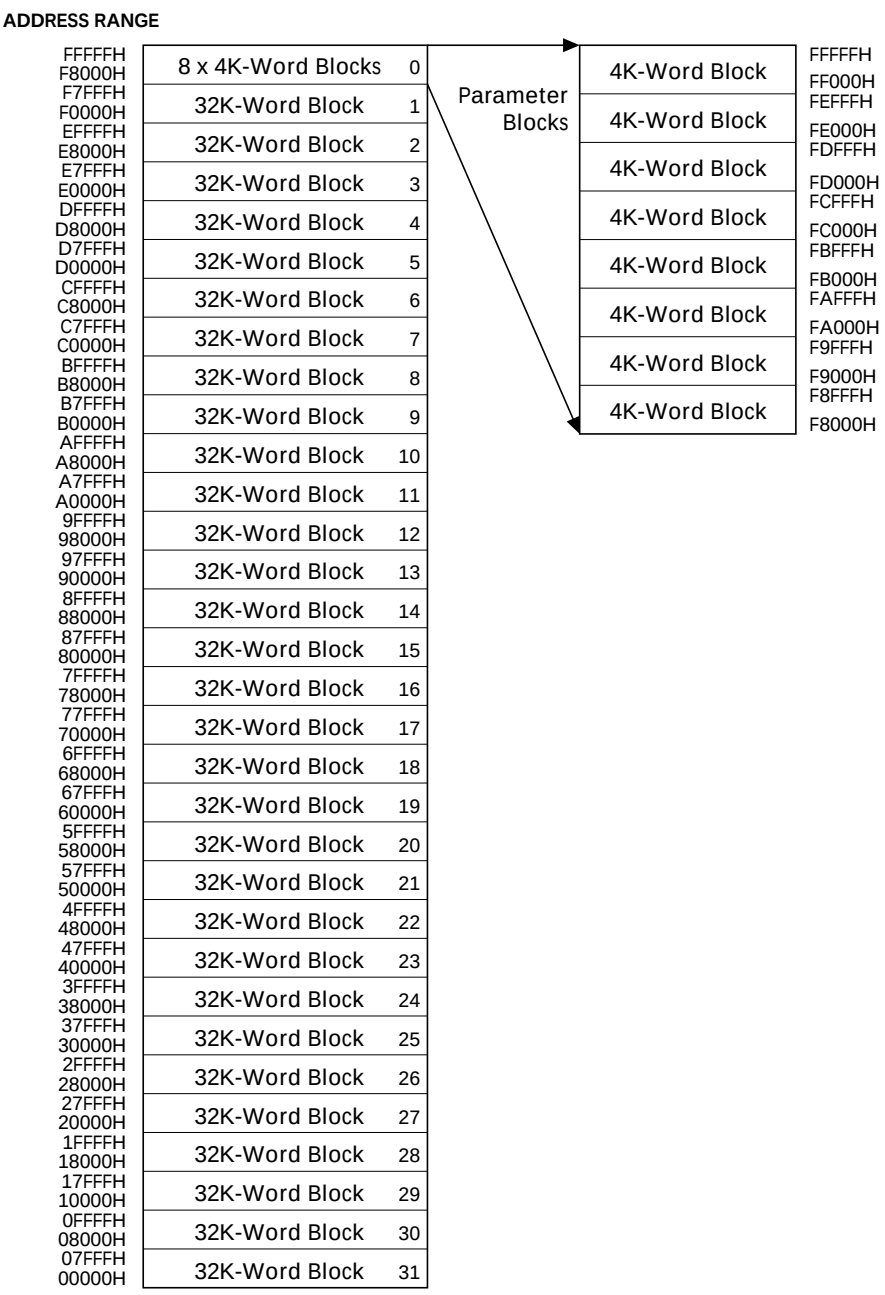


Figure 1
Top Boot Block Device

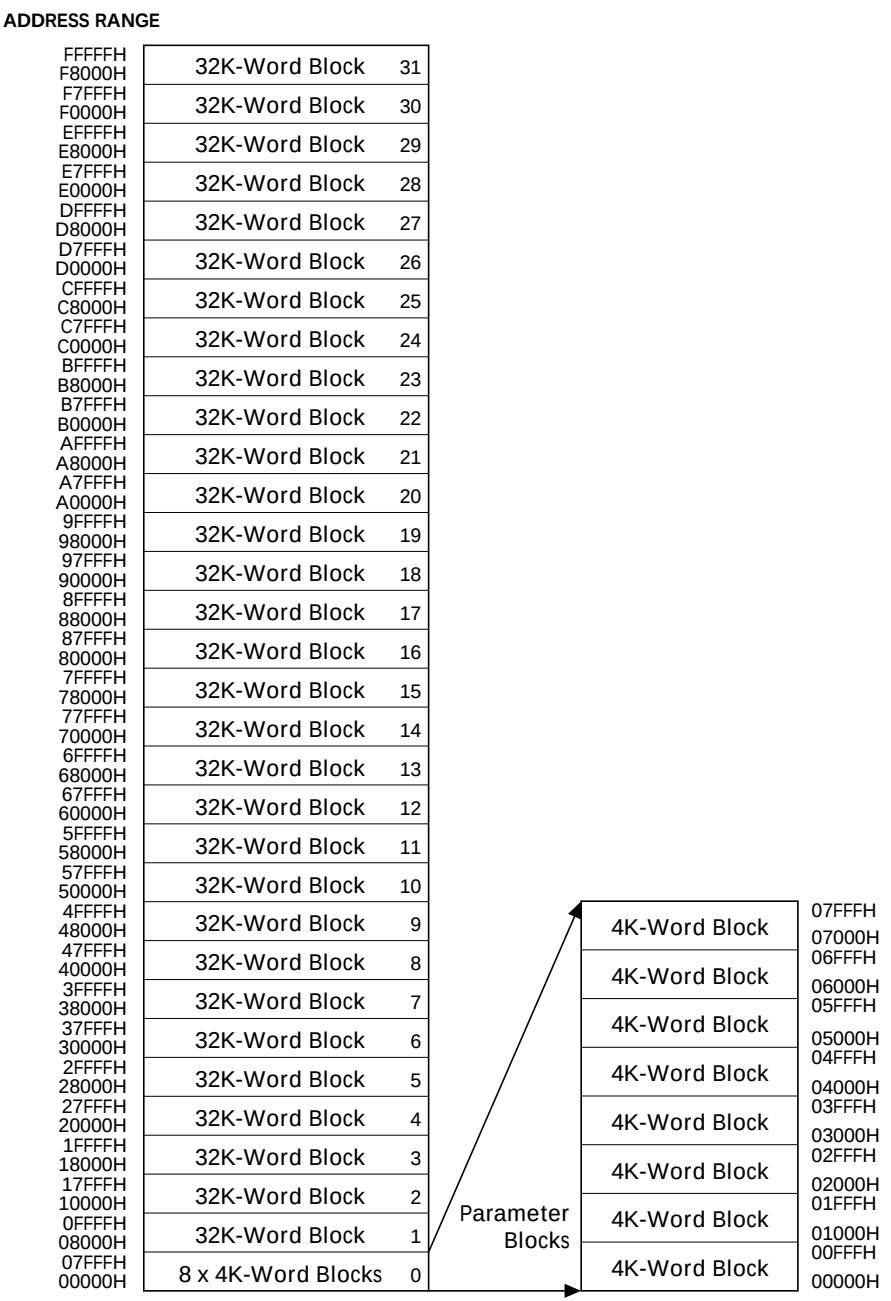


Figure 2
Bottom Boot Block Device

FLASH MEMORY OPERATING MODES

COMMAND STATE MACHINE

Commands are issued to the command state machine (CSM) using standard microprocessor write timings. The CSM acts as an interface between external microprocessors and the internal write state machine (WSM). The available commands are listed in Table 2, their definitions are given in Table 3 and their descriptions in Table 4. Program and erase algorithms are automated by the on-chip WSM. Table 5 shows the CSM transition states. Once a valid PROGRAM/ERASE command is entered, the WSM executes the appropriate algorithm, which generates the necessary timing signals to control the device internally. A command is valid only if the exact sequence of WRITEs is completed. After the WSM completes its task, the write state machine status (WSMS) bit (SR7) (see Table 7) is set to a logic HIGH level (V_{IH}), allowing the CSM to respond to the full command set again.

OPERATIONS

Device operations are selected by entering a standard JEDEC 8-bit command code with conventional microprocessor timings into an on-chip CSM through I/O pins DQ0–DQ7. The number of bus cycles required to activate a command is typically one or two. The first operation is always a WRITE. Control pins F_CE# and F_WE# must be at a logic LOW level (V_{IL}), and F_OE# and F_RP# must be at logic HIGH (V_{IH}). The second operation, when needed, can be a WRITE or a READ depending upon the command. During a READ operation, control pins F_CE# and F_OE# must be at a logic LOW level (V_{IL}), and F_WE# and F_RP# must be at logic HIGH (V_{IH}).

Table 6 illustrates the bus operations for all the modes: write, read, reset, standby, and output disable.

When the device is powered up, internal reset circuitry initializes the chip to a read array mode of operation. Changing the mode of operation requires that a command code be entered into the CSM. The on-chip status register allows the monitoring of the progress of various operations that can take place. The status register is interrogated by entering a READ STATUS REGISTER command onto the CSM (cycle 1) and reading the register data on I/O pins DQ0–DQ7 (cycle 2). Status register bits SR0-SR7 correspond to DQ0–DQ7 (see Table 7).

COMMAND DEFINITION

Once a specific command code has been entered, the WSM executes an internal algorithm, generating the necessary timing signals to program, erase, and verify data. See Table 3 for the CSM command definitions and data for each of the bus cycles.

STATUS REGISTER

The status register allows the user to determine whether the state of a PROGRAM/ERASE operation is pending or complete. The status register is monitored toggling F_OE#, F_CE#, and address lines by reading the resulting status code on I/O pins DQ0–DQ7. The high-order I/Os (DQ8–DQ15) are set to 00h internally, so only the low-order I/O pins (DQ0–DQ7) need to be interpreted. Address lines select the status register pertinent to the selected memory partition.

Register data is updated on the falling edge of F_OE# or F_CE#, whichever occurs first. The latest falling edge of either of these two signals updates the latch within a

Table 2
Command State Machine Codes For Device Mode Selection

COMMAND DQ0–DQ7	CODE ON DEVICE MODE
10h/40h	Program setup/alternate program setup
20h	Block erase setup
50h	Clear status register
60h	Reserved
70h	Read status register
90h	Read device identity
0Fh	Soft protection
B0h	Program/erase suspend
D0h	Program/erase resume - erase confirm
FFh	Read array/OTP exit
AFh	OTP entry

given READ cycle. Latching the data prevents errors from occurring if the register input changes during a status register read. To ensure that the status register output contains updated status data, CE# or OE# must be toggled for each subsequent STATUS READ.

The status register provides the internal state of the WSM to the external microprocessor. During periods when the WSM is active, the status register can be polled to determine the WSM status. Table 7 defines the status register bits.

After monitoring the status register during a PROGRAM/ERASE operation, the data appearing on DQ0–DQ7 remains as status register data until a new command is issued to the CSM. To return the device to other modes of operation, a new command must be issued to the CSM.

COMMAND STATE MACHINE OPERATIONS

The CSM decodes instructions for the commands listed in Table 2. The 8-bit command code is input to the device on DQ0–DQ7 (see Table 3 for command definitions). During a PROGRAM or ERASE cycle, the CSM informs the WSM that a PROGRAM or ERASE cycle has been requested.

During a PROGRAM cycle, the WSM controls the program sequences and the CSM responds to a PROGRAM SUSPEND command only.

During an ERASE cycle, the CSM responds to an ERASE SUSPEND command only. When the WSM has completed its task, the WSMS bit (SR7) is set to a logic HIGH level and the CSM responds to the full command set. The CSM stays in the current command state until the microprocessor issues another command.

The WSM successfully initiates an ERASE or PROGRAM operation only when V_{PP} is within its correct voltage range.

Table 3
Command Definitions

	FIRST CYCLE			SECOND CYCLE		
COMMAND	**OPERATION**	**ADDRESS**	**CSM/INPUT**	**OPERATION**	**ADDRESS**	**DATA**
READ ARRAY	WRITE	X	FFh	READ	WA	AD
IDENTIFY DEVICE	WRITE	X	90h	READ	IA	ID
READ STATUS REGISTER	WRITE	X	70h	READ	BA	SRD
WORD PROGRAM	WRITE	X	10h/40h	WRITE	WA	PD
BLOCK ERASE	WRITE	X	20h	WRITE	BA	D0h
PROGRAM/ERASE SUSPEND	WRITE	X	B0h			
PROGRAM/ERASE RESUME	WRITE	X	D0h			
CLEAR STATUS REGISTER	WRITE	X	50h			
SOFT PROTECTION	WRITE	X	0Fh	WRITE	BA	SPC
OTP ENTRY	WRITE	X	AFh	WRITE	X	AFh
OTP EXIT	WRITE	X	FFh	WRITE	X	FFh

NOTE: 1. The command data is written through DQ0-DQ7
2. ID = Manufacturer ID: 002Ch; Device ID (Top Boot): 4492h; Device ID (Bottom Boot): 4493h
3. IA = Identify address: 00000h for manufacturer code and 00001h for device code
4. BA = Any address within the block to be selected
5. WA = Word address
6. AD = Array data
7. SRD = Data read from status register
8. PD = Data to be written at location WA
9. SPC = Soft protect command:
   00h = Clear all soft protection
   FFh = Set all soft protection
   F0h = Clear addressed block soft protection
   0Fh = Set addressed block soft protection
10. X = Don't Care

Table 4
Command Descriptions

CODE	DEVICE MODE	BUS CYCLE	DESCRIPTION
10h	Alt. Program Setup	First	Operates the same as a PROGRAM SETUP command.
20h	Erase Setup	First	Prepares the CSM for an ERASE CONFIRM command. If the next command is not ERASE CONFIRM, the CSM will set both SR4 and SR5 of the status register to a “1,” place the device into read status register mode, and wait for another command.
40h	Program Setup	First	A two-cycle command: The first cycle prepares for a PROGRAM operation, the second cycle latches addresses and data and initiates the WSM to execute the program algorithm. The flash outputs status register data on the falling edge of F_OE# or F_CE#, whichever occurs first.
50h	Clear Status Register	First	The WSM can set the program status (SR4), and erase status (SR5) bits in the status register to “1,” but it cannot clear them to “0.” Issuing this command clears those bits to “0.”
70h	Read Status Register	First	Places the device into read status register mode. Reading the device will output the contents of the status register, regardless of the address presented to the device. The device will automatically enter this mode after a PROGRAM or ERASE operation has been initiated.
90h	Read Device Identity	First	Puts the device into the read configuration mode so that reading the device will output the manufacturer/device codes.
0Fh	Soft Protection	First	Puts the device into the soft protection mode so that the protection bit for each block can be set and cleared.
B0h	Program Suspend Erase Suspend	First First	Suspends the currently executing PROGRAM/ERASE operation. The status register will indicate when the operation has been successfully suspended by setting either the program suspend (SR2) or erase suspend (SR6) and the WSMS bit (SR7) to a “1” (ready). The WSM will continue to idle in the suspend state, regardless of the state of all input control pins except F_RP#, which will immediately shut down the WSM and the remainder of the chip if F_RP# is driven to V_{IL}.
D0h	Erase Confirm	First	If the previous command was an ERASE SETUP command, then the CSM will close the address and data latches, and it will begin erasing the block indicated on the address pins. During programming/erase, the device will respond only to the ERASE SUSPEND command and will output status register data on the falling edge of F_OE# or F_CE#, whichever occurs last.
	Program/Erase Resume	First	If a PROGRAM or ERASE operation was previously suspended, this command will resume the operation.
FFh	Read Array OTP Exit	First Second	During the array mode, array data will be output on the data bus. Exits the OTP area on second FFh command.
AFh	OTP Entry	Second	Allows programming or reading of the OTP area on second AFh command.

CLEAR STATUS REGISTER

The internal circuitry can set, but not clear, the block lock status bit (SR1), the V_{PP} status bit (SR3), the program status bit (SR4), and the erase status bit (SR5) of the status register. The CLEAR STATUS REGISTER command (50h) allows the external microprocessor to clear these status bits and synchronize to the internal operations. When the status bits are cleared, the device returns to the read array mode.

READ OPERATIONS

The following READ operations are available: READ ARRAY, READ DEVICE IDENTIFICATION and READ STATUS REGISTER.

READ ARRAY

The array is read by entering the command code FFh on DQ0–DQ7. Control pins F_CE# and F_OE# must be at a logic LOW level (V_{IL}), and F_WE# and F_RP# must be at a logic HIGH level (V_{IH}) to read data from the array. Data is available on DQ0–DQ15. Any valid address within any of the blocks selects that address and allows data to be read from that address. Upon initial power-up, the device defaults to the read array mode.

READ DEVICE IDENTIFICATION DATA

Device identification codes are read by entering command code 90h on DQ0-DQ7. Two bus cycles are required for this operation, the first to enter the command code and the second to read the selected code. Control pins CE# and OE# must be at a logic LOW level (V_{IL}) and WE# and RP# must be at a logic HIGH level (V_{IH}). The manufacturer code is obtained on DQ0-DQ15 in the second cycle, after the identify address 00000h is latched. The device code is obtained on DQ0-DQ15 in the second cycle, after the identify address 00001h is latched (see Table 3).

READ STATUS REGISTER

The status register is read by entering the command code 70h on DQ0-DQ7. Control pins F_CE# and F_OE# must be at a logic LOW level (V_{IL}), andF_ WE# and F_RP# must be at a logic HIGH level (V_{IH}). Two bus cycles are required for this operation: one to enter the command code, and one to read the status register. The status register contents are updated on the falling edge of F_CE# or F_OE#, whichever occurs last within the cycle.

PROGRAMMING OPERATIONS

There are two CSM commands for programming: PROGRAM SETUP and ALTERNATE PROGRAM SETUP (see Table 2).

After the desired command code is entered (10h or 40h command code on DQ0–DQ7), the WSM takes over and correctly sequences the device to complete the PROGRAM operation. The WRITE operation may be monitored through the status register (see the Status Register section). During this time, the CSM will only respond to a PROGRAM SUSPEND command until the PROGRAM operation has been completed, after which time all commands to the CSM become valid again. During programming, V_{PP} must remain in the appropriate V_{PP} voltage range as shown in the recommended operating conditions table. Different combinations of RP#, WP#, and V_{PP} pin voltage levels ensure that data in certain blocks are secure and therefore cannot be programmed (see Table 5 for a list of combinations). Only “0s” are written and compared during a PROGRAM operation. If “1s” are programmed, the memory cell contents do not change and no error occurs. The PROGRAM operation can be suspended by issuing a PROGRAM SUSPEND command (B0h). Once the WSM reaches the suspend state, it allows the CSM to respond only to READ ARRAY, READ STATUS REGISTER or PROGRAM RESUME commands. During the PROGRAM SUSPEND operation, array data should be read from an address other than the one being programmed. To resume the PROGRAM operation, a PROGRAM RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 3 for programming operation and Figure 4 for program suspend and program resume).

ERASE OPERATIONS

An ERASE operation must be used to initialize all bits in an array block to “1s.” After BLOCK ERASE confirm is issued, the CSM responds only to an ERASE SUSPEND command until the WSM completes its task.

Block erasure inside the memory array sets all bits within the address block to logic 1s. Erase is accomplished only by blocks; data at single address locations within the array cannot be erased individually. The block to be erased is selected by using any valid address within that block. Block erasure is initiated by a command sequence to the CSM: BLOCK ERASE setup (20h) followed by BLOCK ERASE CONFIRM (D0h) (see Table 3). A two-command erase sequence protects against accidental erasure of memory contents.

When the BLOCK ERASE CONFIRM command is complete, the WSM automatically executes a sequence of events to complete the block erasure. During this sequence, the block is programmed with logic 0s, data is verified, all bits in the block are erased, and finally verification is performed to ensure that all bits are correctly erased. Monitoring of the ERASE operation is possible through the status register (see the Status

Table 5
Command State Machine Transition Table

	COMMAND INPUTS (and next state)													
Current State	SR7	Data when Read	Read Array (FFh)	Write setup (10h/ 40h)	Block erase setup (20h)	Erase confirm (D0h)	Prog./ erase susp. (B0h)	Prog./ erase resume (D0h)	Read SR (70h)	Clear SR (50h)	Identify device (90h)	Soft prot. setup (0Fh)	Soft prot. (SPC)	Otp entry (AFh)
Read Array	1	Array	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Read Status	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Identify Device	1	ID	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Soft Prot. Setup	1	Status	Soft prot. all	Read array								Soft prot. block	Soft prot.	Read array
Soft Protection Complete	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Write Setup	1	Status	Program											
Program Not Complete	0	Status	Program (not complete)				Prog. susp. status		Program (not complete)					
Program Suspend Status	1	Status	Program susp. read array	Program suspend read array		Program	Program susp. read array	Program	Program susp. status	Program suspend read array				
Program Suspend Read Array	1	Array	Program susp. read array	Program suspend read array		Program	Program susp. read array	Program	Program susp. status	Program suspend read array				
Program Complete	1	Status	Read Array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry
Erase Setup	1	Status	Erase command error			Erase	Erase	Erase	Erase command error					
Erase Comd. Error	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ Read array	Otp entry
Erase Not Complete	0	Status	Erase (not complete)				Erase susp. to status		Erase (not complete)					
Erase Suspend Status	1	Status	Erase susp. read array	Write setup	Erase susp. read array	Erase	Erase susp. read array	Erase	Erase susp. status	Erase suspend read array				
Erase Suspend Array	1	Array	Erase susp. read array	Write setup	Erase susp. read array	Erase	Erase susp. read array	Erase	Erase susp. status	Erase suspend read array				
Erase Complete	1	Status	Read array	Write setup	Erase setup	Read array			Read status	Read array	Identify device	Soft prot. setup	Soft prot. setup/ read array	Otp entry

Register section).

During the execution of an ERASE operation, the ERASE SUSPEND command (B0h) can be entered to direct the WSM to suspend the ERASE operation. Once the WSM has reached the suspend state, it allows the CSM to respond only to the READ ARRAY, READ STATUS REGISTER, PROGRAM SETUP, PROGRAM RESUME and ERASE RESUME. During the ERASE SUSPEND operation, array data must be read from a block other than the one being erased. To resume the ERASE operation, an ERASE RESUME command (D0h) must be issued to cause the CSM to clear the suspend state previously set (see Figure 6). It is also possible that an ERASE in any block can be suspended and a WRITE to another block can be initiated. After the completion of a WRITE, the ERASE can be resumed by writing an ERASE RESUME command.

Table 6
Bus Operations

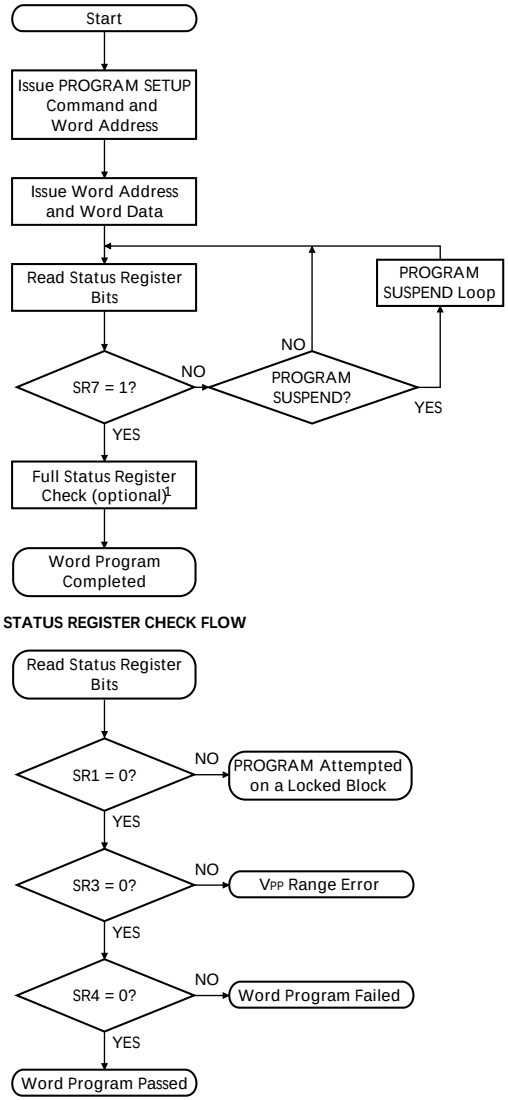
MODE	F_RP#	F_CE#	F_OE#	F_WE#	ADDRESS	DQ0–DQ15
Read (array, status register, device identification register)	V_{IH}	V_{IL}	V_{IL}	V_{IH}	X	D_{OUT}
Standby	V_{IH}	V_{IH}	X	X	X	High-Z
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	High-Z
Reset	V_{IL}	X	X	X	X	High-Z
Write	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	D_{IN}

Table 7
Status Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy	Check write state machine bit first to determine word program or block erase completion, before checking program or erase status bits.
SR6	ERASE SUSPEND STATUS (ESS) 1 = BLOCK ERASE Suspended 0 = BLOCK ERASE in Progress/Completed	When ERASE SUSPEND is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an ERASE RESUME command is issued.
SR5	ERASE STATUS (ES) 1 = Error in Block Erasure 0 = Successful BLOCK ERASE	When this bit is set to "1," WSM has applied the maximum number of erase pulses to the block and is still unable to verify successful block erasure.
SR4	PROGRAM STATUS (PS) 1 = Error in PROGRAM 0 = Successful PROGRAM	When this bit is set to "1," WSM has attempted but failed to program a word.
SR3	VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP = OK	The VPP status bit does not provide continuous indication of the VPP level. The WSM interrogates the VPP level only after the program or erase command sequences have been entered and informs the system if VPP has not been switched on. The VPP level is also checked before the PROGRAM/ERASE operation is verified by the WSM.
SR2	PROGRAM SUSPEND STATUS (PSS) 1 = PROGRAM Suspended 0 = PROGRAM in Progress/Completed	When PROGRAM SUSPEND is issued, WSM halts execution and sets both WSM and PSS bits to "1." PSS bit remains set to "1" until a PROGRAM RESUME command is issued.
SR1	BLOCK LOCK STATUS (BLS) 1 = PROGRAM/ERASE Attempted on a Locked Block; Operation Aborted 0 = No Operation to Locked Blocks	If a PROGRAM or ERASE operation is attempted to one of the locked blocks, this is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR0	RESERVED FOR FUTURE ENHANCEMENT	This bit is reserved for future.

Figure 3
Automated Word Programming Flowchart



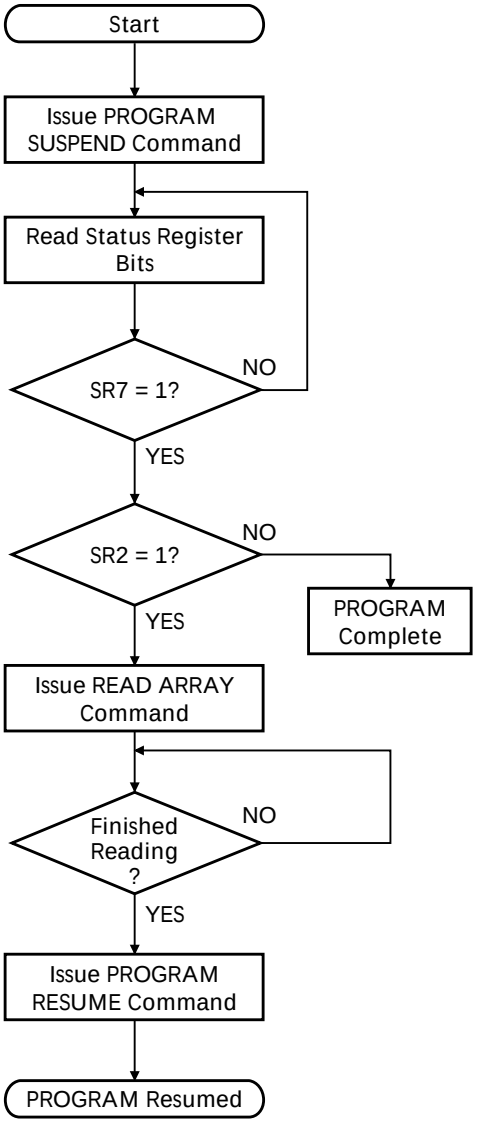
BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE PROGRAM SETUP	Data = 40h or 10h Addr = Don't care
WRITE	WRITE DATA	Data = Word to be programmed Addr = Address of word to be programmed
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent words. Write FFh after the last word programming operation to reset the device to read array mode.		

FULL STATUS REGISTER CHECK FLOW

BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect VPP low
Standby		Check SR4[3] 1 = Word program error

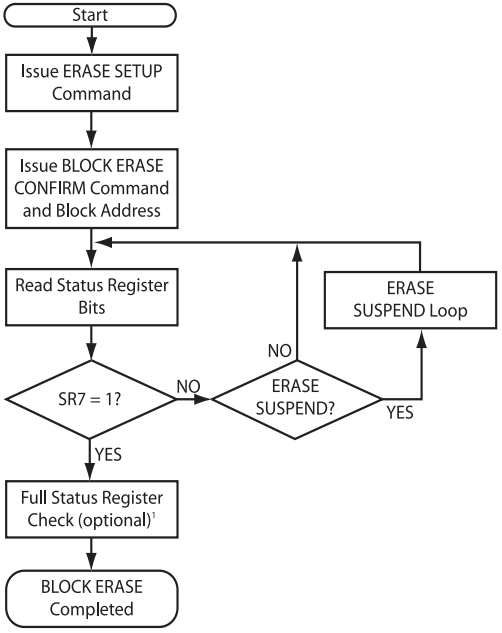
NOTE: 1. Full status register check can be done after each word or after a sequence of words.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR4 is cleared only by the CLEAR STATUS REGISTER command, but it does not prevent additional program operation attempts.

Figure 4
PROGRAM SUSPEND/
PROGRAM RESUME Flowchart



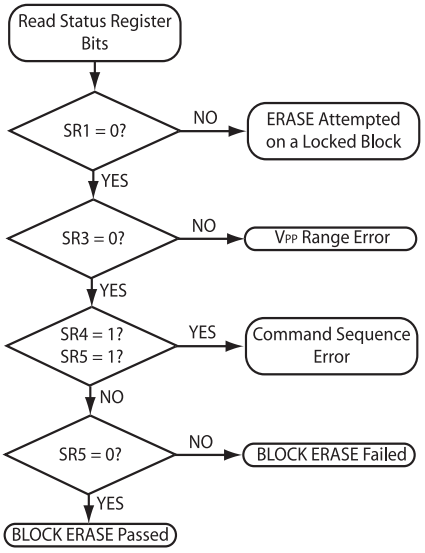
BUS OPERATION	COMMAND	COMMENTS
WRITE	PROGRAM SUSPEND	Data = B0h
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready
Standby		Check SR2 1 = Suspended
WRITE	READ MEMORY	Data = FFh
READ		Read data from block other than that being programmed.
WRITE	PROGRAM RESUME	Data = D0h Addr = Don't care

Figure 5
BLOCK ERASE Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	WRITE ERASE SETUP	Data = 20h Addr = Don't care
WRITE	ERASE	Data = D0h Block Addr = Address within block to be erased
READ		Status register data; toggle OE# or CE# to update status register.
Standby		Check SR7 1 = Ready, 0 = Busy
Repeat for subsequent blocks. Write FFh after the last BLOCK ERASE operation to reset the device to read array mode.		

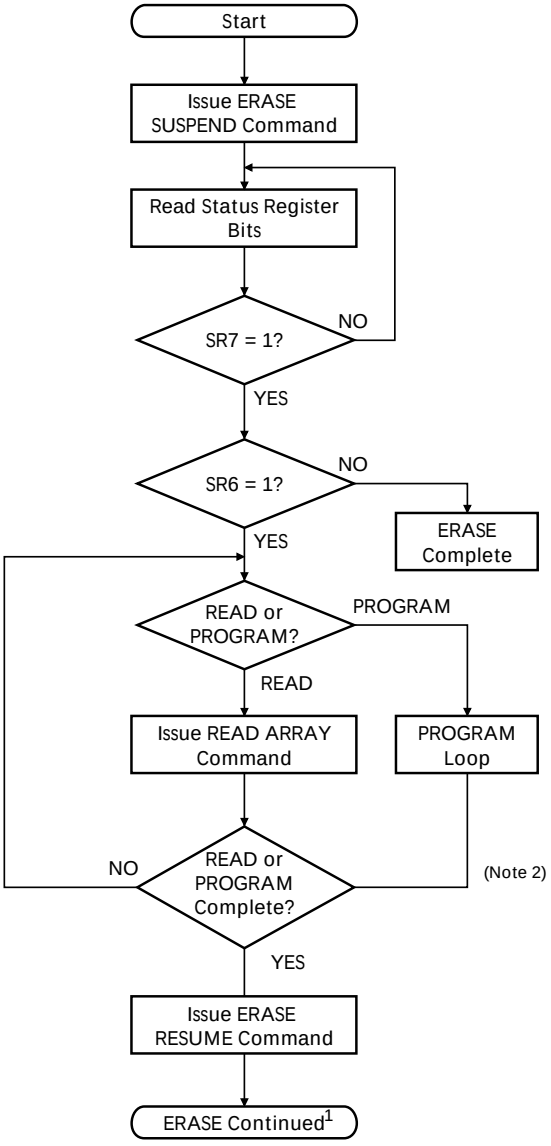
FULL STATUS REGISTER CHECK FLOW



BUS OPERATION	COMMAND	COMMENTS
Standby		Check SR1 1 = Detect locked block
Standby		Check SR3[2] 1 = Detect V_{PP} block
Standby		Check SR4 and SR5 1 = BLOCK ERASE command error
Standby		Check SR5[3] 1 = BLOCK ERASE error

NOTE: 1. Full status register check can be done after each block or after a sequence of blocks.
2. SR3 must be cleared before attempting additional PROGRAM/ERASE operations.
3. SR5 is cleared only by the CLEAR STATUS REGISTER command in cases where multiple blocks are erased before full status is checked.

Figure 6
ERASE SUSPEND/ERASE RESUME Flowchart



BUS OPERATION	COMMAND	COMMENTS
WRITE	ERASE SUSPEND	Data = B0h
READ		Status register data Toggle OE# or CE# to update status register
Standby		Check SR7 1 = Ready
Standby		Check SR6 1 = Suspended
WRITE or WRITE	READ MEMORY WRITE SETUP	Data = FFh Data = 40h or 10h Addr = Don't Care
READ or WRITE	 WRITE DATA	Read data from block other than that being erased Data = Word to be programmed Addr = Address of word to be programmed
WRITE	ERASE RESUME	Data = D0h Addr = Don't Care

NOTE: 1. See BLOCK ERASE Flowchart for complete erasure procedure.
2. See Word Programming Flowchart for complete programming procedure.

OTP MODE

The device has 128 bits of OTP (one time programmable) area. There are 64 bits that are programmed at the factory with a unique 64-bit code that is not modifiable. The other 64-bit OTP area is left blank to program for customer design requirements if needed. Protection of the user-programmable, 64-bit contents is provided, after the area is programmed, by programming the lock-bit.

To program the OTP area, two "AFh" commands must be written, followed by two WRITE cycles of the normal program sequences. When in the OTP mode, the WSM programs the OTP area and not the array. During programming, a read can acquire only the WSM status (status register output). When the programming is complete, the device remains in the OTP mode and only the status can be read in the OTP area. Writing two "FFh" commands exits the OTP mode and causes the device to go into the read array mode. To read the OTP area after programming, the OTP mode must be re-entered.

To read the OTP area contents, two "AFh" commands must be written, followed by a READ. Writing two "FFh" commands exits the OTP mode and causes the device to go into the read array mode.

After programming the 64-bit OTP area, the lock-bit can be programmed. The lock-bit is at address 00040H and is on DQ15. Once the lock-bit is programmed to a "0," the 64-bit, user-programmable area is permanently protected (see Figure 7). The lock- bit can be read in OTP mode, as described above.

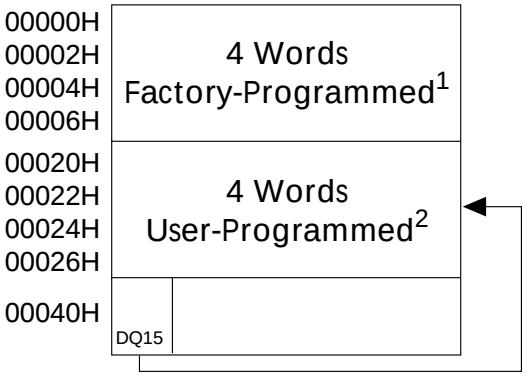


Figure 7
OTP Area Map

NOTE: 1. Always locked.
2. Locked by programming DQ15 at address 00040H.

STANDBY MODE

Icc supply current is reduced by applying a logic HIGH level on F_CE# and F_RP# to enter the standby mode. In the standby mode, the outputs are placed in High-Z. Applying a CMOS logic HIGH level on F_CE# and F_RP# reduces the current to I_{CC2} (MAX). If the device is deselected during an ERASE operation or during programming, the device continues to draw current until the operation is complete.

SOFT BLOCK DATA PROTECTION

Soft protection is available with CSM command 0Fh (see Table 3). The protection bit for each block can be set and cleared individually, or all at once. After the soft protection bit of a block is set, the block is protected when $V_{PP} > V_{PPLK}$, RP# is HIGH, and WP# is LOW. When $V_{PP} \leq V_{PPLK}$ the block is protected (locked) as well. A block is unlocked when WP# is HIGH, even if its soft protection bit is set (see Table 8)..

When the device is powered down or RP# reset, the soft protection blocks will be set to the protected state. So, if WP# goes LOW after first power-up, RP# reset, or power-down, all blocks will be protected. The CSM command 0Fh is needed to clear the soft protected blocks. When WP# goes LOW the cleared blocks will be unprotected.

The block lock status bit SR1 is used to monitor the individual block lock status after the second WRITE cycle of the soft protection CSM command. Additionally, to monitor the block lock status of any block, the read status register command 70h can be used. On the command's second cycle, any address within a block is issued and SR1 will indicate the block lock status for that block. When monitoring the block lock status bit SR1, the correct status can only be obtained with WP# LOW.

AUTOMATIC POWER SAVE MODE (APS)

Substantial power savings are realized during periods when the Flash array is not being read and the device is in the active mode. During this time the device switches to the automatic power save (APS) mode. When the device switches to this mode, I_{CC} is reduced to I_{CC2}. The low level of power is maintained until another operation is initiated. In this mode, the I/O pins retain the data from the last memory address read until a new address is read. This mode is entered automatically if no address or control pins toggle. At least one transition of F_CE# must occur after power-up to activate this mode's availability.

Table 8
Data Protection Combinations

DATA PROTECTION PROVIDED	V_{PP}	RP#	WP#
All blocks locked	≤ V_{PPLK}	X	X
All blocks locked	X	V_{IL}	X
All blocks unlocked	≥V_{PPLK}	V_{IH}	V_{IH}
Soft-protected blocks unlocked	≥V_{PPLK}	V_{IH}	V_{IL}

V_{PP} / V_{CC} PROGRAM AND ERASE VOLTAGES

The flash memory of the N02C1630E1AM provides in-system programming and erase with V_{PP} in the 1.65V–3.3V range. V_{PP} at 12V ±5% is supported for a maximum of 100 cycles and 10 cumulative hours. The device can withstand 100,000 WRITE/ERASE operations with V_{PP} = V_{CC}. During WRITE and ERASE operations, the WSM monitors the V_{PP} voltage level. WRITE/ERASE operations areallowed only when V_{PP} is within the ranges specified in Table 9.

Table 9
V_{PP} RANGE (V)

	MIN	MAX
In-System	1.65	2.2
In-Factory	11.4	12.6

POWER-UP

During a power-up, it is not necessary to sequence V_{CC} Q, V_{CC} and V_{PP}. However, it is recommended that RP# be held LOW during power-up for additional protection while V_{CC} is ramping above V_{LKO} to a stable operative level. After a power-up or RESET, the status register is reset, and the device will enter the array read mode.

POWER-UP PROTECTION

The likelihood of unwanted WRITE or ERASE operations is minimized since two consecutive cycles are required to execute either operation. When V_{CC} < V_{LKO}, the device does not accept any WRITE cycles, and noise pulses < 5ns on CE# or WE# do not initiate a WRITE cycle.

FLASH ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Voltage to Any Pin Except V_{CC} and V_{PP}
with Respect to V_{SS} ..... -0.5V to +4.0V
V_{PP} Voltage (for BLOCK ERASE and PROGRAM)
with Respect to V_{SS} ..... -0.5V to +13.0V**
V_{CC} Supply Voltage
with Respect to V_{SS} ..... -0.3V to +4.0V
Output Short Circuit Current 100mA
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Cycle ..... 260°C for 10s

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum DC voltage on Vpp may overshoot to +13.5V for periods less than 20ns.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Operating temperature	^{t}A	-40	+85	°C	
V_{CC} supply voltage	F_V_{CC}, S_V_{CC}	2.7	3.3	V	
Supply voltage, when used as logic control	V_{PP1}	1.65	3.3	V	
V_{PP} in-factory programming voltage	V_{PP2}	11.4	12.6	V	1
Data retention supply voltage	S_V_{DR}	1.0	–	V	
Block erase cycling		100,000	–	Cycles	

NOTE: 1. 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.

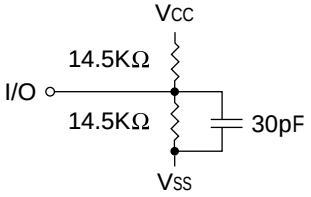


Figure 8
Output Load Circuit

COMBINED DC CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	Vcc = 2.7V–3.3V			UNITS	NOTES
			MIN	TYP	MAX		
Input Low Voltage		V_{IL}	-0.2	–	0.2	V	
Input High Voltage		V_{IH}	V_{CC} - 0.2V	–	V_{CC} + 0.2V	V	
Output Low Voltage I_{OL} = 100□A	Vcc = Vcc (MIN),	V_{OL}	–	–	0.10	V	
Output High Voltage I_{OH} = 100□A	Vcc=Vcc(MIN),	V_{OH} 0.1V	V_{CC} -	–	–	V	
V_{PP} Lock Out Voltage		V_{PPLK}	–	–	1.0	V	
V_{PP} During Program/Erase		V_{PP1}	1.65	–	3.3	V	
Operations		V_{PP2}	11.4	–	12.6	V	2
V_{CC} Program/Erase Lock Voltage		V_{LKO}	1.5	–	–	V	
Input Leakage Current	Vcc=Vcc(MAX)	I_L	–	–	1	µA	
Output Leakage Current	Vcc=Vcc(MAX)	I_{OZ}	–	–	10	µA	
F_V_{CC} Read Current at 5MHz	Vcc=Vcc(MAX) CE#=Vil,OE#=VihRP#=Vih	I_{CC1}	–	–	30	mA	3
F_V_{CC} plus S_V_{CC} Standby Current	Vcc=Vcc(MAX)	I_{CC3}	–	25	70	µA	
F_V_{CC} Program Current		I_{CC4}+I_{PP3}	–	–	55	m A	
F_V_{CC} Erase Current		I_{CC5}+I_{PP4}	–	–	45	mA	
F_V_{CC}/S_V_{CC} Erase Suspend Current		I_{CC6}	–	–	25	µA	
F_V_{CC}/S_V_{CC} Program Suspend Current		I_{CC7}	–	–	25	µA	
Read-While-Write Current		I_{CC8}	–	–	95	mA	
S_V_{CC} Read/Write Operating Supply Current – Word Access Mode	V_{IN} = V_{IH} or V_{IL} Chip Enabled, I_{OL} = 0	I_{CC10}	–	3	8	mA	4

NOTE: 1. All currents are in RMS unless otherwise noted.
2. 12V V_{PP} is supported for a maximum of 100 cycles and may be connected for up to 10 cumulative hours.
3. Icc is dependent on cycle rates.
4. Operating current is a linear function of operating frequency and voltage. Operating current can be calculated using the formula shown with operating frequency (f) expressed in MHz and operating voltage (V) in volts.
Example: When operating at 2 MHz at 2V, the device will draw a typical active current of 0.8*2* = 3.2mA in the page access mode. This parameter is specified with the outputs disabled to avoid external loading effects. The user must add current required to drive output capacitance expected in the actual system.

(continued on the next page)

COMBINED DC CHARACTERISTICS (continued)

DESCRIPTION	CONDITIONS	SYMBOL	V_{CC} = 2.7V–3.3V			UNITS	NOTES
			MIN	TYP	MAX		
V_{PP} Read Current	$V_{PP} \leq V_{CC}$	I_{PP1}	–	–	15	µA	
	$V_{PP} \geq V_{CC}$		–	–	200	µA	
V_{PP} Standby Current	$V_{PP} \leq V_{CC}$	I_{PP2}	–	–	10	µA	
	$V_{PP} \geq V_{CC}$		–	–	200	µA	
V_{PP} Erase Suspend Current	$V_{PP} = V_{PP1}$	I_{PP5}	–	–	10	µA	
	$V_{PP} = V_{PP2}$		–	–	200	µA	
V_{PP} Program Suspend Current	$V_{PP} = V_{PP1}$	I_{PP6}	–	–	10	µA	
	$V_{PP} = V_{PP2}$		–	–	200	µA	

NOTE: 1. All currents are in RMS unless otherwise noted.

FLASH READ CYCLE TIMING REQUIREMENTS

PARAMETER	SYMBOL	-90 Vcc = 2.7V–3.3V MIN	-90 Vcc = 2.7V–3.3V MAX			UNITS
Address to output delay	tAA		90			ns
CE# LOW to output delay	tACE		90			ns
OE# LOW to output delay	tAOE		30			ns
F_RP# HIGH to output delay	tRWH		600			ns
CE# or OE# HIGH to output High-Z	tOD		25			ns
Output hold from address, CE# or OE# change	tOH	0				ns
CE# HIGH between subsequent synchronous READs	tCBPH	20				ns
READ Cycle Time	tRC	90				ns

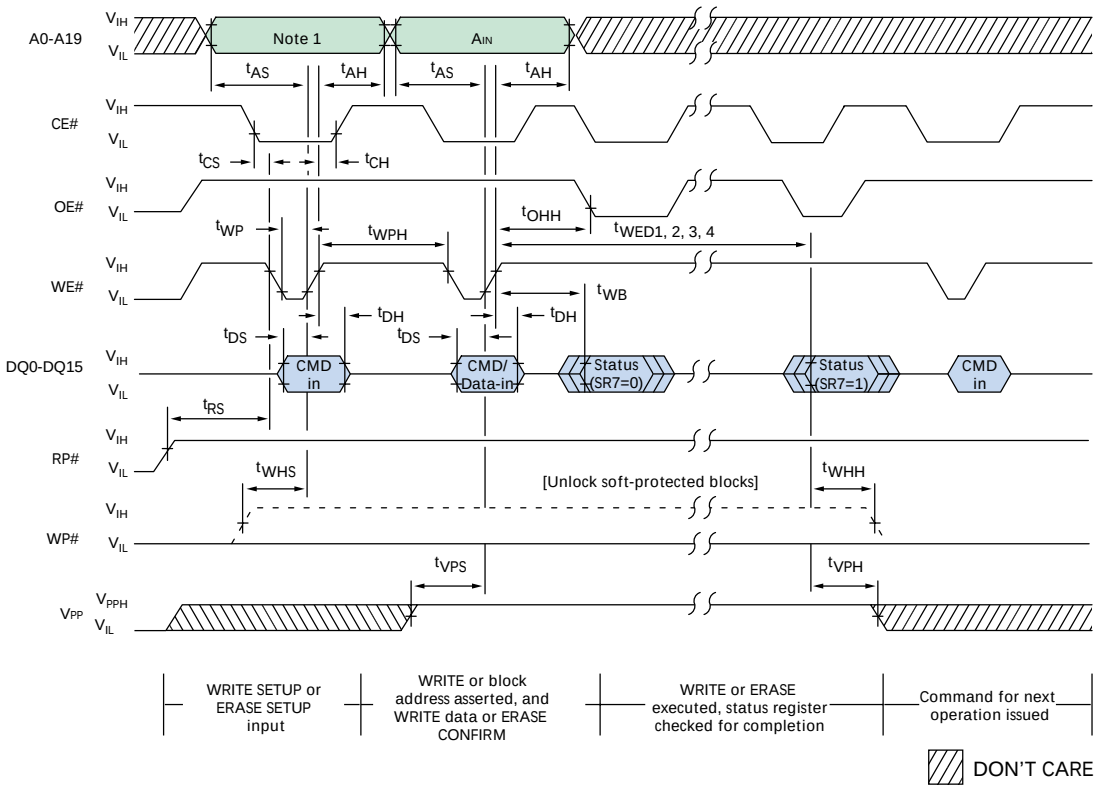
FLASH WRITE CYCLE TIMING REQUIREMENTS

PARAMETER	SYMBOL	-90 Vcc = 2.7V–3.3V MIN	-90 Vcc = 2.7V–3.3V MAX	UNITS
Reset HIGH recovery to WE# going LOW	tRS	150		ns
CE# setup to WE# going LOW	tCS	0		ns
Write pulse width	tWP	70		ns
Data setup to WE# going HIGH	tDS	50		ns
Address setup to WE# going HIGH	tAS	70		ns
CE# hold from WE# HIGH	tCH	0		ns
Data hold from WE# HIGH	tDH	0		ns
Address hold from WE# HIGH	tAH	0		ns
Write pulse width HIGH	tWPH	30		ns
WP# setup to WE# going HIGH	tWHS	0		ns
VPP setup to WE# going HIGH	tVPS	200		ns
OE# hold from WE# going HIGH	tOHH	30		ns
WP# hold from valid SRD	tWHH	0		ns
VPP hold from valid SRD	tVPH	0		ns
WE# HIGH to busy status	tWB	200		ns
WRITE duration	tWED1	6		us
Boot BLOCK ERASE duration	tWED2	0.5		s
Parameter BLOCK ERASE duration	tWED3	0.5		s
Main BLOCK ERASE duration	tWED4	1		s

FLASH ERASE AND PROGRAM CYCLE TIMING REQUIREMENTS

PARAMETER	2.7V–3.3V Vcc 1.65V–3.3V VPP TYP	2.7V–3.3V Vcc 1.65V–3.3V VPP MAX	12V VPP TYP	12V VPP MAX	UNITS	NOTES
Boot/parameter BLOCK ERASE time	0.5	4	0.5	4	s	
Main BLOCK ERASE time	1	5	1	5	s	
Boot/parameter BLOCK WRITE time	0.1	–	0.1	–	s	
Main BLOCK WRITE time	0.3	–	0.3	–	s	
Program/erase suspend latency	1	3	1	3	□s	

WRITE/ERASE OPERATION

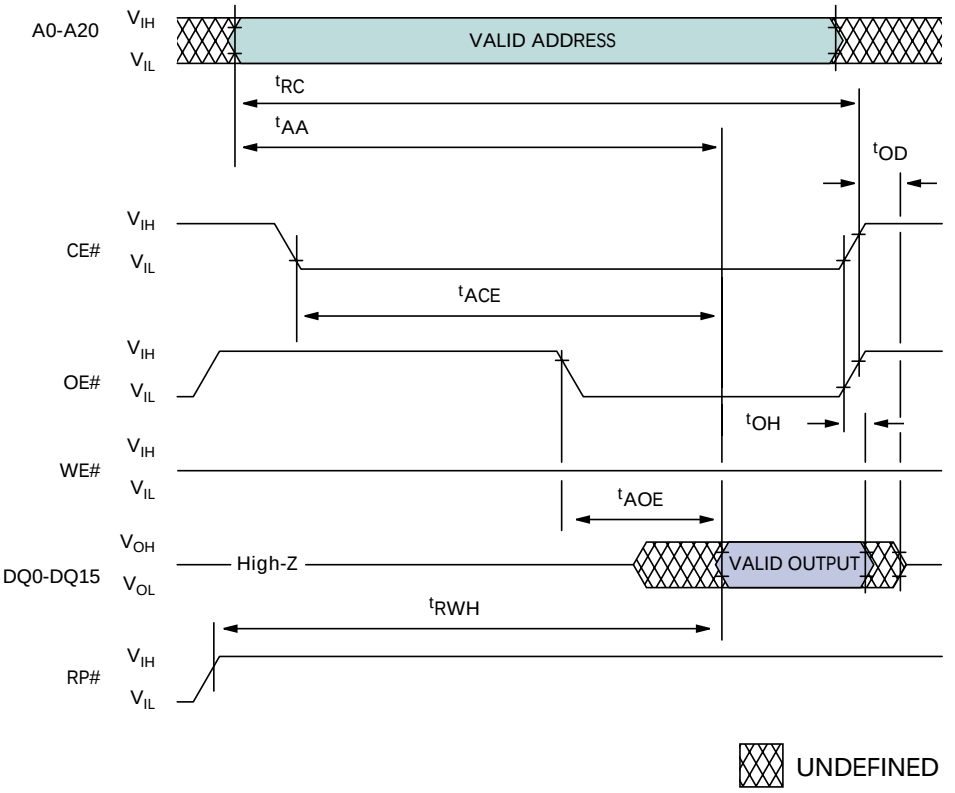


TIMING PARAMETERS

SYMBOL	-90 MIN		UNITS
tWPH	30		ns
tWP	70		ns
tAS	70		ns
tAH	0		ns
tDS	50		ns
tDH	0		ns
tCS	0		ns
tCH	0		ns
tVPS	200		ns
tRS	150		ns

SYMBOL	-90 MIN		UNITS
tWED1	6		□s
tWED2	0.5		s
tWED3	0.5		s
tWED4	1		s
tVPH	0		ns
tWB	200		ns
tWHS	0		ns
tWHH	0		ns
tOHH	30		ns

READ OPERATION



READ TIMING PARAMETERS

SYMBOL	-90 Vcc=2.7V–3.3V MIN	MAX			UNITS
tAA		90			ns
tACE		90			ns
tAOE		30			ns
tRWH		600			ns

SYMBOL	-90 Vcc=2.7V–3.3V MIN	MAX			UNITS
tOD		25			ns
tOH	0				ns
tRC	90				ns

SRAM OPERATING MODES

SRAM READ ARRAY

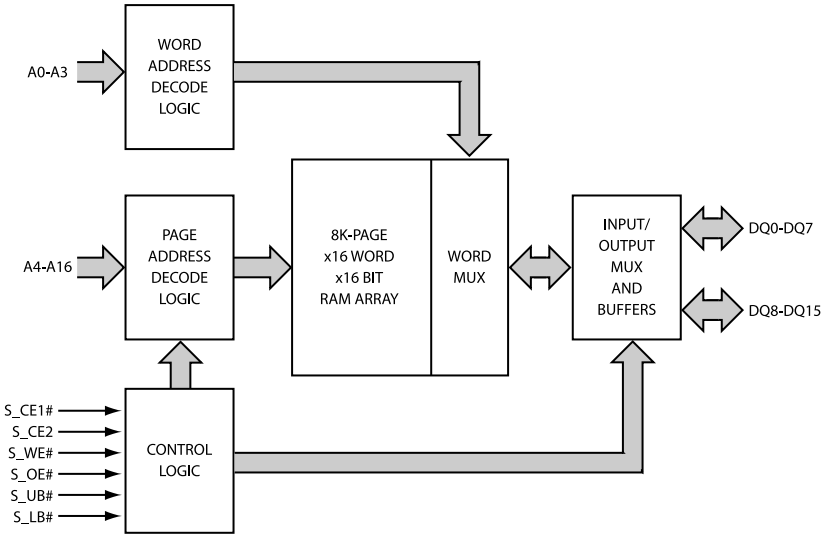
The operational state of the SRAM is determined by S_CE1#, S_CE2, S_WE#, S_OE#, S_UB#, and S_LB#, as indicated in the Truth Table. In order to perform an SRAM READ operation, S_CE1#, and S_OE#, must be at V_{IL}, and S_CE2 and S_WE# must be at V_{IH}. When in this state, S_UB# and S_LB# control whether the lower byte is read (S_UB# V_{IH}, S_LB# V_{IL}), the upper byte is read (S_UB# V_{IL}, S_LB# V_{IH}), both upper and lower bytes are read (S_UB# V_{IL}, S_LB# V_{IL}), or neither are read (S_UB# V_{IH}, S_LB# V_{IH}) and the device is in a standby state.

While performing an SRAM READ operation, current consumption may be reduced by reading within a 16-word page. This is done by holding S_CE1# and S_OE# at V_{IL}, S_WE# and S_CE2 at V_{IH}, and toggling addresses A0-A3. S_UB# and S_LB# control the data width as described above.

SRAM WRITE ARRAY

In order to perform an SRAM WRITE operation, S_CE1# and S_WE# must be at V_{IL}, and S_CE2 and S_OE# must be at V_{IH}. When in this state, S_UB# and S_LB# control whether the lower byte is written (S_UB# V_{IH}, S_LB# V_{IL}), the upper byte is written (S_UB# V_{IL}, S_LB# V_{IH}), both upper and lower bytes are written (S_UB# V_{IL}, S_LB# V_{IL}), or neither are written (S_UB# V_{IH}, S_LB# V_{IH}) and the device is in a standby state.

SRAM FUNCTIONAL BLOCK DIAGRAM



TIMING TEST CONDITIONS

Input pulse levels	0.1V V_{CC} to 0.9V V_{CC}
Input rise and fall times	5ns
Input timing reference levels	0.5V
Output timing reference levels	0.5V
Operating Temperature	-40°C to +85°C

SRAM READ CYCLE TIMING

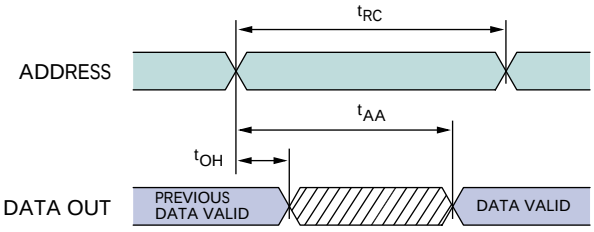
DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Read Cycle Time	^tRC	85		ns
Address Access Time	^tAA		85	ns
Chip Enable to Valid Output	^tCO		85	ns
Output Enable to Valid Output	^tOE		35	ns
Byte Select to Valid Output	^tLB, ^tUB		85	ns
Chip Enable to Low-Z Output	^tLZ	0		ns
Output Enable to Low-Z Output	^tOLZ	0		ns
Byte Select to Low-Z Output	^tLBZ, ^tUBZ	0		ns
Chip Enable to High-Z Output	^tHZ	0	15	ns
Output Disable to High-Z Output	^tOHZ	0	15	ns
Byte Select Disable to High-Z Output	^tLBHZ, ^tUBHZ	0	15	ns
Output Hold from Address Change	^tOH	5		ns

SRAM WRITE CYCLE TIMING

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Write Cycle Time	^tWC		85	ns
Chip Enable to End of Write	^tCW	50		ns
Address Valid to End of Write	^tAW	50		ns
Byte Select to End of Write	^tLBW, ^tUBW	50		ns
Address Setup Time	^tAS	0		ns
Write Pulse Width	^tWP	50		ns
Write Recovery Time	^tWR	0		ns
Write to High-Z Output	^tWHZ	0	15	ns
Data to Write Time Overlap	^tDW	50		ns
Data Hold from Write Time	^tDH	0		ns
End Write to Low-Z Output	^tOW	0		ns

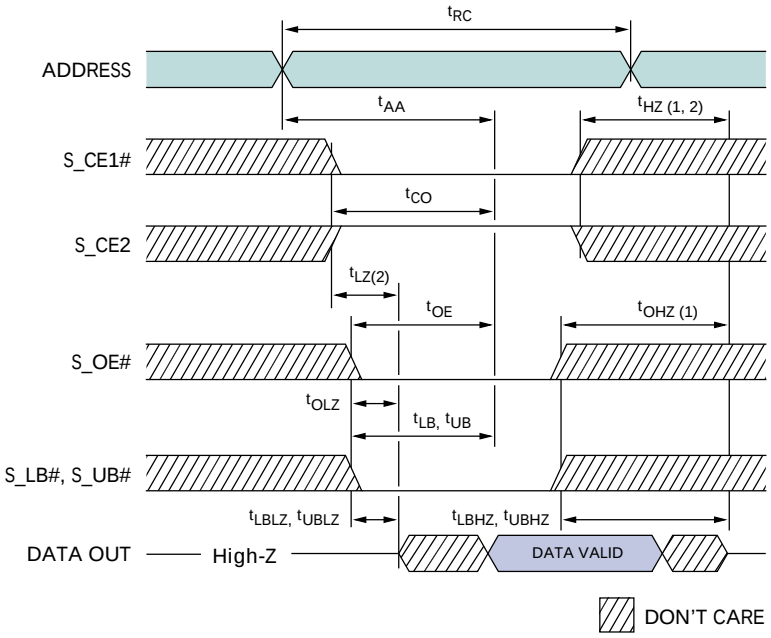
READ CYCLE 1

(S_CE1# = S_OE# = V_{IL}; S_CE2, S_WE# = V_{IH})



READ CYCLE 2

(S_WE# = V_{IH})

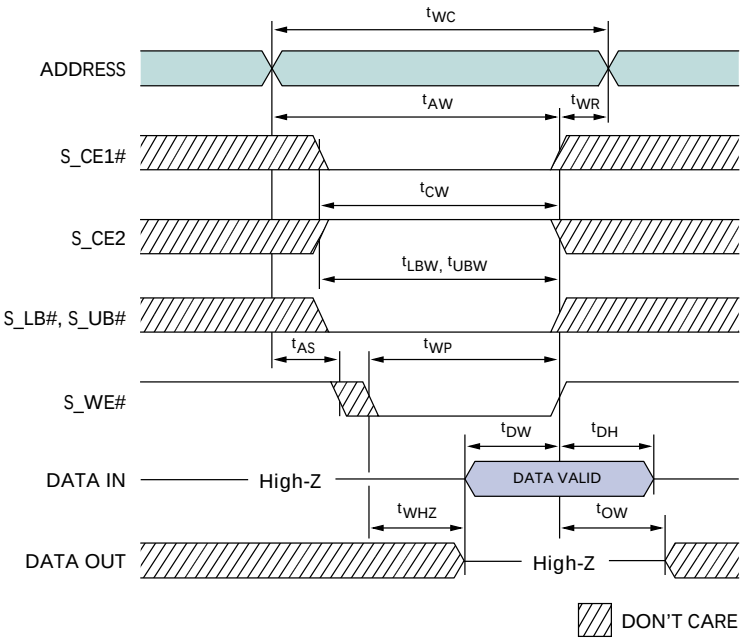


READ TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t_{RC}		85	ns
t_{AA}		85	ns
t_{CO}		85	ns
t_{OE}		35	ns
t_{LB}, t_{UB}		85	ns
t_{LZ}	0		ns

SYMBOL	MIN	MAX	UNITS
t_{OLZ}	0		ns
t_{HZ}	0	15	ns
t_{OHZ}	0	15	ns
t_{LBHZ}, t_{UBHZ}	0	15	ns
t_{OH}	5		ns

WRITE CYCLE
(S_WE# CONTROL)

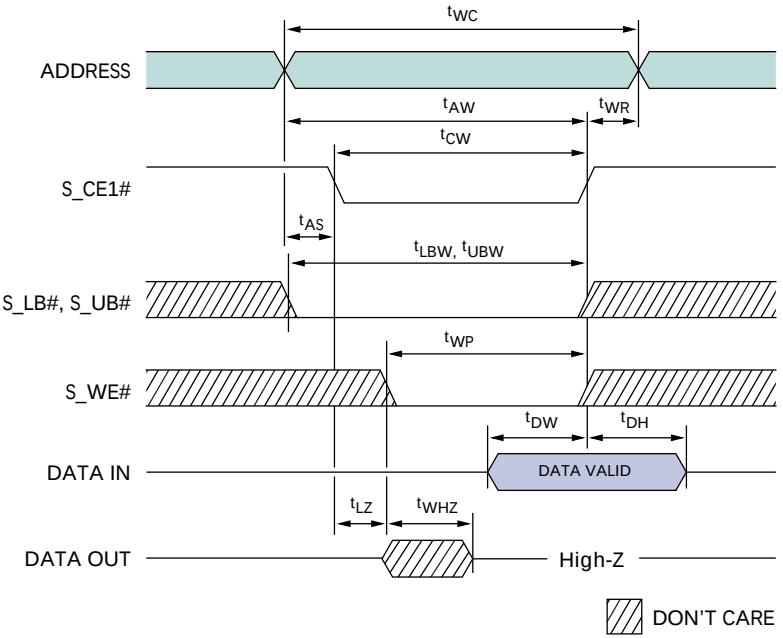


WRITE TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t_{WC}		85	ns
t_{CW}		85	ns
t_{AW}		85	ns
t_{LBW}, t_{UBW}		85	ns
t_{AS}	0		ns
t_{WP}	50		ns

SYMBOL	MIN	MAX	UNITS
t_{WR}	0		ns
t_{WHZ}	0	15	ns
t_{DW}	50		ns
t_{DH}	0		ns
t_{OW}	0		ns

WRITE CYCLE 2
(S_CE1# CONTROL)

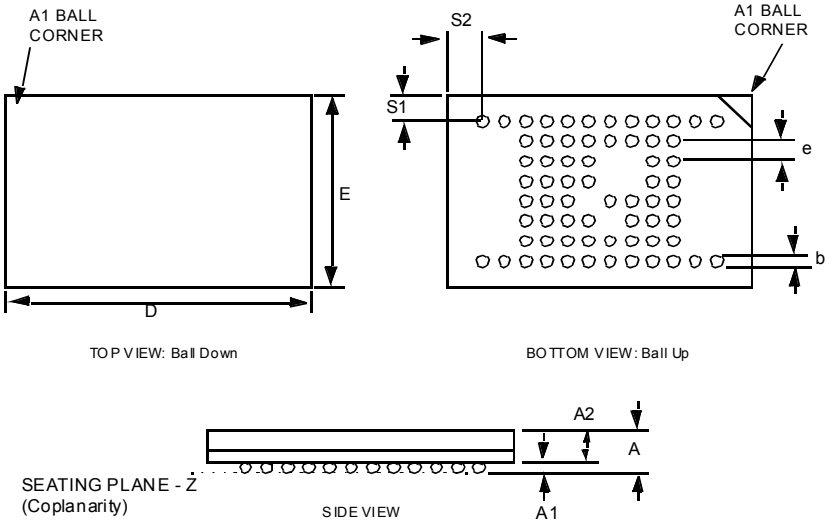


WRITE TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
tWC		85	ns
tCW		85	ns
tAW		85	ns
tLBW, tUBW		85	ns
tAS	0		ns
tWP	50		ns

SYMBOL	MIN	MAX	UNITS
tWR	0		ns
tWHZ	0	15	ns
tDW	50		ns
tDH	0		ns
tOW	0		ns

66-BALL FBGA



FBGA PACKAGE DIMENSIONS

		MIN	NOM	MAX
Package height	A	1.20	1.30	1.40
Solder ball height (Standoff)	A1	0.30	0.35	0.40
Package body thickness	A2	0.92	0.97	1.02
Ball lead diameter	b	0.325	0.40	0.475
Body length	D	11.90	12.00	12.10
Body width	E	7.90	8.00	8.10
Ball pitch	e		0.80	
Seating plane coplanarity	Z			0.10
Corner to first bump distance	S1	1.10	1.20	1.30
Corner to first bump distance	S2	1.50	1.60	1.70

All dimensions in millimeters.
Solder ball material: 63% Sn, 37% Pb
Substrate: plastic laminate
Mold compound: epoxy novolac

Revision History

Revision #	Date	Description
A	January 2001	Preliminary Release
B	May 8, 2001	Updated ballout, removed -11
C	November 2001	Part number change