NEL

NS GD E108A
11 Jan. 2001
PRELIMINARY

NLG4306
12.5 Gb/s 16 : 1 MUX

The NLG4306 is an ultra-fast 16:1 multiplexer. NLG4306 combines 16 parallel input signals operating at up to 781.25Mb/s into a single serial output signal as fast as 12.5 Gb/s (MIN.).
It was designed with LSCFL (Low-power Source Coupled FET Logic).
Owing to built-in 50-ohm termination resistors, external termination resistors are unnecessary for impedance matching.
The NLG4306 is fabricated using the 0.15-μm gate length A-SAINT (Advanced Self-Aligned Implantation for N^+ layer Technology) process.

FEATURES

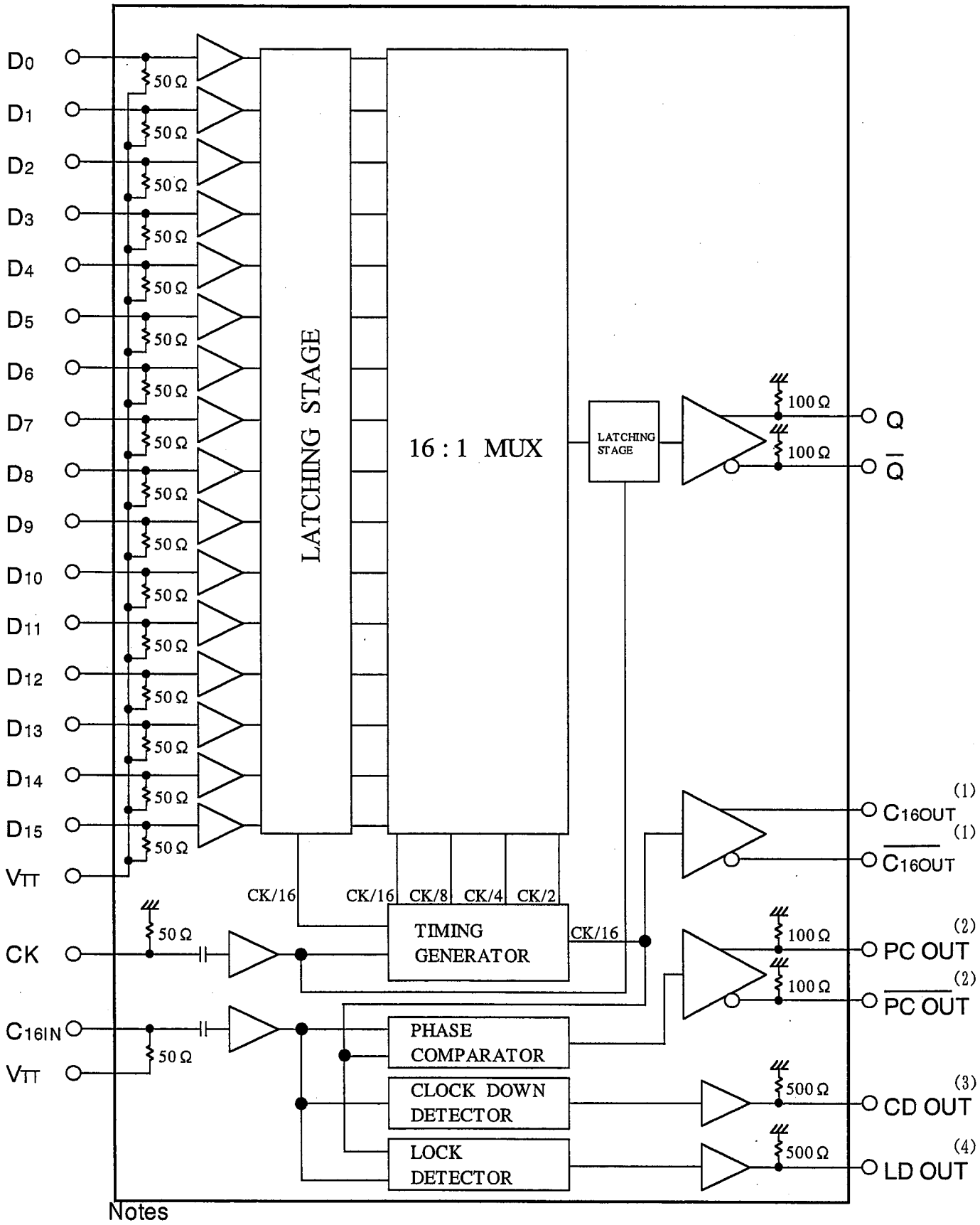
Ultra-high speed :	maximum clock frequency	f_{MAX}: 12.5 GHz [MIN.]
	minimum clock frequency	f_{MIN} : 5.0 GHz [MAX.]
	output rise time	tr = 35 ps (20-80%) [TYP.]
	output fall time	tf = 30 ps (20-80%) [TYP.]

High reliability : Hermetically-sealed package

APPLICATIONS

- Parallel-to-serial converters
- Pulse pattern generators
- Digital transmission system transmitters
- Computer links
- Board links

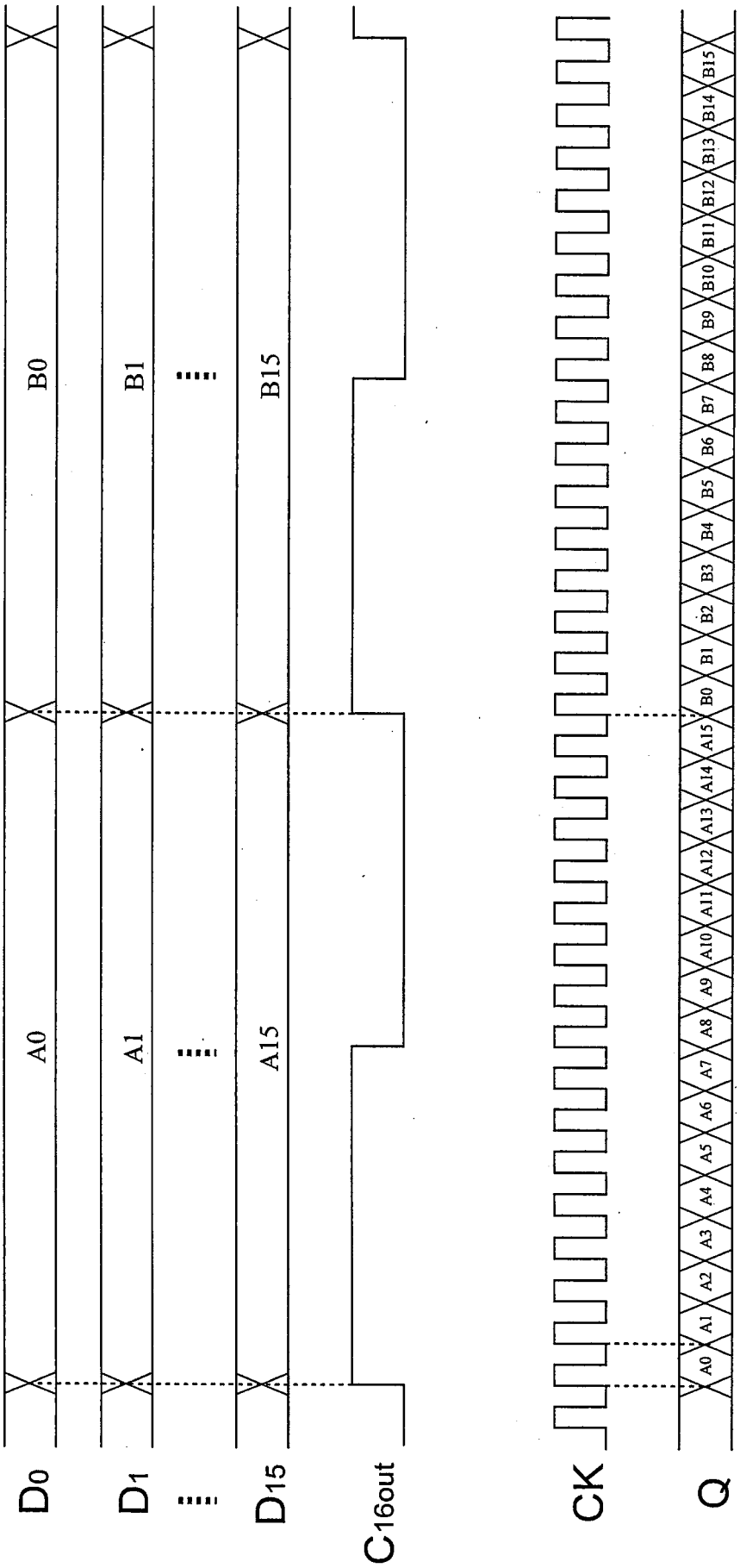
FUNCTIONAL DIAGRAM



Notes

(1) 1/16 clock output terminals. (ECL output)
(2) Phase comparator output terminals.
(3) Clock down detector output terminal.
(4) Lock detector output terminal.

TIMING CHART



PIN CONNECTION TABLE

No.	NAME	FUNCTION	No.	NAME	FUNCTION
1	GND	Ground (0.0V)	43	GND	Ground (0.0V)
2	V_{TT}	Input Signal Termination Power Supply (- 2.0 V)	44	V_{TT}	Input Signal Termination Power Supply (- 2.0 V)
3	GND	Ground (0.0V)	45	GND	Ground (0.0V)
4	D_1	1/16 Data Input 1	46	D_2	1/16 Data Input 2
5	GND	Ground (0.0V)	47	GND	Ground (0.0V)
6	D_9	1/16 Data Input 9	48	D_{10}	1/16 Data Input 10
7	GND	Ground (0.0V)	49	GND	Ground (0.0V)
8	D_5	1/16 Data Input 5	50	D_6	1/16 Data Input 6
9	GND	Ground (0.0V)	51	GND	Ground (0.0V)
10	D_{13}	1/16 Data Input 13	52	D_{14}	1/16 Data Input 14
11	GND	Ground (0.0V)	53	GND	Ground (0.0V)
12	D_{15}	1/16 Data Input 15	54	D_{12}	1/16 Data Input 12
13	GND	Ground (0.0V)	55	GND	Ground (0.0V)
14	D_7	1/16 Data Input 7	56	D_4	1/16 Data Input 4
15	GND	Ground (0.0V)	57	GND	Ground (0.0V)
16	D_{11}	1/16 Data Input 11	58	D_8	1/16 Data Input 8
17	GND	Ground (0.0V)	59	GND	Ground (0.0V)
18	D_3	1/16 Data Input 3	60	D_0	1/16 Data Input 0
19	GND	Ground (0.0V)	61	GND	Ground (0.0V)
20	V_{TT}	Input Signal Termination Power Supply (- 2.0 V)	62	V_{SS}	Power Supply (- 3.5 V)
21	GND	Ground (0.0V)	63	GND	Ground (0.0V)
22	GND	Ground (0.0V)	64	GND	Ground (0.0V)
23	V_{ref01}	1/16 Data Input Ref. 1 (1)	65	LD OUT	Lock Detecter Output (6)
24	GND	Ground (0.0V)	66	GND	Ground (0.0V)
25	V_{SS}	Power Supply (- 3.5 V)	67	$\overline{\text{PC OUT}}$	Phase Comparator Output (Comp.) (5)
26	GND	Ground (0.0V)	68	GND	Ground (0.0V)
27	V_{ref1}	Clock Input Ref. (3)	69	PC OUT	Phase Comparator Output (True) (5)
28	GND	Ground (0.0V)	70	GND	Ground (0.0V)
29	CK	Clock Input	71	$\overline{\text{C16OUT}}$	1/16 Clock Output (Comp.) (7)
30	GND	Ground (0.0V)	72	GND	Ground (0.0V)
31	V_{SS}	Power Supply (- 3.5 V)	73	C16OUT	1/16 Clock Output (True) (7)
32	GND	Ground (0.0V)	74	GND	Ground (0.0V)
33	Q	Data Output (True) (5)	75	V_{SS}	Power Supply (- 3.5 V)
34	GND	Ground (0.0V)	76	GND	Ground (0.0V)
35	$\overline{Q}$	Data Output (Comp.) (5)	77	C16IN	1/16 Clock Input
36	GND	Ground (0.0V)	78	GND	Ground (0.0V)
37	V_{SS}	Power Supply (- 3.5 V)	79	V_{ref2}	1/16 Clock Input Ref. (4)
38	GND	Ground (0.0V)	80	GND	Ground (0.0V)
39	V_{ref02}	1/16 Data Input Ref. 2 (2)	81	CD OUT	1/16 Clock Down Detector Output (6)
40	GND	Ground (0.0V)	82	GND	Ground (0.0V)
41	TCMON	Case Temperature Monitor	83	V_{SS}	Power Supply (- 3.5 V)
42	GND	Ground (0.0V)	84	GND	Ground (0.0V)

Notes

See Page 5.

PIN CONNECTION TABLE

Notes

(1) V_{ref01} : Internally generated reference voltage that determines the data input (D_1, D_3, D_5, D_7, D_9, D_{11}, D_{13}, D_{15}) threshold level. By applying - 1.6 to - 1.0V externally to this pin, an arbitrary data input threshold voltage can be established.

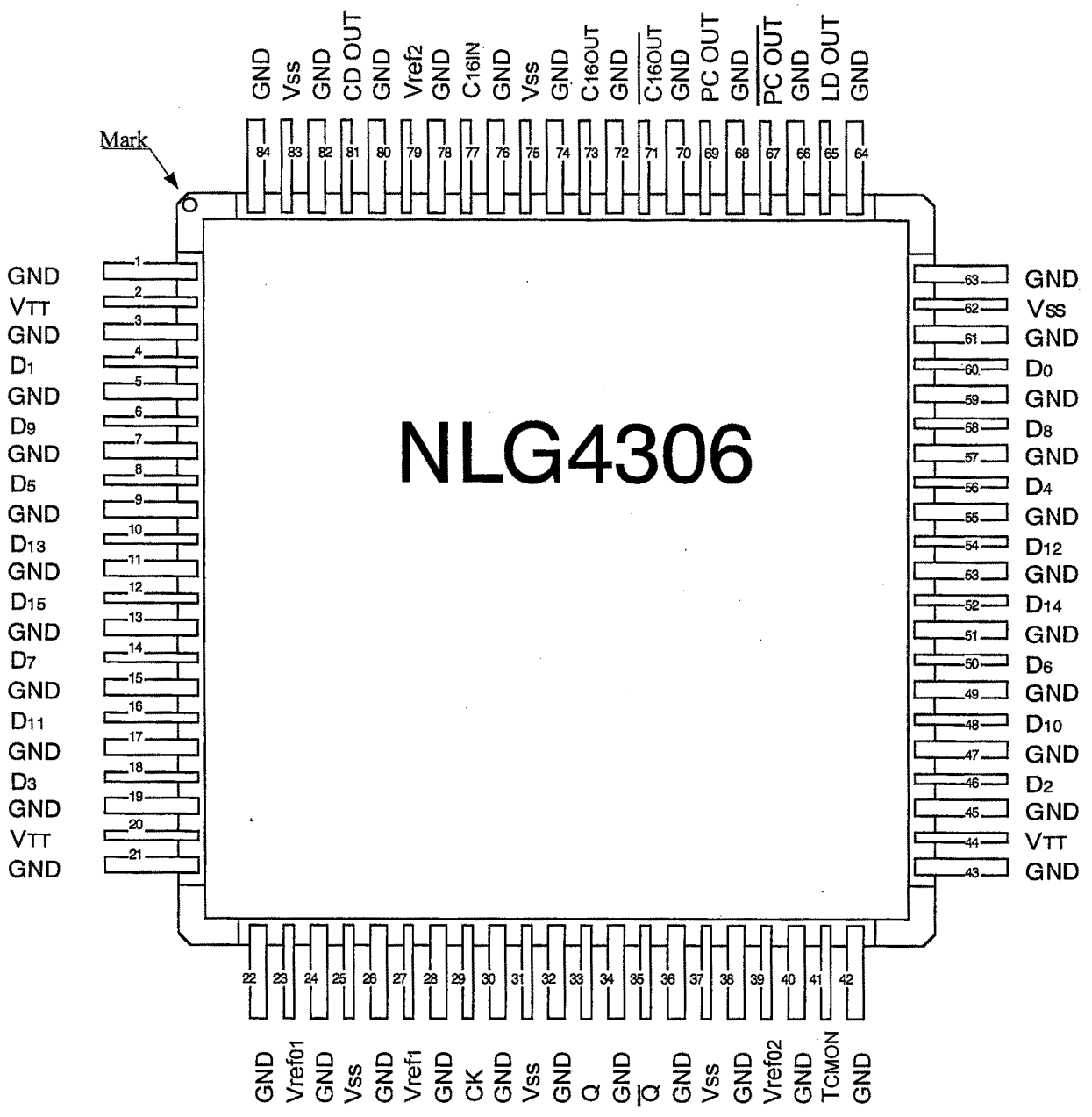
(2) V_{ref02} : Internally generated reference voltage that determines the data input (D_0, D_2, D_4, D_6, D_8, D_{10}, D_{12}, D_{14}) threshold level. By applying - 1.6 to - 1.0V externally to this pin, an arbitrary data input threshold voltage can be established.

(3) V_{ref1} : Internally generated reference voltage that determines the clock input threshold level. By applying - 2.1 to - 1.55 V externally to this pin, an arbitrary clock input threshold voltage can be established.

(4) V_{ref2} : Internally generated reference voltage that determines the 1/16 clock input threshold level. By applying - 2.05 to - 1.47 V externally to this pin, an arbitrary 1/16 clock input threshold voltage can be established.

(5) Terminate unused output pins to GND through 50-ohm resistors.
(6) Terminate unused output pins to GND through 500-ohm resistor.
(7) Terminate unused output pins to -2 V through 50-ohm resistors.

CONNECTION DIAGRAM (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
Vss	Power Supply Voltage	+0.5 V ~ - 4.0 V
VTT	Termination Voltage	+0.5 V ~ - 2.5 V
Vin	Applied Voltage Amplitude at Clock Inputs (CK, C16IN)	1.6 Vp-p
Vindin	Applied Voltage at Data Inputs (D0 ~ D15)	+0.3 V ~ - 2.5 V
Vinck1	Applied Voltage at Clock Input (CK)	+ 1.6 V ~ - 1.6 V
Vinck2	Applied Voltage at 1/16 Clock Input (C16IN)	+0.3 V ~ - 2.5 V
Vout	Applied Voltage at Signal Outputs (Q, $\overline{Q}$, PC OUT, $\overline{PC\ OUT}$, CD OUT, LD OUT)	+0.2 V ~ - 1.75 V
VoutE	Applied Voltage at Signal Outputs (C16OUT, $\overline{C16OUT}$)	+0.2 V ~ - 2.5 V
Vref01, Vref02	Applied Voltage at Vref01 and Vref02 pins	+0.3 V ~ - 2.5 V
Vref1, Vref2	Applied Voltage at Vref1 and Vref2 pins under Bias	- 1.0 V ~ - 2.5 V
VTCMON	Applied Voltage at Case Temperature Monitor pin	- 1.0 V ~ + 1.0 V
Tstor	Storage Temperature	- 60 ℃ ~ +150 ℃
Tc (1)	Case Temperature under Bias	- 60 ℃ ~ +125 ℃

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Vss	Power Supply Voltage	- 3.75	- 3.5	- 3.4	V
VTT	Termination Voltage		- 2.0		V
Vref01, Vref02	Data Input Reference Voltage	Adjust in the range from -1.6 V to -1.0 V			V
Vref1	Clock Input Reference Voltage	Normally Open			V
Vref2	1/16 Clock Input Reference Voltage	Normally Open			V
Dn (n = 0~15)	Data Input Interface	DC Coupling 50 Ω to VTT (See DC Characteristics)			—
CK	Clock Input Interface	DC Coupling (See DC Characteristics) or AC Coupling (See AC Characteristics)			—
C16IN	1/16 Clock Input Interface	DC Coupling 50 Ω to VTT (See pages 10, 11)			—
OUT	Data Output, Phase Comparator Output Interface (Q, $\overline{Q}$, PC OUT, $\overline{PC\ OUT}$)	DC Coupling, Terminate to GND through 50 Ω			—
	1/16 Clock Output Interface (C16OUT, $\overline{C16OUT}$)	DC Coupling, Terminate to VTT through 50 Ω			—
	Clock Down Detector Output Interface (CD OUT)	DC Coupling, Terminate to GND through 500 Ω			—
	Lock Detector Output Interface (LD OUT)	DC Coupling, Terminate to GND through 500 Ω			—
TCMON	Case Temperature Monitor	Connect to a DC voltmeter for estimating case temperature. Relationship between TCMON and case temperature is shown in page 22.			—

Notes

(1) Tc : temperature at package base.

DC CHARACTERISTICS

(VSS = -3.75 V ~ -3.4 V, VTT = -2.0 V, GND = 0.0 V, Tc = 0 ~ 75℃ (1))

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
V_{OH}	Output Voltage, High (Q, $\overline{Q}$)	-0.15	0.0		V	
V_{OL}	Output Voltage, Low (Q, $\overline{Q}$)		-0.9	-0.80	V	
V_{OHE}	Output Voltage, High (C_{16OUT}, $\overline{C_{16OUT}}$)	-0.98	-0.75		V	
V_{OLE}	Output Voltage, Low (C_{16OUT}, $\overline{C_{16OUT}}$)		-1.8	-1.74	V	
V_{IH}	Input Voltage, High (CK)	-0.1	0.0		V	
V_{IL}	Input Voltage, Low (CK)		-0.9	-0.8	V	
V_{IHE}	Input Voltage, High (D_0 ~ D_{15})	-1.17	-0.9		V	
V_{ILE}	Input Voltage, Low (D_0 ~ D_{15})	V_{TT}	-1.7	-1.48	V	
I_{SS}	Power Supply Current (V_{SS})		1.2	1.77	A	
I_{TT}	Power Supply Current (V_{TT})		0.24	0.53 (2)	A	
Pd	Power Dissipation		4.2	6.64	W	(3)

AC CHARACTERISTICS

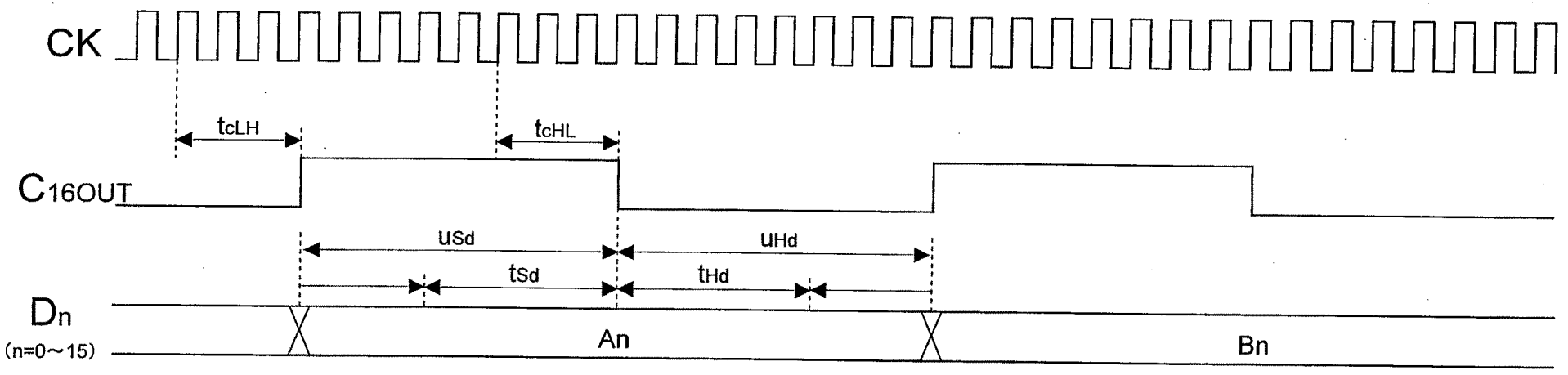
(VSS = -3.75 V~ -3.4 V, VTT = -2.0 V, GND = 0.0 V, Tc = 0 ~ 75℃ (1), Vref01 : Adjust in the range from -1.6 V to -1.0 V, Vref02 : Adjust in the range from -1.6 V to -1.0 V, Vrefl : Open, Vref2 : Open)

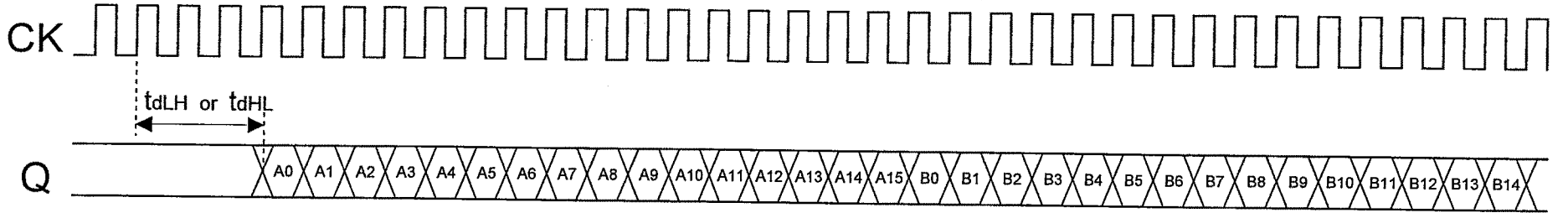
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
Vin	Minimum Clock Input Voltage Amplitude (CK)			0.7	Vp-p	
V_{OH}	Output Voltage, High (Q, $\overline{Q}$)	-0.13	0.0		V	
V_{OL}	Output Voltage, Low (Q, $\overline{Q}$)		-0.9	-0.82	V	
Vamp	Output Voltage Amplitude (Q, $\overline{Q}$)	0.76	1.00		Vp-p	
f_{MAX}	Maximum Clock Frequency	12.5			GHz	(4)
f_{MIN}	Minimum Clock Frequency			5.0	GHz	
tr	Output Rise Time (Q, $\overline{Q}$ 20-80%)		35	50	ps	
tf	Output Fall Time (Q, $\overline{Q}$ 20-80%)		30	45	ps	
trc	Output Rise Time (C_{16OUT}, $\overline{C_{16OUT}}$ 20-80%)		180	300	ps	
tfc	Output Fall Time (C_{16OUT}, $\overline{C_{16OUT}}$ 20-80%)		110	200	ps	
tdLH	Output Rise Delay (CK - Q, $\overline{Q}$)	375	415	450	ps	(5)
tdHL	Output Fall Delay (CK - Q, $\overline{Q}$)	375	415	450	ps	(5)
tcLH	Output Rise Delay (CK - C_{16OUT}, $\overline{C_{16OUT}}$)	560	630	705	ps	(5)
tcHL	Output Fall Delay (CK - C_{16OUT}, $\overline{C_{16OUT}}$)	555	630	710	ps	(5)
tSd	Minimum Setup Time (Dn - C_{16OUT})		0.38	0.45	ns	(5)
tHd	Minimum Hold Time (C_{16OUT} - Dn)		-0.19	-0.10	ns	(5)
PM	Phase Margin	280			deg.	(6)

Notes

(1) Tc : temperature at package base.
(2) I_{TT} (MAX.) : D_0 ~ D_{15}, C_{16IN} = -0.8 V
(3) Pd = Vss × Iss. Excludes current through input termination resistors and ECL output FETs.
(4) Confirmed by error-free operation using a pseudo-random pattern having a word length of 2^{23}-1 bits.
(5) See page 9.
(6) PM={ (1 / f) - (tsd + thd) } × f × 360

TIMING CHART (INCLUDING DELAY TIMES)





(See the timing chart on page 3 for a more complete logical description. Here, tsd and tHd are the minimum setup and hold times as defined on the previous page; usd and uHd are the corresponding user setup and hold times.)

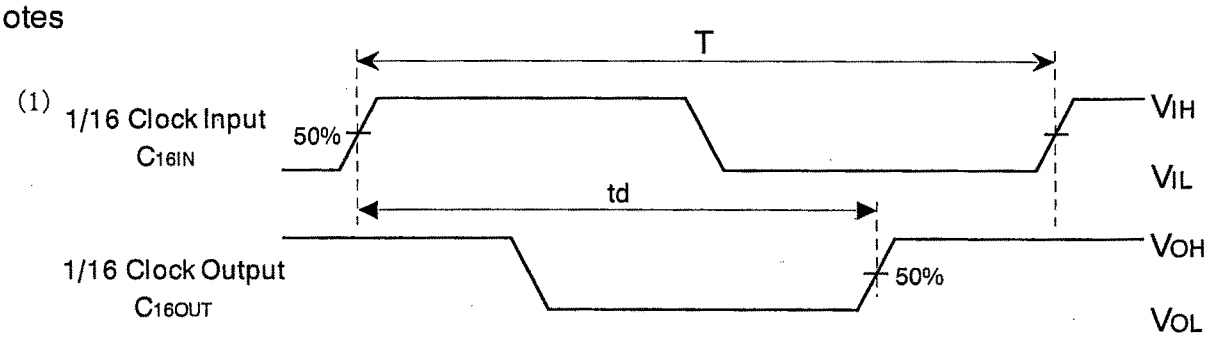
PHASE COMPARATOR CHARACTERISTICS

(VSS = -3.75 V ~ -3.4 V, VTT = -2.0 V, GND = 0.0 V, Tc = 0 ~ 75℃, Vref01 : Adjust in the range from -1.6 V to -1.0 V, Vref02 : Adjust in the range from -1.6 V to -1.0V, Vrefl : Open, Vref2 : Open, C16IN=0.8Vp-p)

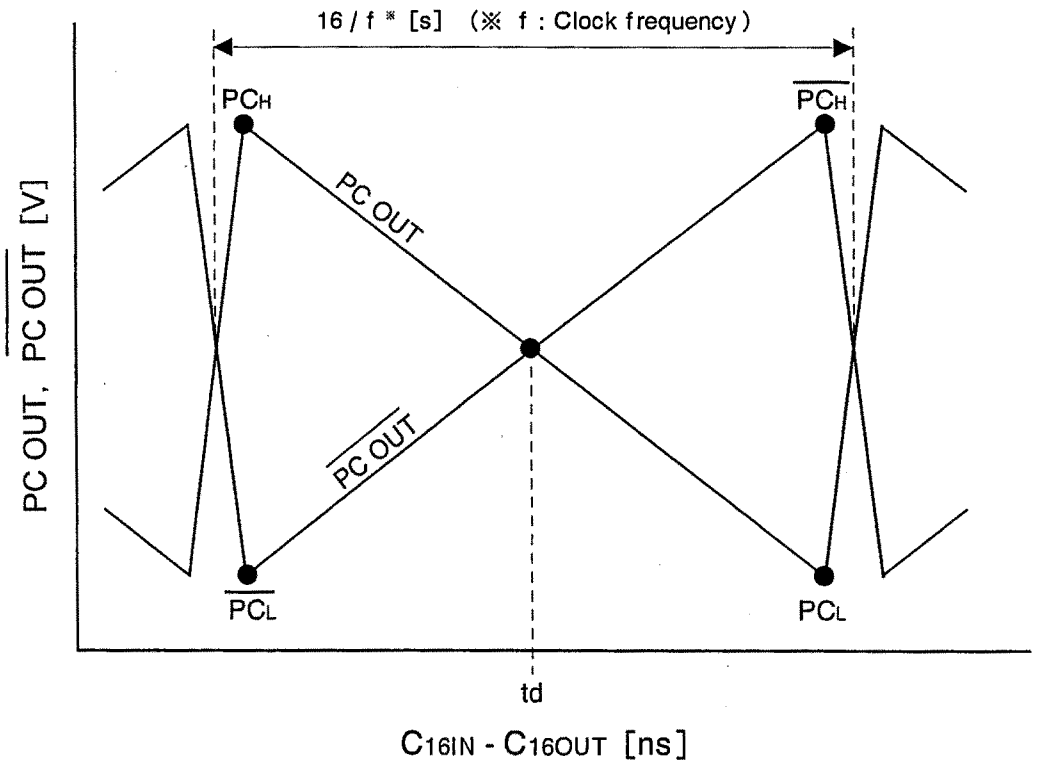
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
td	1/16 Clock Delay (C16IN - C16OUT)	T/2+0.25	T/2+0.4	T/2+0.55	ns	(1),(2)
PC_H	Phase Comparator Output Voltage, High (PC OUT)	-0.2	-0.1		V	(2)
PC_L	Phase Comparator Output Voltage, Low (PC OUT)		-1.20	-0.75	V	(2)
$\overline{PC_H}$	Phase Comparator Output Voltage, High ($\overline{PC\ OUT}$)	-0.2	-0.1		V	(2)
$\overline{PC_L}$	Phase Comparator Output Voltage, Low ($\overline{PC\ OUT}$)		-1.20	-0.75	V	(2)

Notes

(1)



(2)



CLOCK DOWN DETECTOR CHARACTERISTICS

(VSS = -3.75 V ~ -3.4 V, VTT = -2.0 V, GND = 0.0 V, Tc = 0 ~ 75℃, Vref01 : Adjust in the range from -1.6 V to -1.0 V, Vref02 : Adjust in the range from -1.6 V to -1.0 V, Vref1 : Open, Vref2 : Open)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
CD_H	Clock Down Detector Output Voltage, High	-0.3	-0.2		V	(1)
CD_L	Clock Down Detector Output Voltage, Low		-0.7	-0.45	V	(2)

Notes

(1) Measurement Condition
1/16 clock input amplitude : C_{16IN} = 0.8 Vp-p

(2) Measurement Condition
1/16 clock input amplitude : C_{16IN} = 0 Vp-p

LOCK DETECTOR CHARACTERISTICS

(VSS = -3.75 V ~ -3.4 V, VTT = -2.0 V, GND = 0.0 V, Tc = 0 ~ 75℃, Vref01 : Adjust in the range from -1.6 V to -1.0 V, Vref02 : Adjust in the range from -1.6 V to -1.0 V, Vref1 : Open, Vref2 : Open, C16IN=0.8Vp-p)

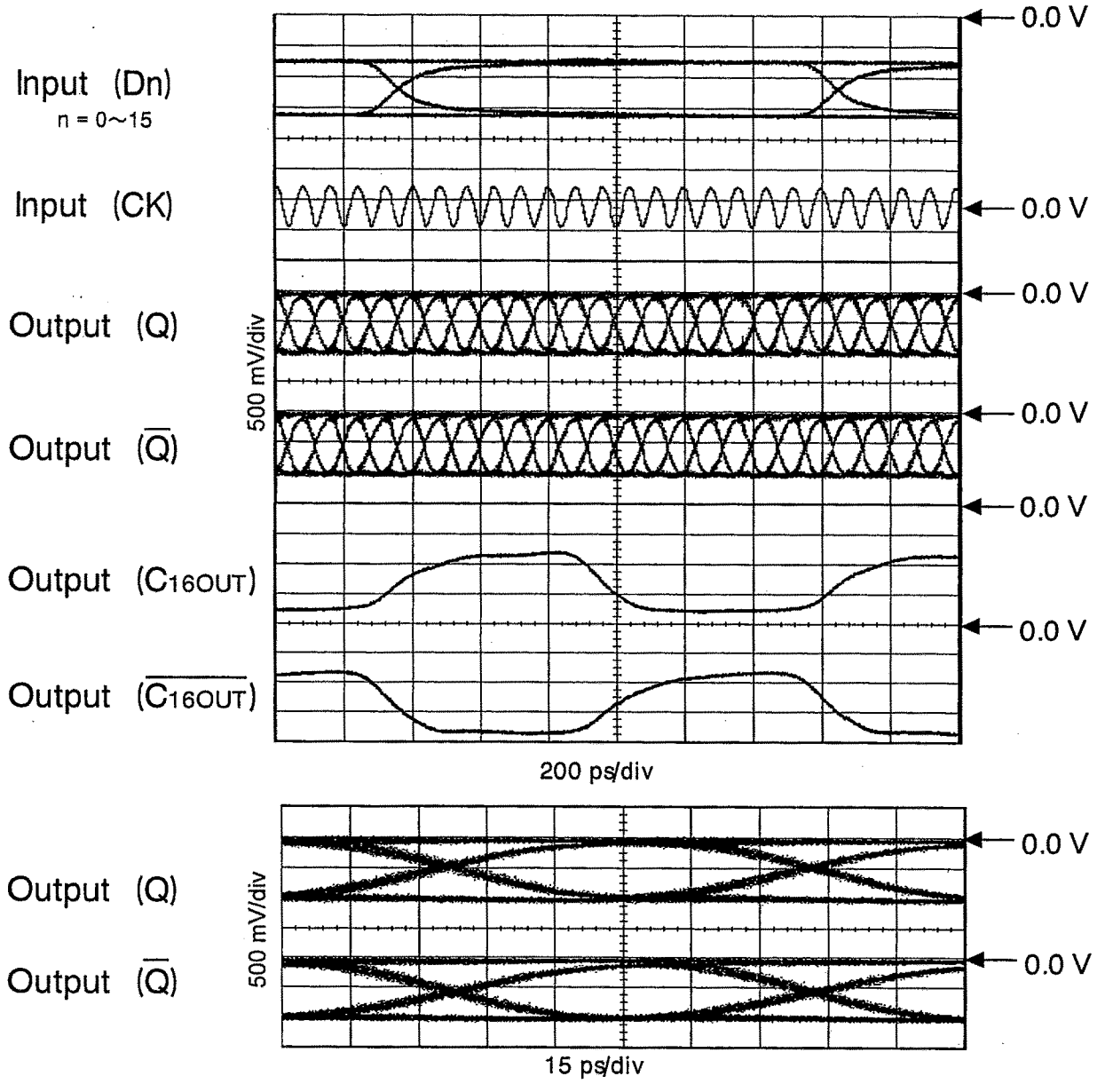
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
LD_H	Lock Detector Output Voltage High	-0.10	-0.05		V
LD_L	Lock Detector Output Voltage Low		-1.40	-1.00	V

Notes

FUNCTION	SYNBOL
fin × m = fout × n (m,n:integer)	LD_H or LD_L
fin ≠ fout fout/2<fin<fout×2	$\frac{LD_H + LD_L}{2}$

fin : C16in frequency [GHz]
fout : C16out frequency [GHz]

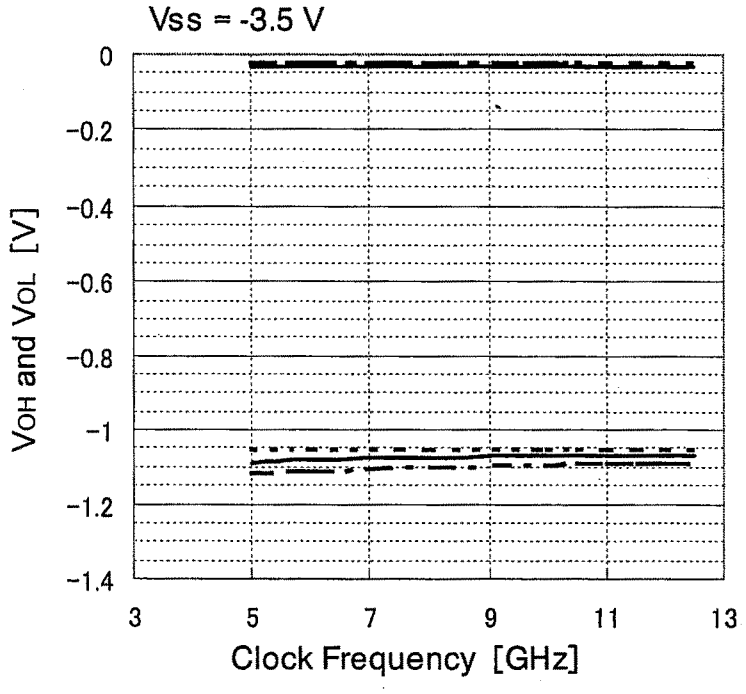
INPUT AND OUTPUT WAVEFORMS (12.5 Gb/s)



Measurement Conditions

Vss = - 3.5 V
VTT = -2.0 V
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Dn (n=0~15) : 781.25 Mb/s, PN = 31, VIH = - 1.0 V, VIL = - 1.7 V
CK : 12.5 GHz, Vin = 0.7 Vp-p, AC coupling,
Tc = 75℃
Data outputs connected to the 50-ohm impedance pins of a sampling oscilloscope.
ECL outputs (C16OUT, $\overline{\text{C16OUT}}$) connected to the 50-ohm impedance pins of a sampling oscilloscope via ECL terminators. Results given here were obtained using the NEL test fixture.

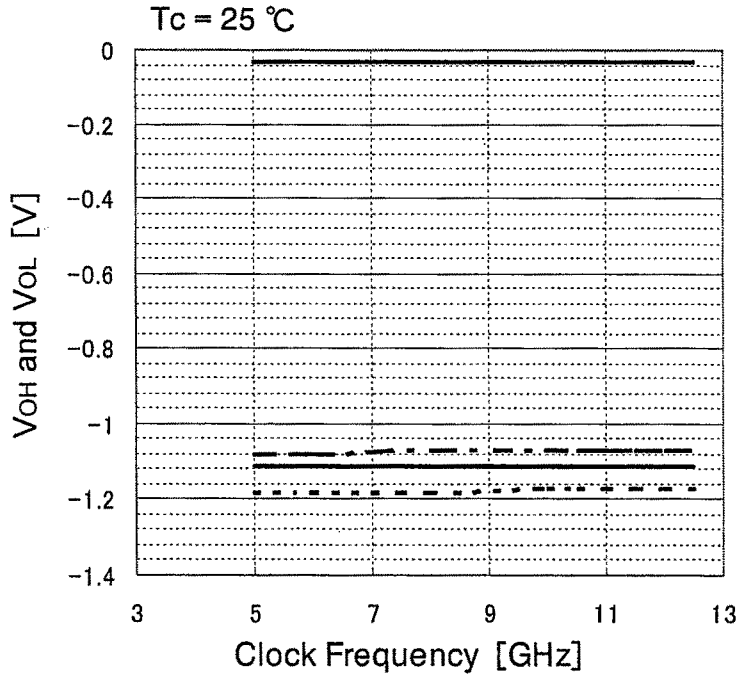
SAMPLE AC CHARACTERISTICS (Q, $\overline{Q}$)



—·—·— : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 75 ℃

Measurement Conditions

V_{TT} = -2.0 V
Dn : V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : Vin = 0.7 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

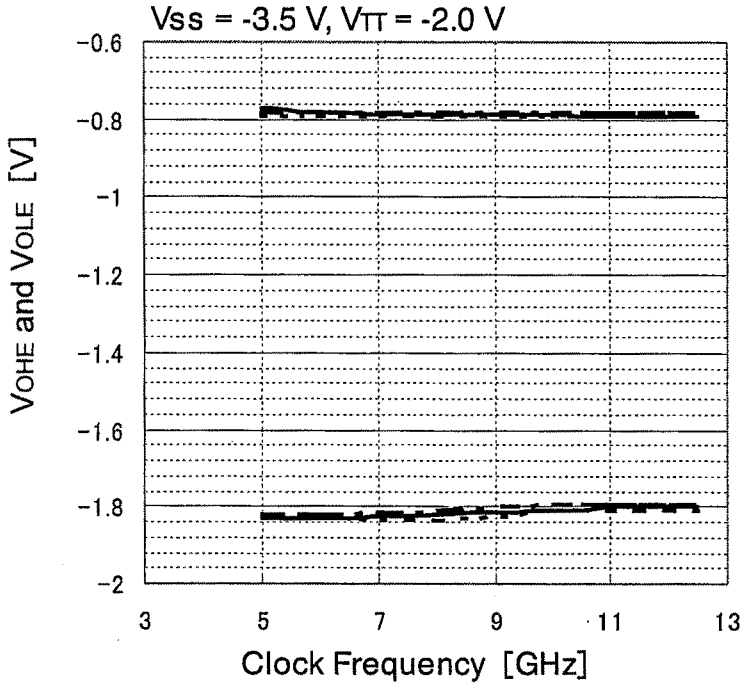


—·—·— : Vss = - 3.4 V
——— : Vss = - 3.5 V
- - - - - - : Vss = - 3.75 V

Measurement Conditions

V_{TT} = -2.0 V
Dn : V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : Vin = 0.7 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

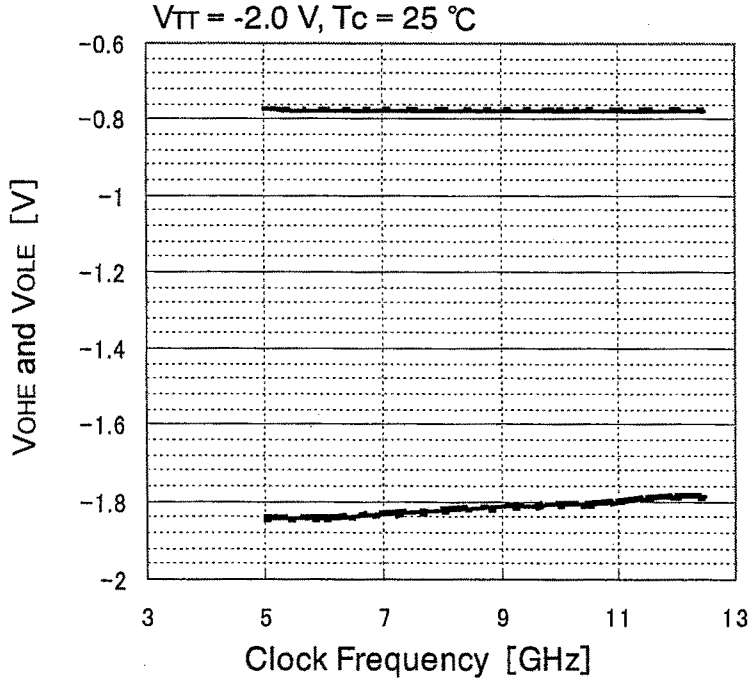
SAMPLE AC CHARACTERISTICS (C16OUT, $\overline{C16OUT}$)



—·—·— : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 75 ℃

Measurement Conditions

Dn : V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : Vin = 0.7 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

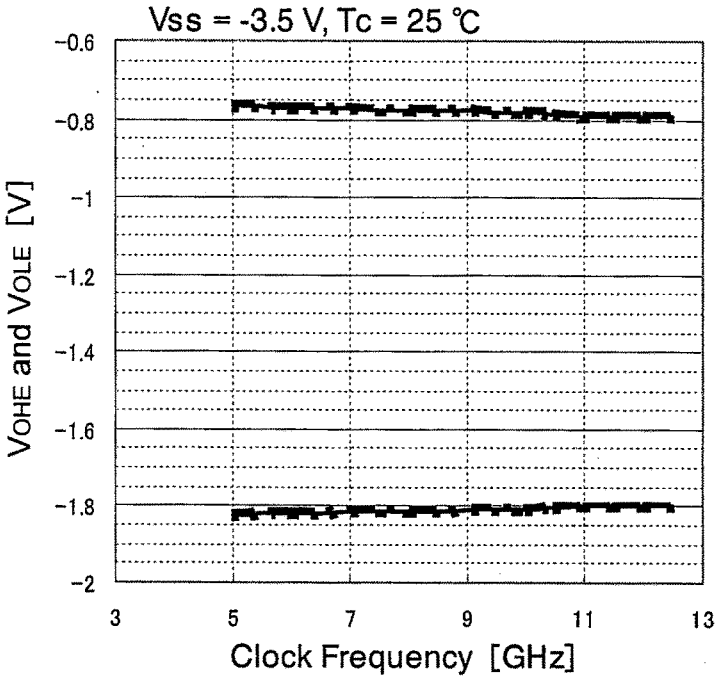


—·—·— : Vss = - 3.4 V
——— : Vss = - 3.5 V
- - - - - - : Vss = - 3.75 V

Measurement Conditions

Dn : V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : Vin = 0.7 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

SAMPLE AC CHARACTERISTICS (C16OUT, $\overline{C16OUT}$)

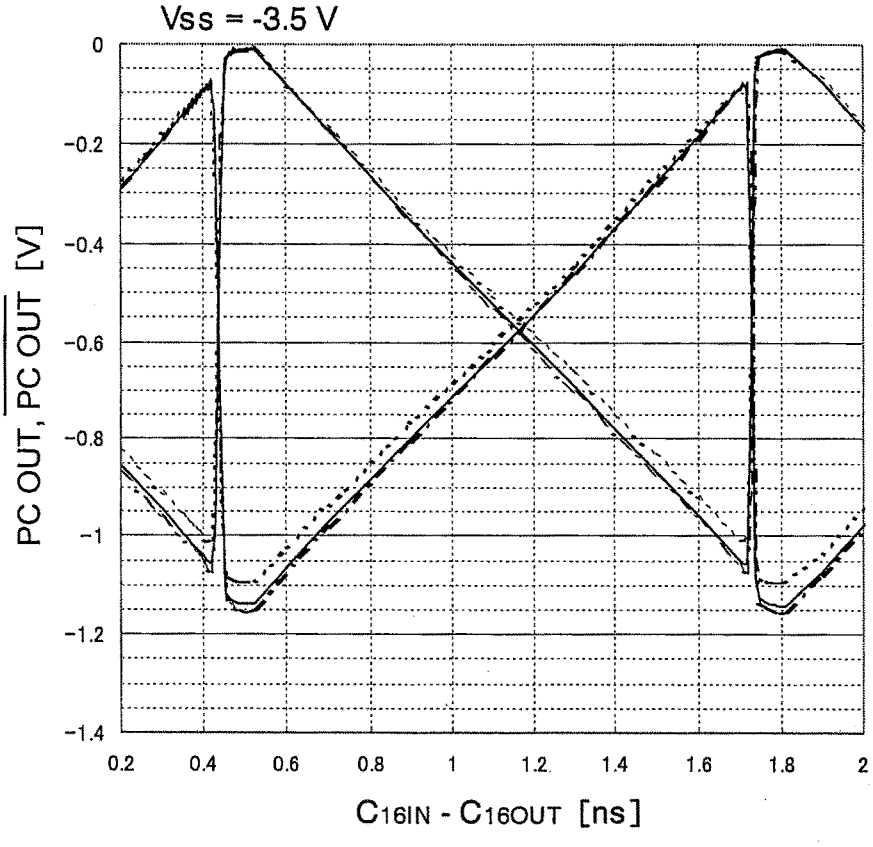


—·—·—· : V_{TT} = - 1.9 V
——— : V_{TT} = - 2.0 V
- - - - - - : V_{TT} = - 2.1 V

Measurement Conditions

Dn : V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : Vin = 0.7 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

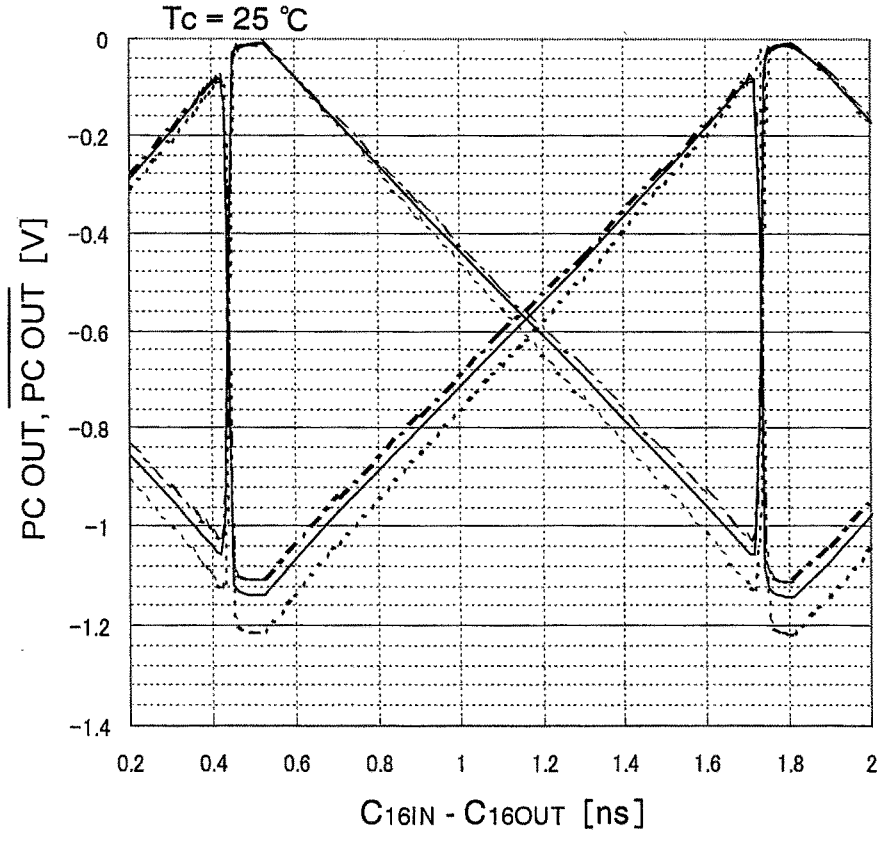
SAMPLE PHASE COMPARATOR CHARACTERISTICS



—·—·—· : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 75 ℃

Measurement Conditions

V_{TT} = -2.0 V
Dn : 781.25 Mb/s,
V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : 12.5 GHz, Vin = 0.7 Vp-p
C_{16IN} : 781.25 MHz,Vin = 0.8 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

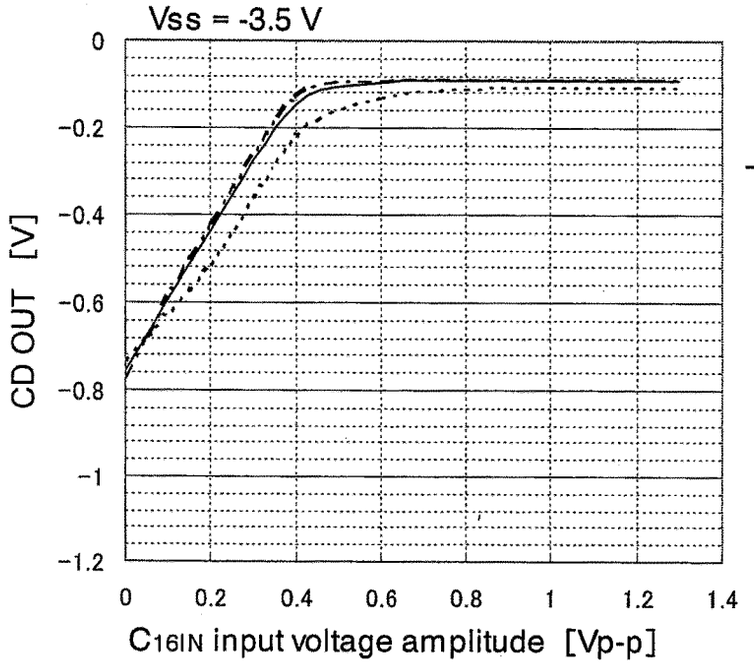


—·—·—· : Vss = -3.4 V
——— : Vss = -3.5 V
- - - - - - : Vss = -3.75 V

Measurement Conditions

V_{TT} = -2.0 V
Dn : 781.25 Mb/s,
V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : 12.5 GHz, Vin = 0.7 Vp-p
C_{16IN} : 781.25 MHz,Vin = 0.8 Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

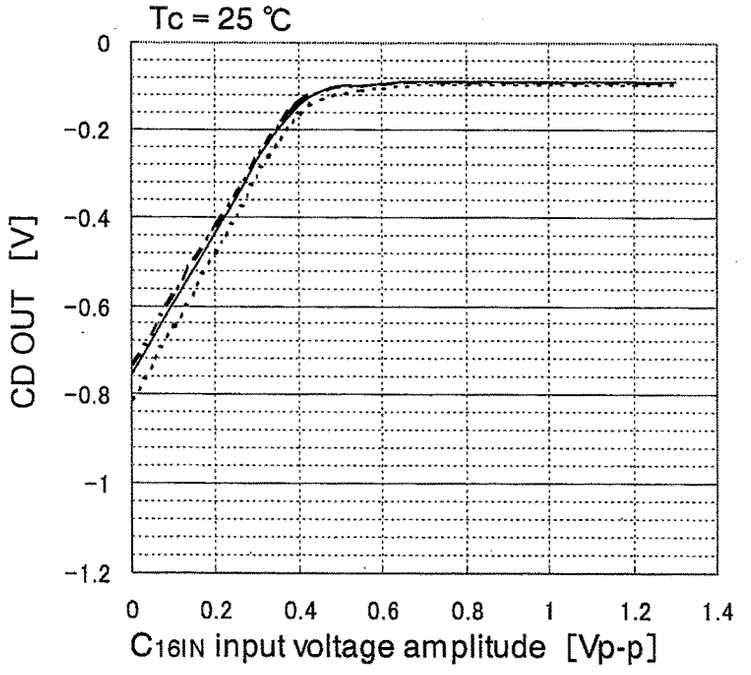
SAMPLE CLOCK DOWN DETECTOR CHARACTERISTICS



—·—·—· : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 75 ℃

Measurement Conditions

V_{TT} = -2.0 V
Dn : 781.25 Mb/s,
V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : 12.5 GHz, Vin = 0.7 Vp-p
C_{16IN} : 781.25 MHz
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

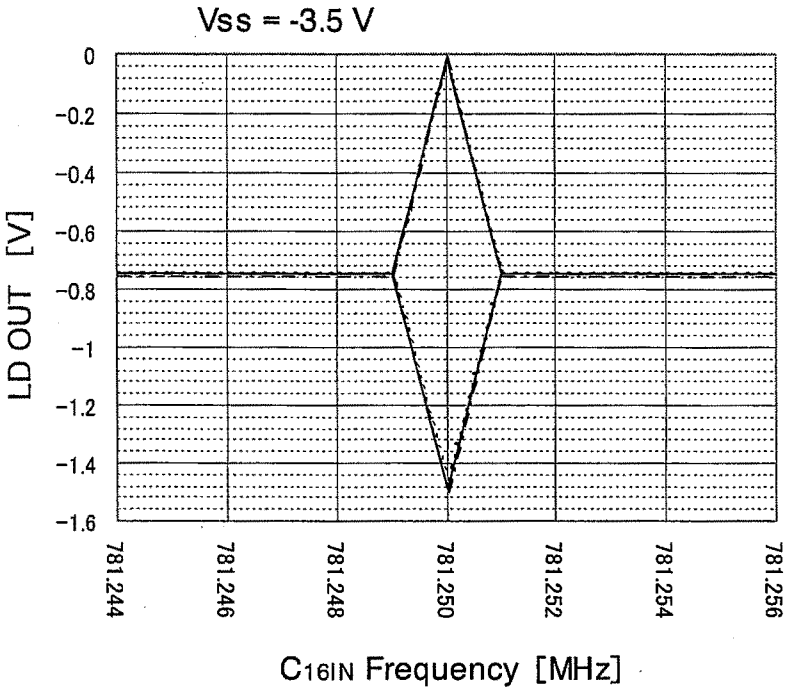


—·—·—· : Vss = - 3.4 V
——— : Vss = - 3.5 V
- - - - - - : Vss = - 3.75 V

Measurement Conditions

V_{TT} = -2.0 V
Dn : 781.25 Mb/s,
V_{IH} = -1.0 V, V_{IL} = -1.7 V
CK : 12.5 GHz, Vin = 0.7 Vp-p
C_{16IN} : 781.25 MHz
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

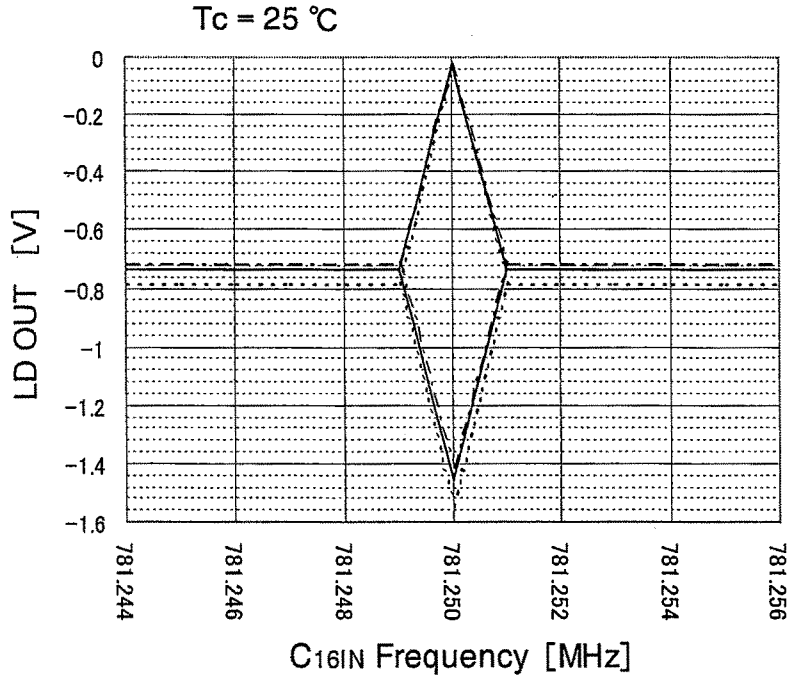
SAMPLE LOCK DETECTOR CHARACTERISTICS



—·—·— : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 75 ℃

Measurement Conditions

VTT = -2.0 V
CK : 12.5 GHz, Vin = 0.7 Vp-p
C16in=0.8Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

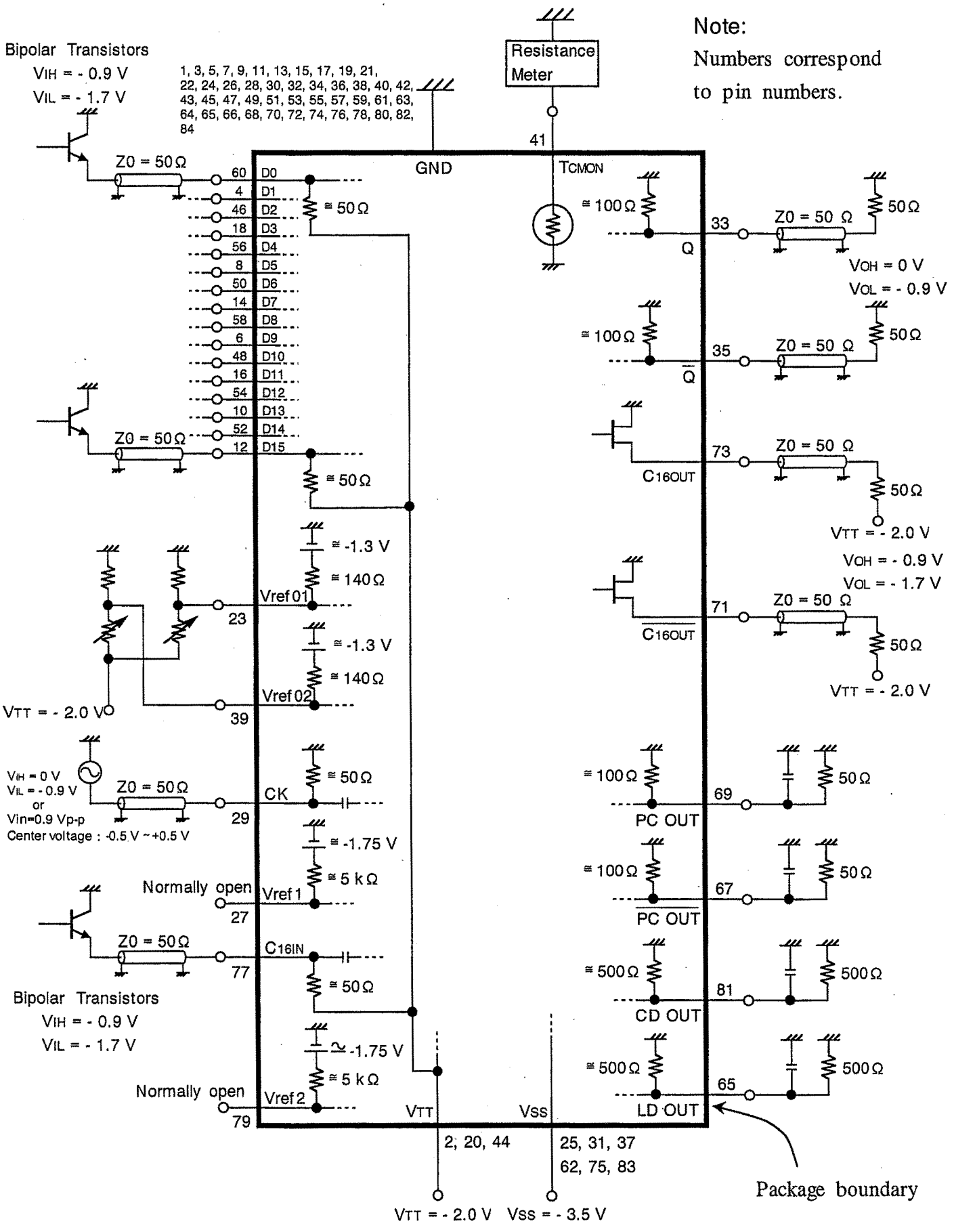


—·—·— : Vss = - 3.4 V
——— : Vss = - 3.5 V
- - - - - - : Vss = - 3.75 V

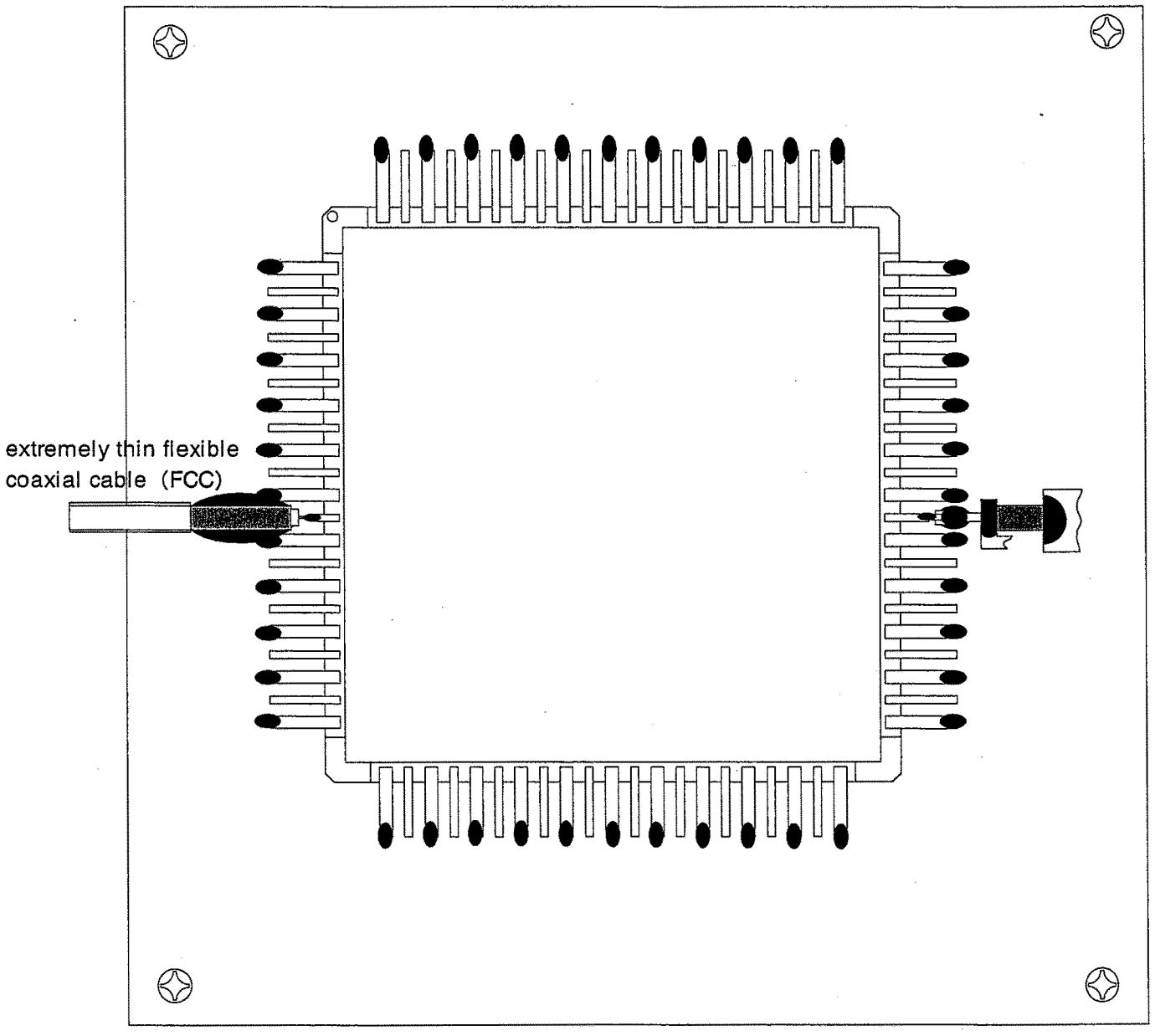
Measurement Conditions

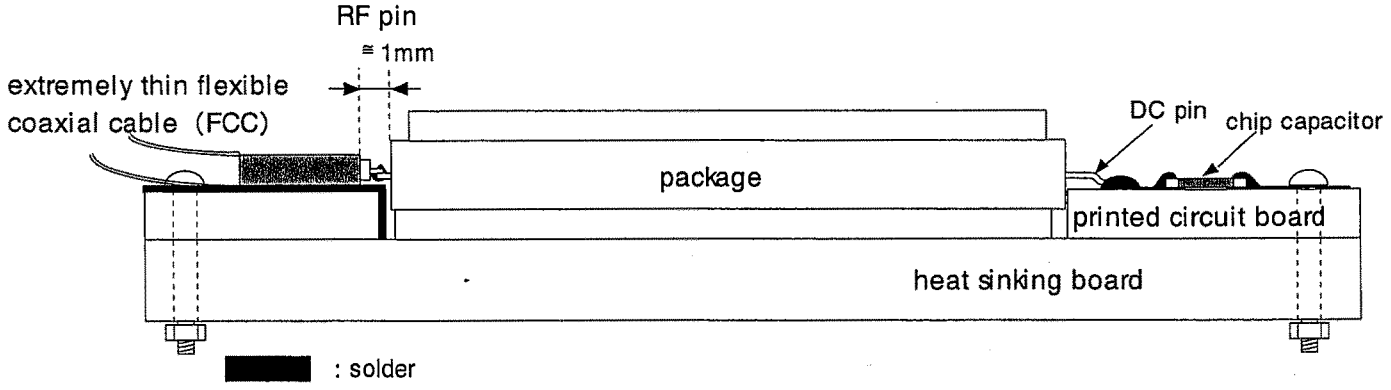
VTT = -2.0 V
CK : 12.5 GHz, Vin = 0.7 Vp-p
C16in=0.8Vp-p
Vref01 : Open
Vref02 : Open
Vref1 : Open
Vref2 : Open
Results given here were obtained using the NEL test fixture.

SAMPLE IMPLEMENTATION



SAMPLE MOUNTING

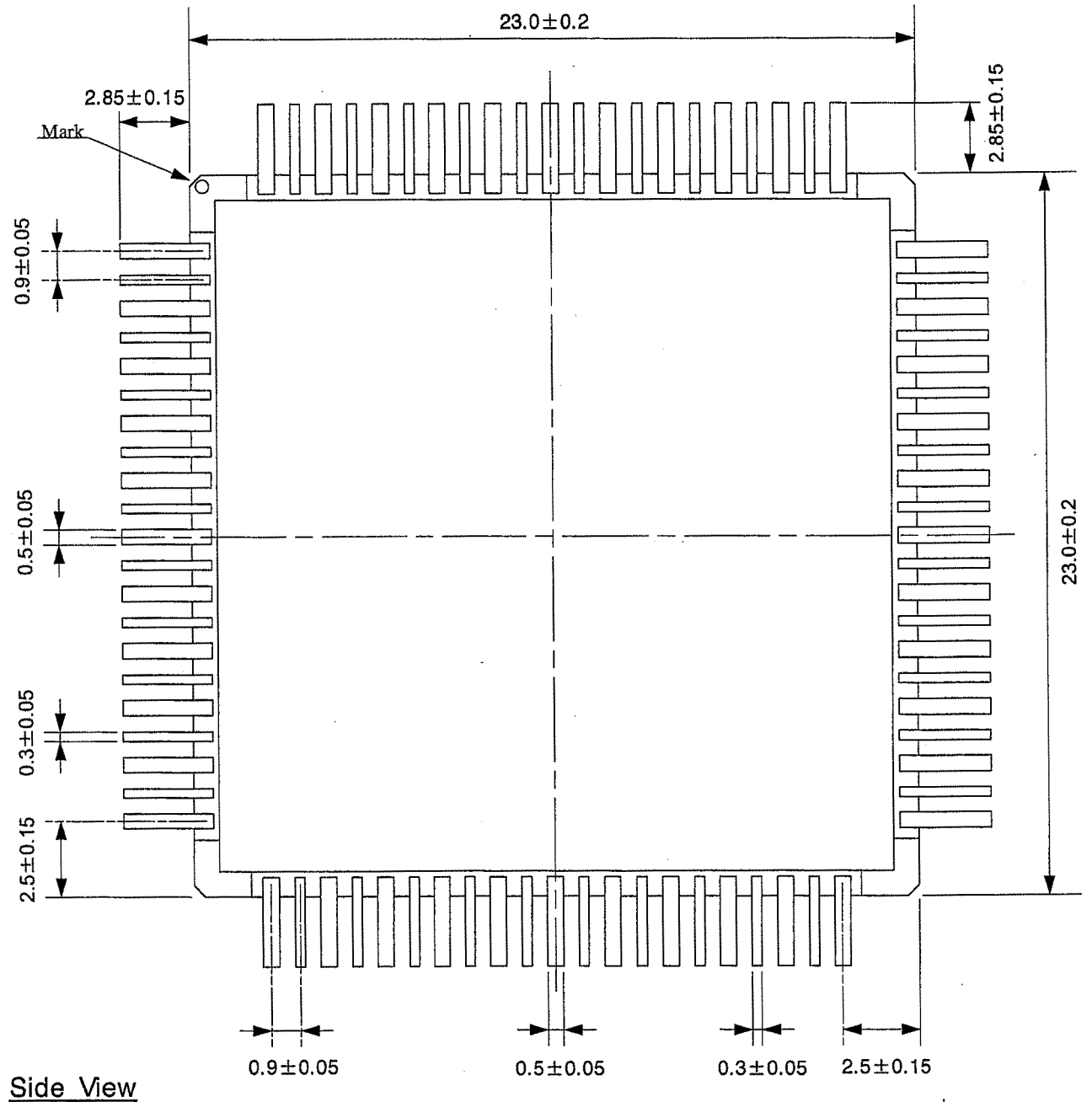




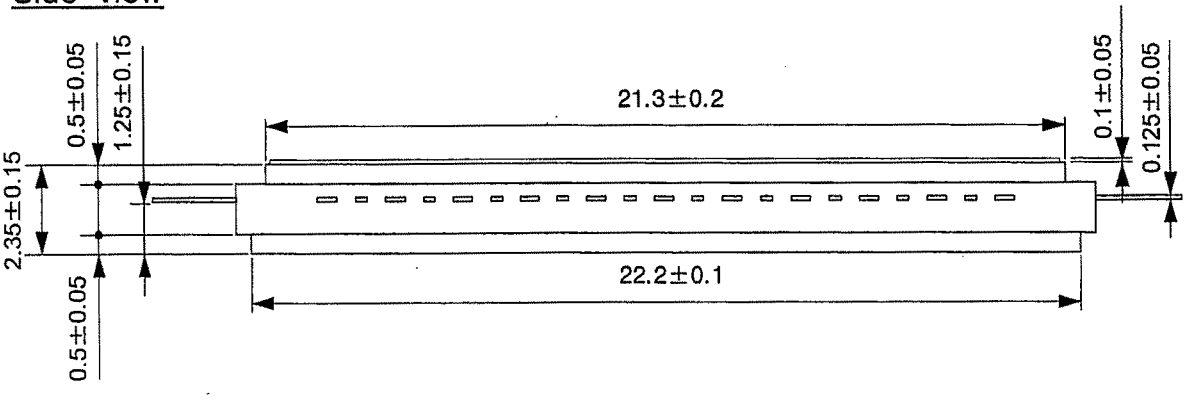
Caution : The package base should be connected to the ground.

TB 84 - PIN PACKAGE DIMENSION (mm)

Top View



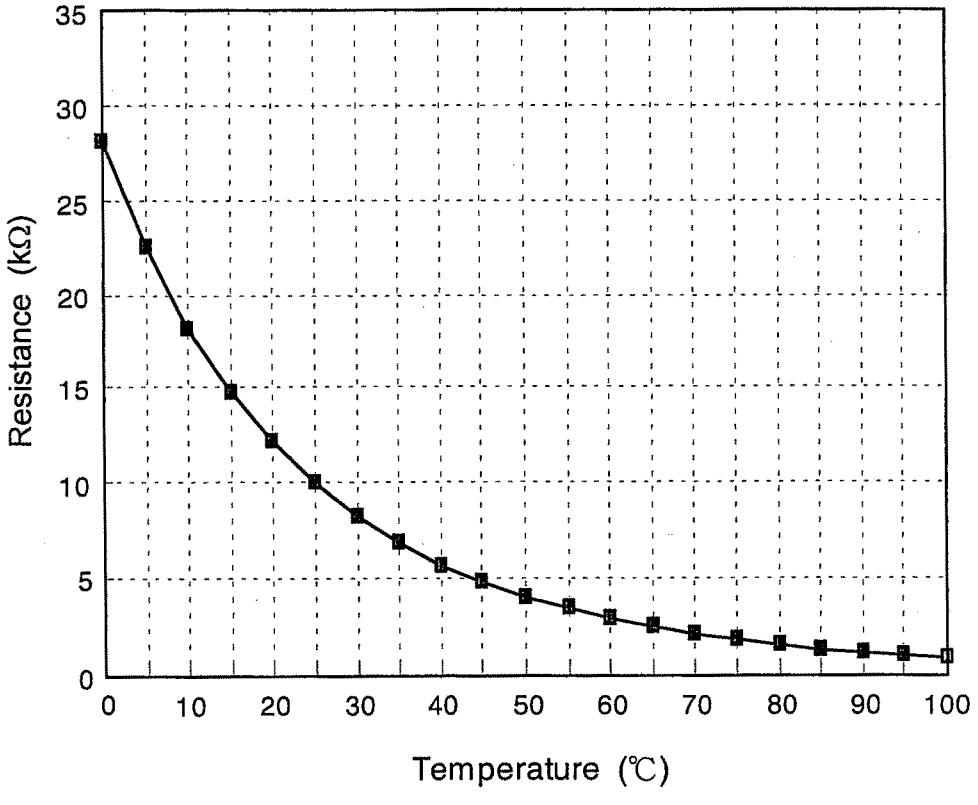
Side View



SAMPLE TEMPERATURE MONITOR

TCMON Resistance Value Versus Case Temperature

TEMPERATURE (℃)	RESISTANCE (kΩ) TYP.	TEMPERATURE (℃)	RESISTANCE (kΩ) TYP.
0	28.08	55	3.464
5	22.56	60	2.950
10	18.24	65	2.523
15	14.84	70	2.166
20	12.15	75	1.867
25	10.00	80	1.615
30	8.277	85	1.402
35	6.887	90	1.221
40	5.759	95	1.068
45	4.839	100	0.9362
50	4.085		



HANDLING INSTRUCTIONS

Since the NLG4306 is fabricated with GaAs MESFET's (Metal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro-static discharge.

(1) Power Supply Sequence

The following power supply sequence is recommended.

1) Set supply voltage Vss, V_{TT}, Vref01, Vref02, Vref1, Vref2 and GND to 0 V.
2) Apply Vref01, Vref02, Vref1, Vref2, Vss and V_{TT}.

RF signals are recommended to be applied while power supplying and biasing.

(2) Handling Precautions

1) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
2) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M-ohm resistors.
3) Ground all test equipment.
4) Ground all soldering iron tops.
5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

MEMO

Caution

1. In order to improve products and technology, specifications are subject to change without notice.

2. When using the products, be sure the latest information and specifications are used.

3. Circuit drawings etc. shall be provided for the purpose of information only on application examples not for actual installation of equipment. NTT Electronics Corp. shall not assume any liability for damage that may result from the use of these circuit drawings etc. NTT Electronics Corp. shall not assent to or guarantee any rights of execution for patent rights of the third parties and other rights that may be raised for use of these circuit drawings.

4. To make a design, the products shall be used within the assured ranges with respect to maximum ratings, voltage, and radiation. NTT Electronics Corp. shall not take any responsibility for damage caused by neglecting the assured values or improper usage.

5. Though NTT Electronics Corp. makes every effort to improve quality and reliability, there is a risk that failure or malfunction may occur in semiconductors. It is therefore necessary that the purchasers should take responsibility for making a design that allows the products to operate safely on equipment and systems without any direct threat to the human body and/or property, should such failures or malfunction occur.

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7. Some of the products are classified as strategic materials and the 'Foreign Exchange and Foreign Trade Control Act' applies. Export of the applicable products necessitates obtaining approval from the Japanese Government as required by law.

8. Some of the products use GaAs (gallium arsenide). GaAs powder and vapor are dangerous for humans. Do not break, cut, crush or chemically destroy the products. To dispose of the products, follow the relevant regulations and laws; do not mix with general industrial waste and domestic garbage.

9. Any questions should be directed to the Sales Department of NTT Electronics Corp.