NLG2132
TRANSIMPEDANCE AMPLIFIER(BARE DIE)

This NLG2132 is a GaAs MESFET IC Chip that performs signal amplification over the wide frequency range extending from DC to 7.7 GHz. This IC Chip is applicable to 10 Gb/s optical fiber communication systems.

The NLG2132 is fabricated using the 0.15 μm gate length A-SAINT(Advanced Self - Aligned Implantation for N+ layer Technology) process.

FEATURES

- Ultra-Wideband : DC ~7.7 GHz
- High Data Rates : 10 Gb/s NRZ
- High Transimpedance Gain : 52 dBΩ (Typ.)
- Low Noise : 12 pA/√Hz at 5 GHz (Typ.)

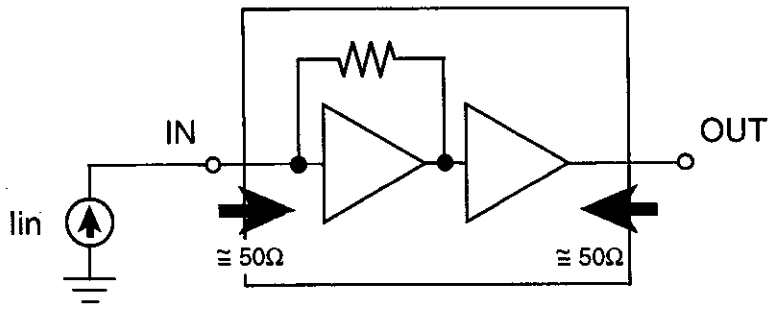
APPLICATIONS

- O/E Transfer module
- Equalizing amplification for optical communication
- Low noise amplification for radio communication

FUNCTION TABLE

IN	OUT
⎍	H
⎎	L

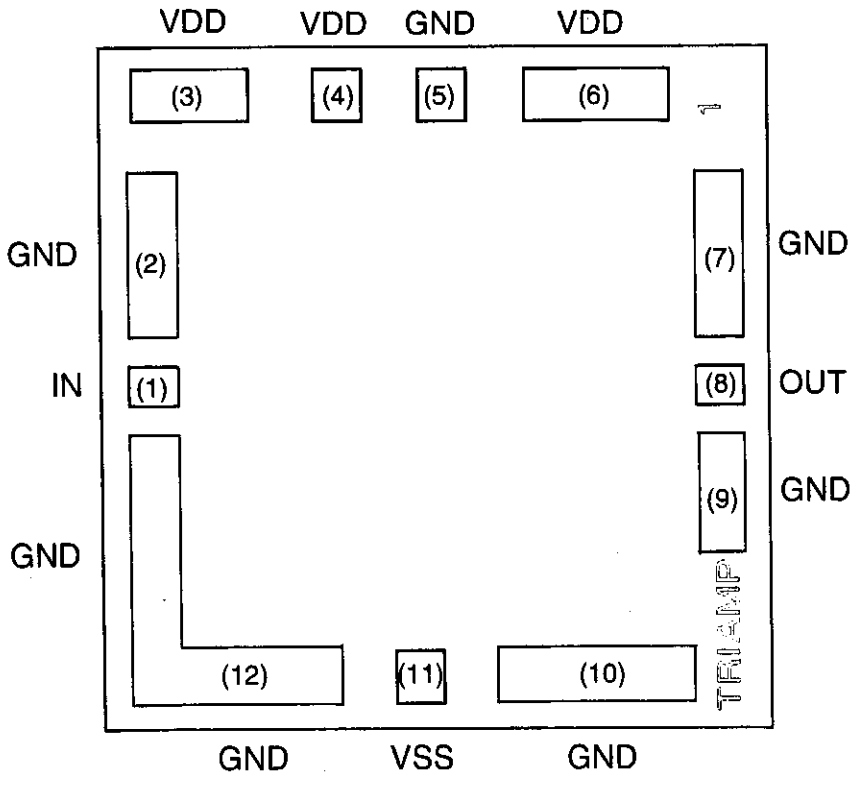
FUNCTION DIAGRAM



PAD ASSIGNMENT

PAD No.	SYMBOL	FUNCTION
1	IN	Input
2	GND	Ground (0.0 V)
3	VDD	Power Supply (+ 9.0 V)
4	VDD	Power Supply (+ 9.0 V)
5	GND	Ground (0.0 V)
6	VDD	Power Supply (+ 9.0 V)
7	GND	Ground (0.0 V)
8	OUT	Output
9	GND	Ground (0.0 V)
10	GND	Ground (0.0 V)
11	VSS	Power Supply (-3.5 V)
12	GND	Ground (0.0 V)

PAD LOCATIONS



ABSOLUTE MAXIMUM RATINGS

(Ta= 25 °C)

SYMBOL	PARAMETER	RATING	UNITS
VDD	Power Supply	11	V
VSS	Power Supply	-5	V
IIN	Current Applied to Input	6.5	mApp
Tstor	Storage Temperature	−60 ~ +150	°C
TCB	Chip Bottom temperature under Bias	−60 ~ +125	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VDD	Power Supply	8.55	9.0	9.45	V
VSS	Power Supply	-3.75	-3.5	-3.4	V
IIN	Current Applied to Input			2	mApp

ELECTRICAL CHARACTERISTICS

(V_{DD}= 8.55 ~ 9.45 V, V_{SS}= -3.75 ~ -3.40 V, Input and Output terminal : AC coupling, Zo=50 Ω)

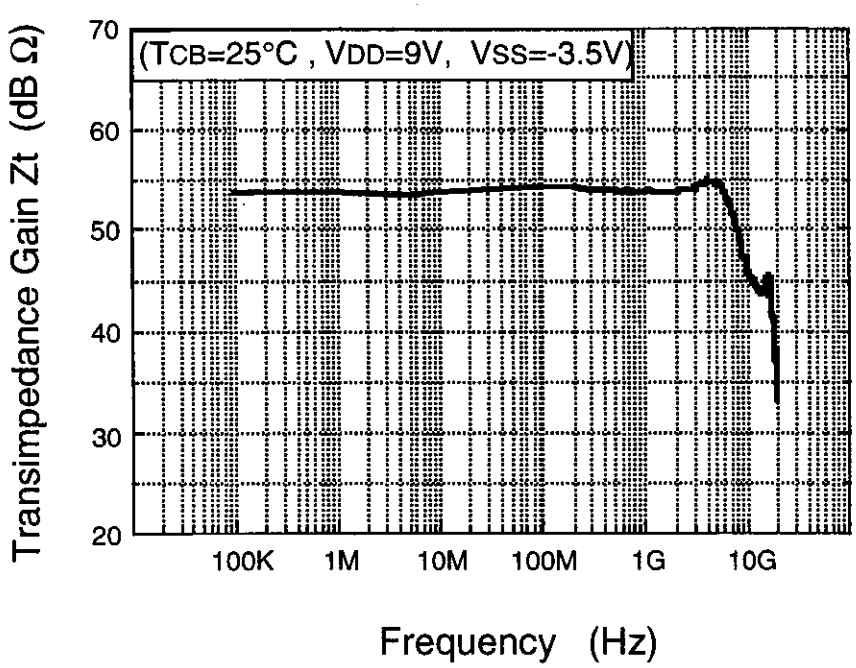
SYMBOL	PARAMETER	CONDITION	TCB=0°C			TCB=25°C			TCB=90°C			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
IDD	Supply Current			77	120		78	120		79	120	mA
ISS	Supply Current			25	38		25	38		25	38	mA
f-3dB	3dB Bandwidth *1	C=0.2pF *2 L=0.5nH *3	7.7G	7.9G		7.5G	7.7G		6.8G	7.0G		Hz
Zt	Transimpedance Gain	f=200MHz C=0.2pF *2 L=0.5nH *3	50	52	54	50	52	54	50	51	53	dB Ω
ΔZtp	Frequency Response *4 Gain Peak	f=100MHz~10GHz C=0.2pF *2 L=0.5nH *3		1.3	2.3		1.0	2.0		0.6	1.6	dB
|ΔZtd|	Frequency Response *4 Gain Dip	f=100MHz~5GHz C=0.2pF *2 L=0.5nH *3		0.6	1.2		0.6	1.2		0.8	1.4	dB
|S22|	Output Return Loss *5	f=100MHz~10GHz	5.0	6.5		5.0	7.5		5.0	8.0		dB
In	Input Current Noise Spectral Density	f=5GHz C=0.2pF *2		12	18		12	18		14	20	pA/√Hz
Vin	Input DC Offset Voltage		-0.39	0.01	0.41	-0.40	0.00	0.40	-0.41	-0.01	0.39	V

*1 The frequency at which gain has been reduced by 3dB from the gain Zt
*2 Photodiode capacitance
*3 The inductance of bonding wire between photodiode and transimpedance amplifier
*4 Referenced from 100MHz
*5 Minimum Value at frequency range of 100MHz ~ 10GHz

1. SMALL SIGNAL INPUT CHARACTERISTICS

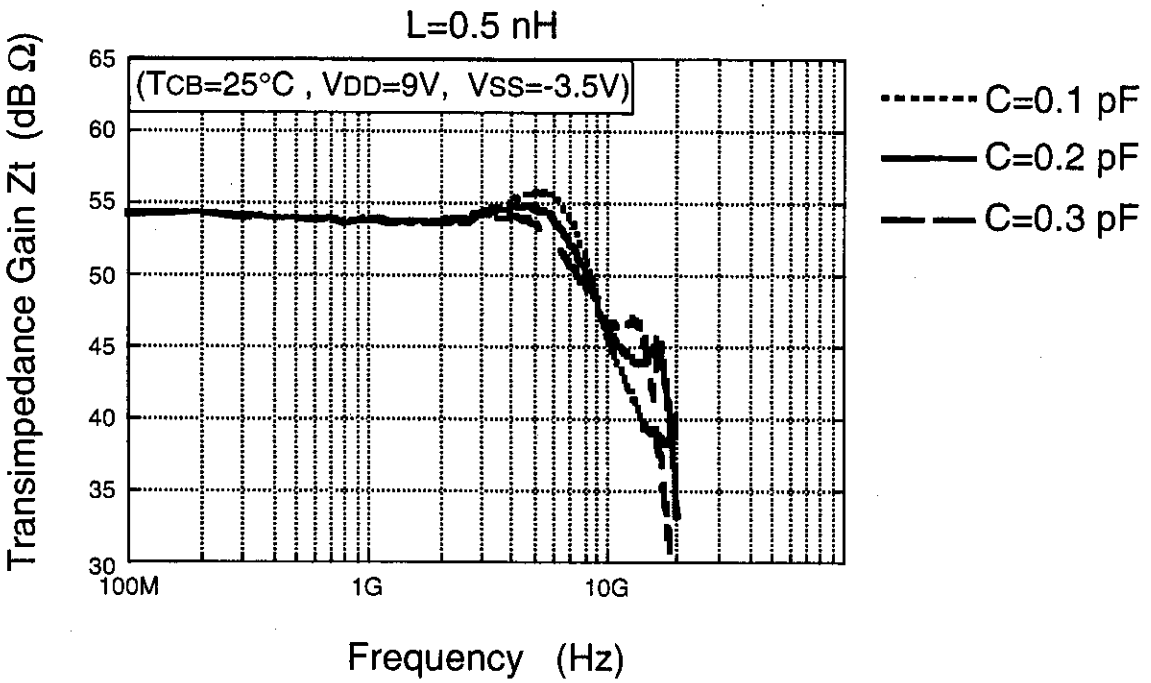
(1-1) SAMPLE TRANSIMPEDANCE GAIN

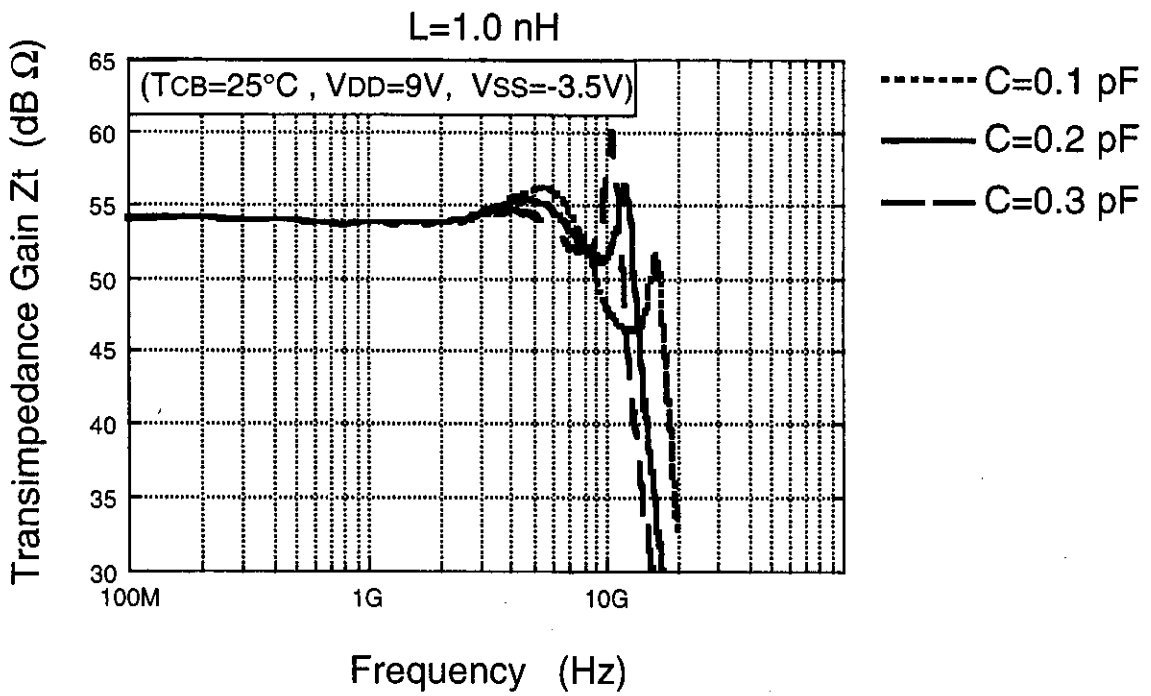
Photodiode capacitance : C=0.2 pF
The inductance of bonding wire between photodiode and transimpedance amplifier : L=0.5 nH



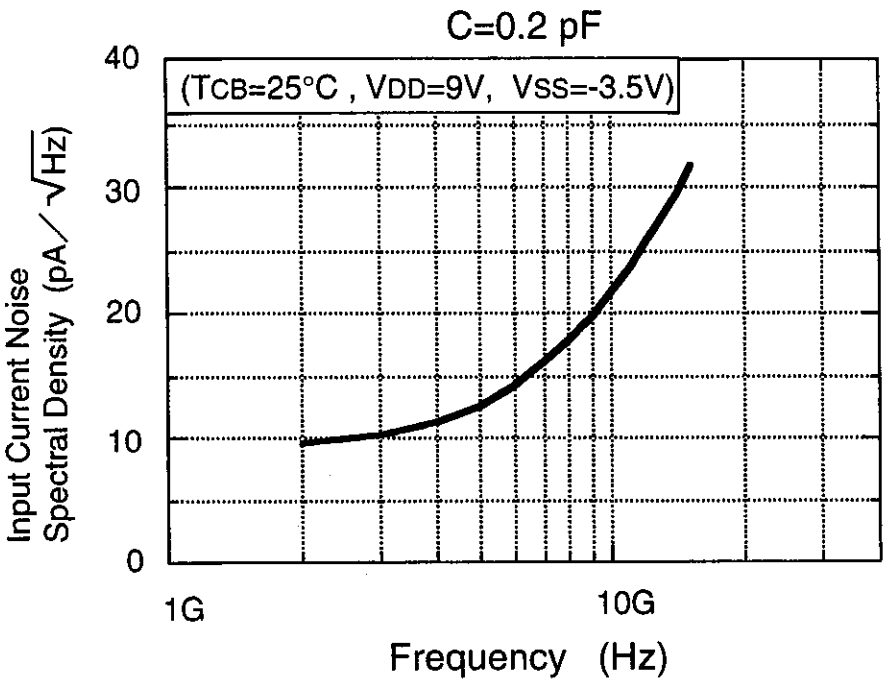
(1-2) SAMPLE TRANSIMPEDANCE GAIN

(Frequency dependence for various photodiode capacitance)

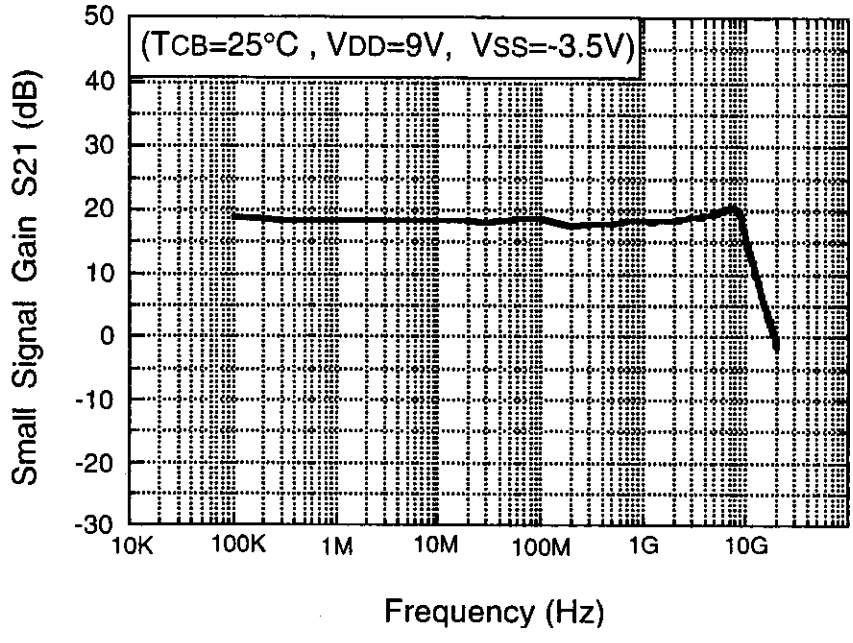


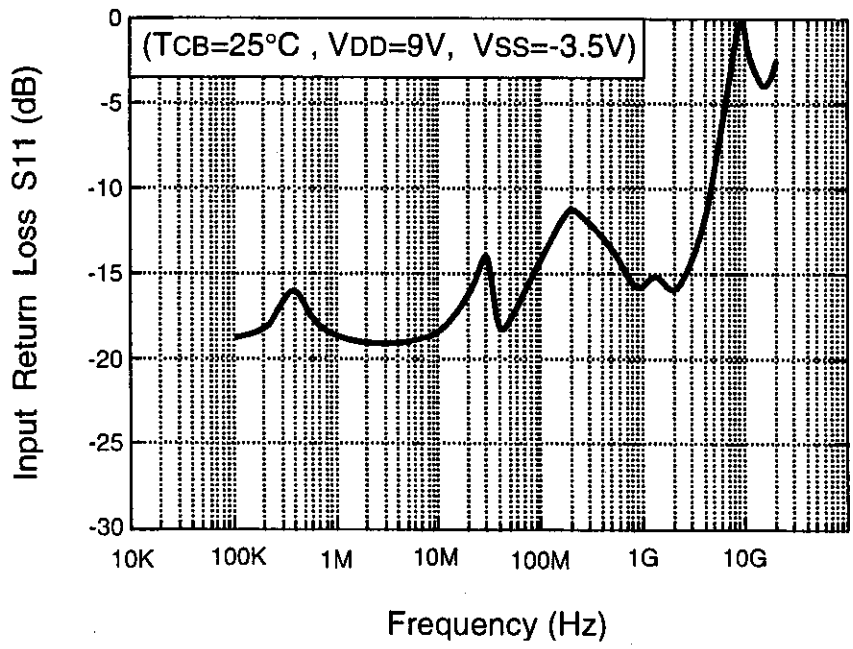


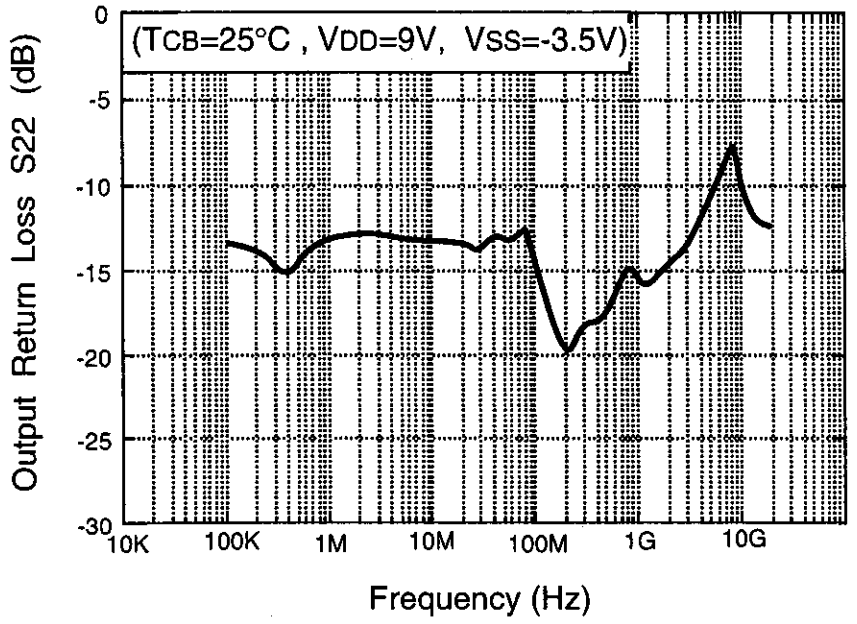
(1-3) SAMPLE INPUT CURRENT NOISE SPECTRAL DENSITY

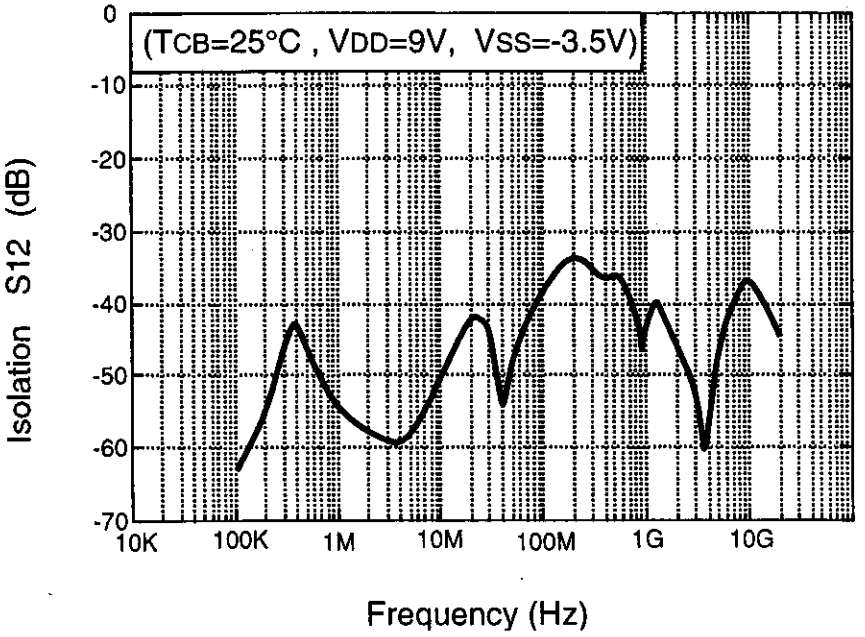


(1-4) SAMPLE S-PARAMETERS

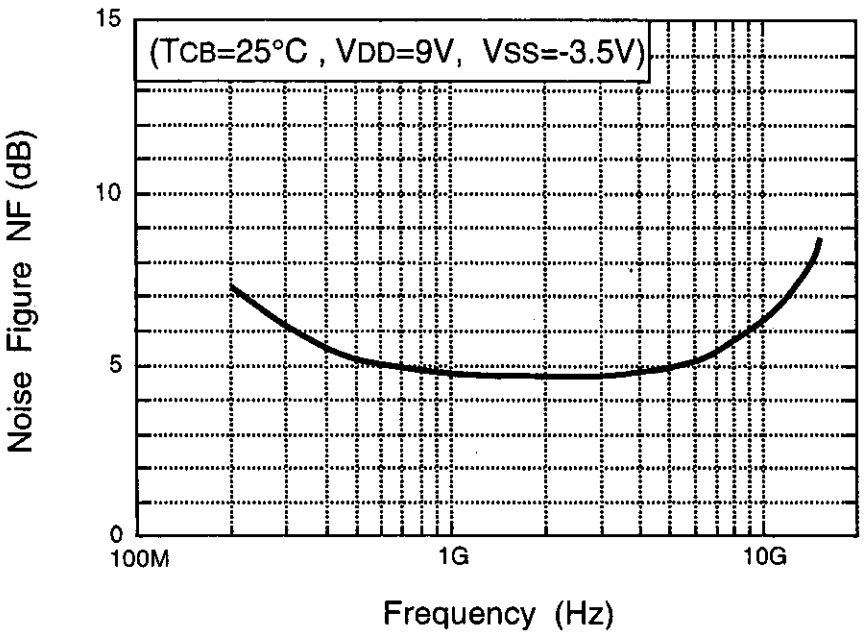




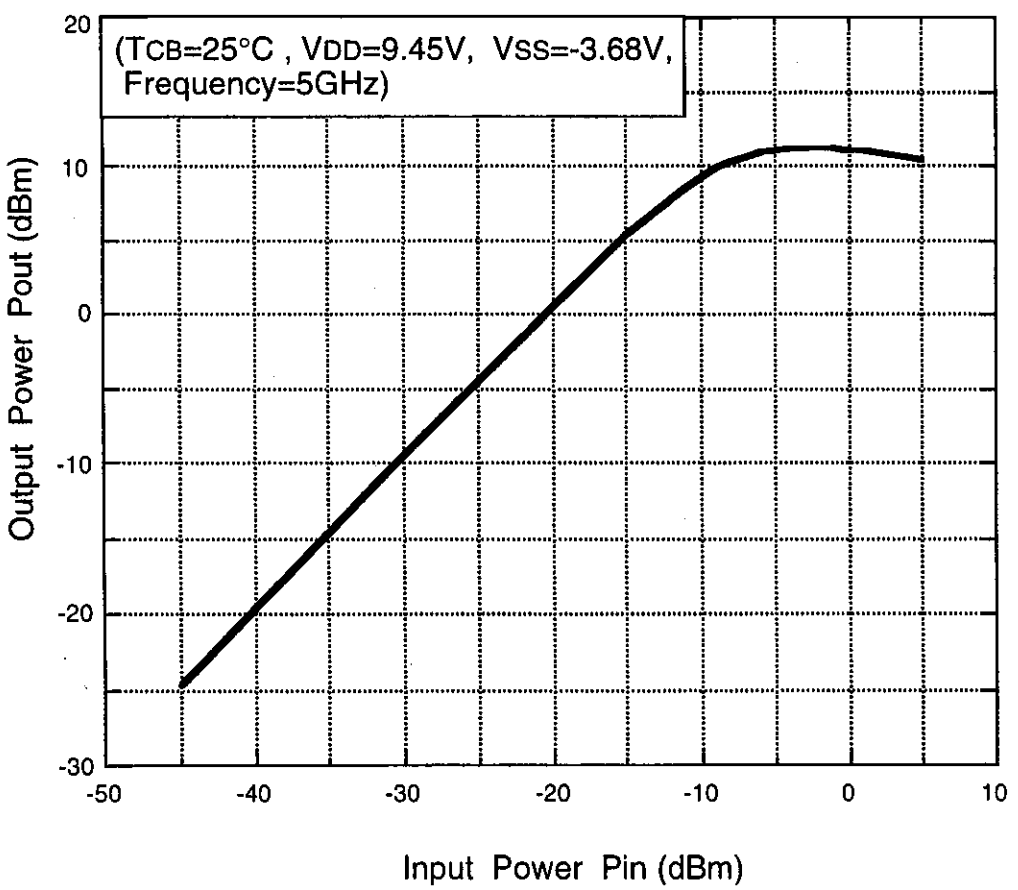

(TCB=25°C , VDD=9V, VSS=-3.5V)
Output Return Loss S22 (dB)
0
-5
-10
-15
-20
-25
-30
10K
100K
1M
10M
100M
1G
10G
Frequency (Hz)


(TCB=25°C , VDD=9V, VSS=-3.5V)
Isolation S12 (dB)
0
-10
-20
-30
-40
-50
-60
-70
10K
100K
1M
10M
100M
1G
10G
Frequency (Hz)

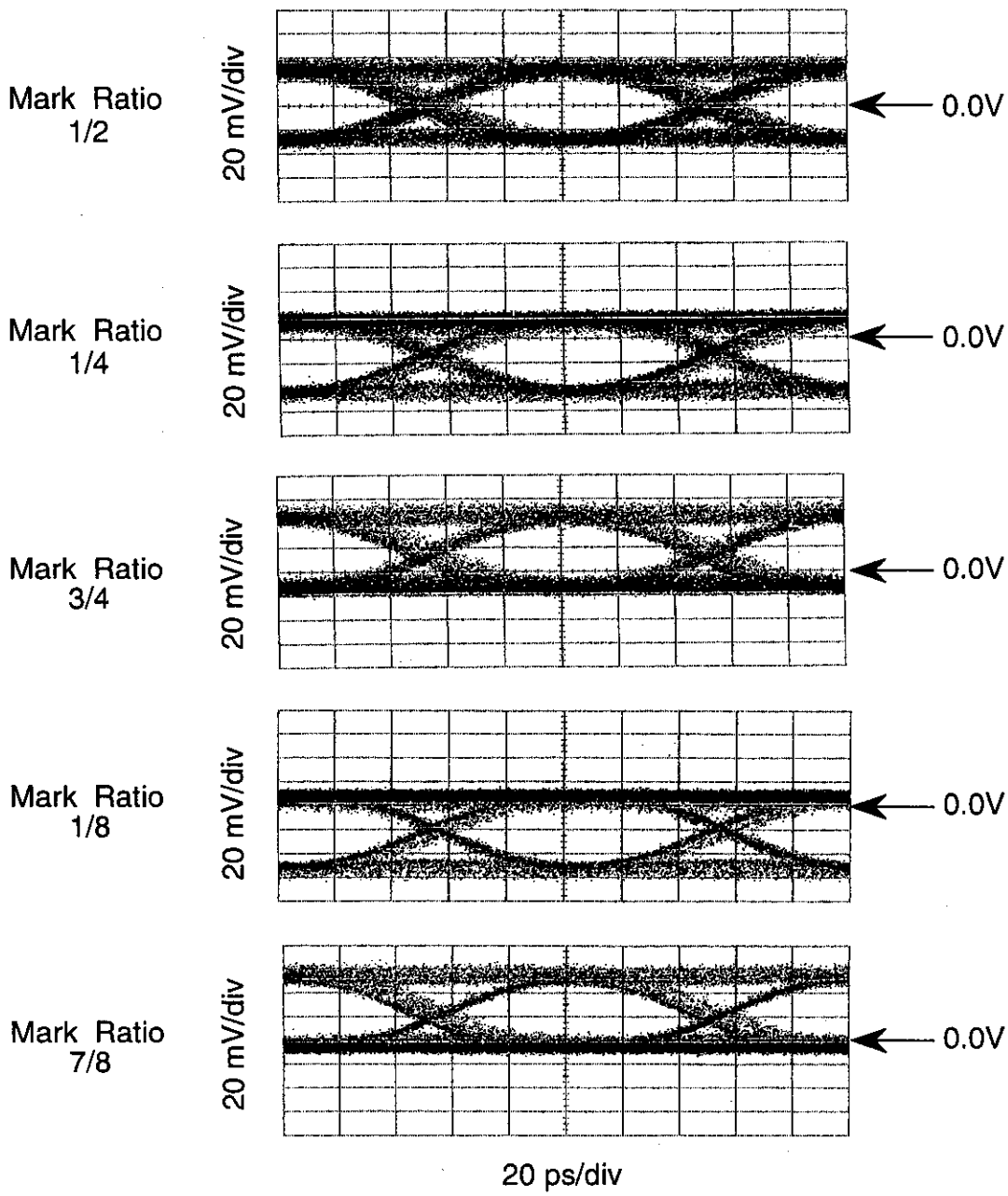
(1-5) SAMPLE NOISE FIGURE



(1-6) SAMPLE INPUT/OUTPUT CHARACTERISTICS



2. OUTPUT WAVEFORMS : PSEUDO-RANDOM INPUT SIGNAL RESPONSE

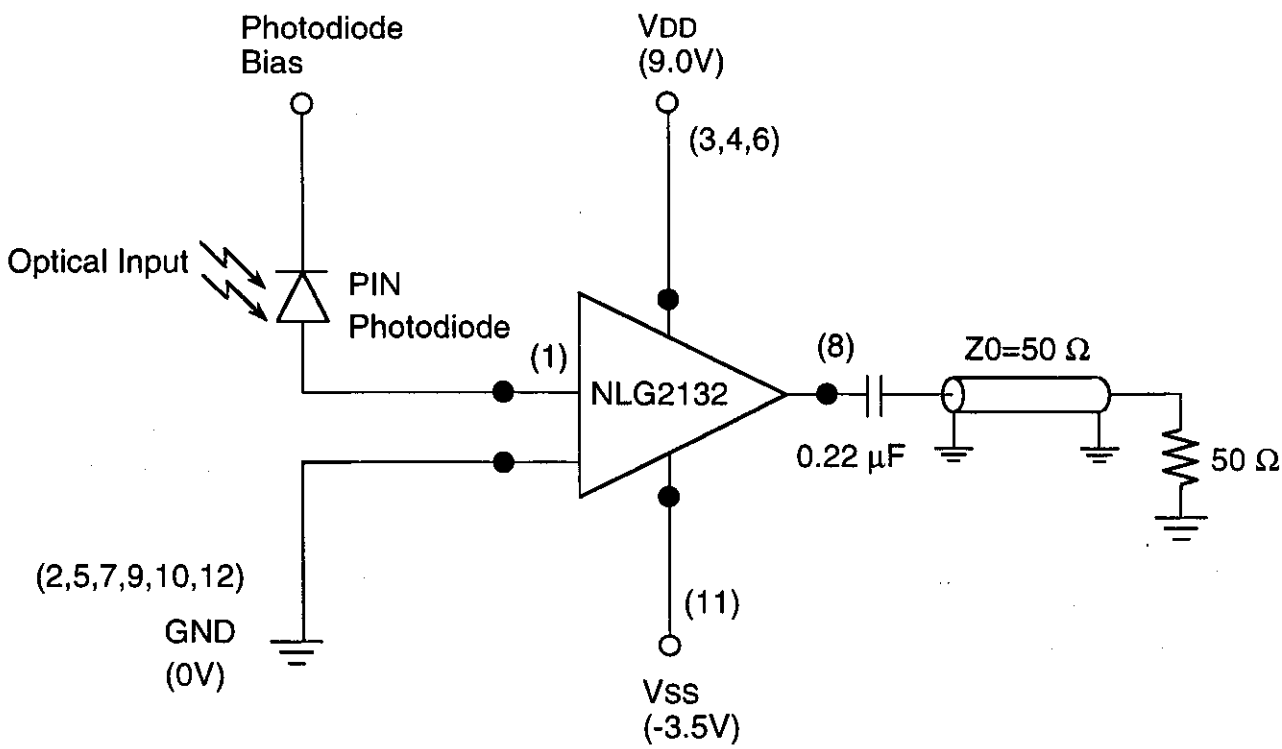


Measurement Conditions

V_{DD}=9.0V, V_{SS}=-3.5V. DC blocking capacitance C=0.22 µF.
Input data a 10Gb/s pseudo-random pattern having a word length of 2^{23}-1 bits,where input signal amplitude is 0.009Vpp.
Error-free operation (an error rate less than 1E-13) confirmed.

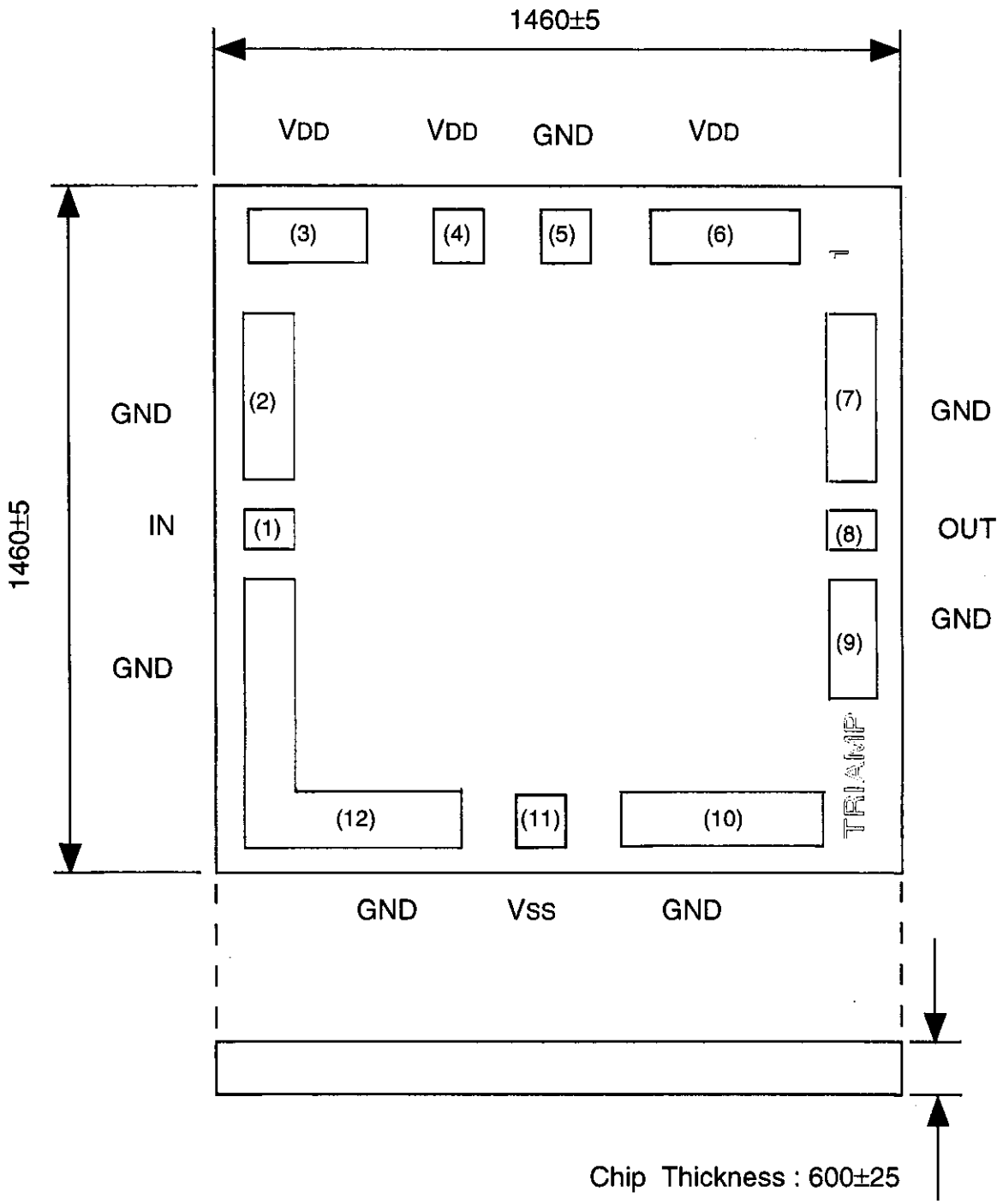
SAMPLE IMPLEMENTATION

Notes : Numbers represent pad numbers



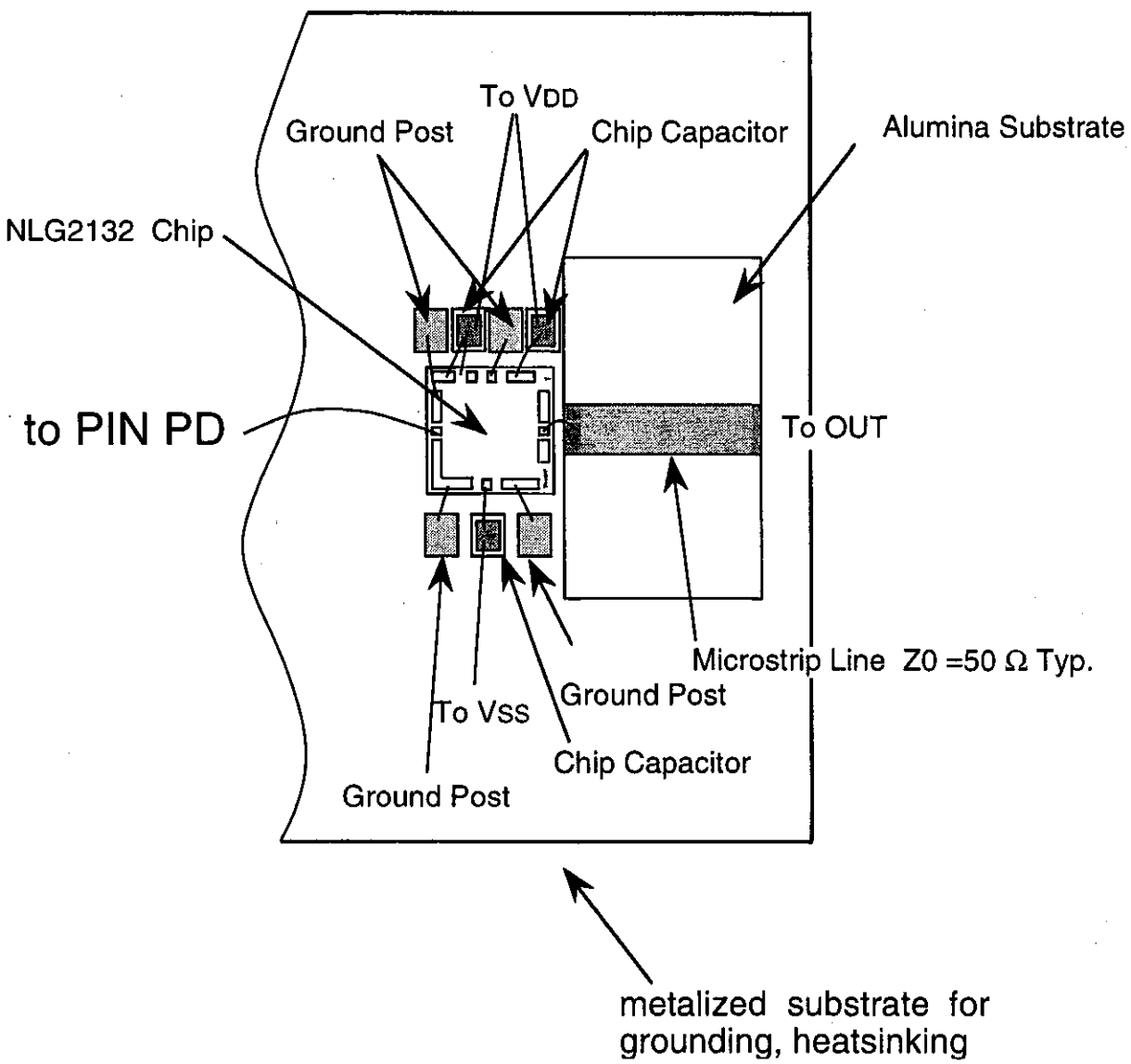
CHIP STRUCTURE

Unit : µm



MOUNTING EXAMPLE

Top View



OPERATING AND HANDLING INSTRUCTIONS

Since the NLG2132 is fabricated with GaAs MESFET's (MEtal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro-statics discharge.

(1) Handling Precautions

1) IC chips are very fragile and handling should be minimized.
2) Use a conductive working desk connected to the ground (or , a conductive table top connected to the ground).
3) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M-ohm resistor.
4) Ground all test equipment.

(2) Storing Precautions

IC chips should be stored in dry-nitrogen , vacuum , or moisture-free sealed environment.

(3) Power supply sequence

The following power supply sequence is recommended.

1) Set supply voltages V_{DD},V_{SS} and GND to 0 V.
2) Apply V_{SS}.
3) Apply V_{DD}.

RF signal is recommended to be applied while power supplying.

Caution

1. In order to improve products and technology, specifications are subject to change without notice.

2. When using the products, be sure the latest information and specifications are used.

3. Circuit drawings etc. shall be provided for the purpose of information only on application examples not for actual installation of equipment. NTT Electronics Corp. shall not assume any liability for damage that may result from the use of these circuit drawings etc. NTT Electronics Corp. shall not assent to or guarantee any rights of execution for patent rights of the third parties and other rights that may be raised for use of these circuit drawings.

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8. Some of the products use GaAs (gallium arsenide). GaAs powder and vapor are dangerous for humans. Do not break, cut, crush or chemically destroy the products. To dispose of the products, follow the relevant regulations and laws; do not mix with general industrial waste and domestic garbage.

9. Any questions should be directed to the Sales Department of NTT Electronics Corp.