NEL

NS GD E129
4 Feb. 2002
PRELIMINARY

NLG4143
CLOCK RECOVERY CIRCUIT

The NLG4143 is an ultra-fast Clock Recovery Circuit.
This IC regenerates a clock signal (9.95328 GHz) from an NRZ data input signal (9.95328 Gb/s) using an external band-pass filter .
Designed with LSCFL (Low-power Source Coupled FET Logic) , it uses SCFL I/O levels (V_H : 0.0 V, V_L : - 0.9 V) .
Owing to built-in 50-ohm termination resistor between data input pin and ground (GND) , external termination resistor is unnecessary for impedance matching.
The NLG4143 is fabricated using the 0.15-µm gate length A-SAINT (**A**dvanced **S**elf-**A**ligned **I**mplantation for $\mathbf{N}^+$ layer **T**echnology) process .

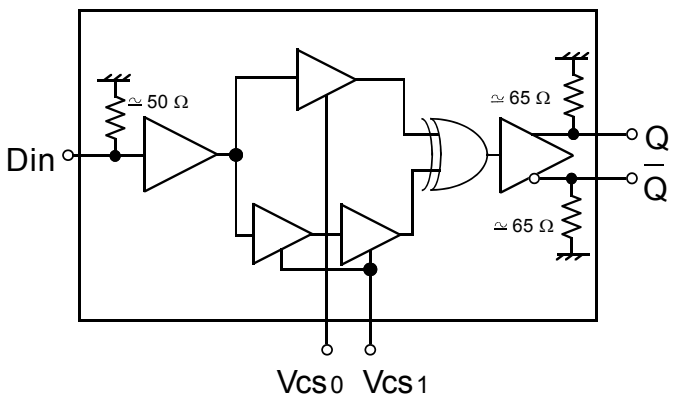
FEATURES

Ultra-high speed :	Input data bit rate	fd : 9.95328 Gb/s
	output rise time	tr = 20 ps (20-80 %) [TYP.]
	output fall time	tf = 20 ps (20-80 %) [TYP.]
High Reliability :	hermetically-sealed package	

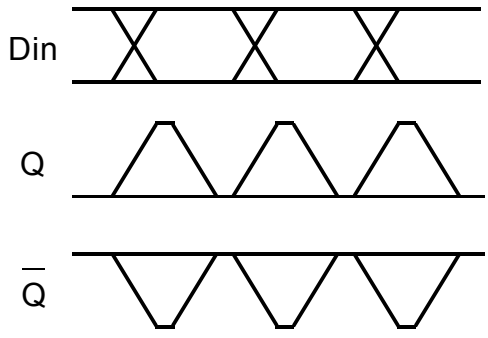
APPLICATIONS

- Clock recovery
- Frequency doubler

FUNCTIONAL DIAGRAM



TIMING CHART



PIN CONNECTION TABLE

PIN No.	NAME	FUNCTION	PIN No.	NAME	FUNCTION
1	NC	No Internal Connection	15	NC	No Internal Connection
2	GND	Ground (0.0 V)	16	GND	Ground (0.0 V)
3	Din	Data Input	17	$\overline{Q}$	Signal Output (Comp.)
4	GND	Ground (0.0 V)	18	GND	Ground (0.0 V)
5	NC	No Internal Connection	19	Q	Signal Output (True)
6	GND	Ground (0.0 V)	20	GND	Ground (0.0 V)
7	NC	No Internal Connection	21	NC	No Internal Connection
8	NC	No Internal Connection	22	Vcs0	Duty Adjust. (2)
9	GND	Ground (0.0 V)	23	GND	Ground (0.0 V)
10	Vss	Power Supply (- 3.5 V)	24	Vss	Power Supply (- 3.5 V)
11	GND	Ground (0.0 V)	25	GND	Ground (0.0 V)
12	Vss	Power Supply (- 3.5 V)	26	Vss	Power Supply (- 3.5 V)
13	GND	Ground (0.0 V)	27	GND	Ground (0.0 V)
14	Vcs1	Duty Adjust. (3)	28	Vref	Data Input Ref. (1)

Notes

(1) Vref : Internally generated reference voltage that determines the data input threshold level. By applying - 0.75 V to - 0.2 V externally to this pin, an arbitrary data input threshold voltage can be established.

(2) Vcs0 : Duty decrease adjustment pin. A duty of data output can be decreased by applying from Vss + 0.30 V to Vss + 0.60 V at Vcs0 while applying Vss + 0.60 V at Vcs1.
See sample duty adjust characteristics(page 7,8) .

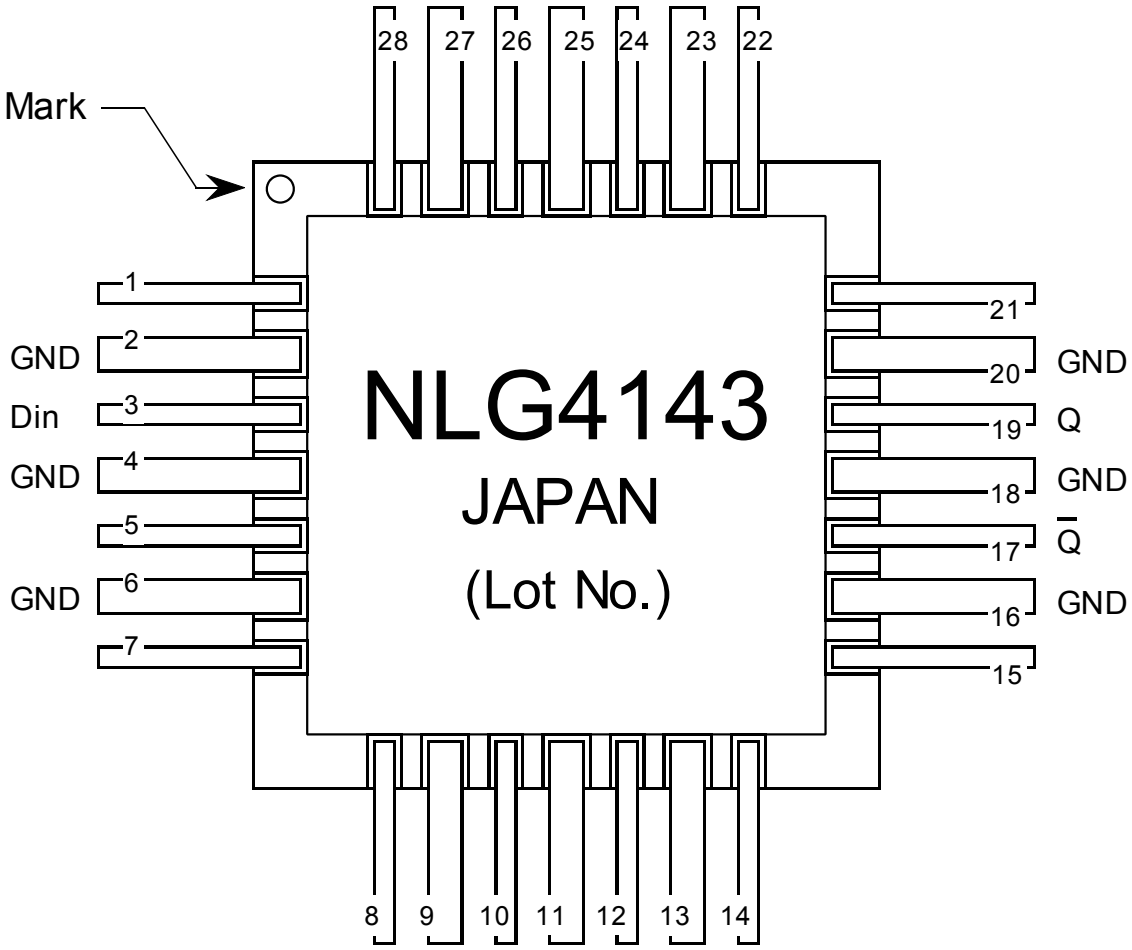
(3) Vcs1 : Duty adjustment pin. Vcs1 is applying Vss + 0.60 V .
See sample implementation(page 9) .

ATTENTION

Please pay attention not to touch the Vcs0 and Vcs1 pins to the GND or the other pins while applying the Vss voltage, otherwise the IC would be damaged.

(4) Terminate unused output pins in 50-ohms.

CONNECTION DIAGRAM (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
Vss	Power Supply Voltage	+ 0.5 V ~ - 4.0 V
Vin	Applied Voltage at Data Input (Din)	+ 0.3 V ~ - 1.6 V
Vout	Applied Voltage at Data Outputs (Q, $\overline{Q}$)	+ 0.2 V ~ - 1.75 V
Vref	Applied Voltage at Vref pin	+ 0.3 V ~ - 1.6 V
Vcs0, Vcs1	Applied Voltage at Vcs0 and Vcs1 pins under Bias	Vss + 0.7 V ~ Vss
Tstor	Storage Temperature	- 60 °C ~ + 150 °C
Tc (1)	Case Temperature under Bias	- 60 °C ~ + 125 °C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Vss	Power Supply Voltage	- 3.75	- 3.5	- 3.4	V
Vref	Data Input Reference Voltage	Adjust in the range from - 0.75 V to - 0.20 V			V
Vcs0	Applied Voltage to decrease duty at Vcs0 pins	Adjust in the range from Vcs0 = Vss + 0.30 V to Vss + 0.60 V			V
Vcs1	Applied Voltage to duty at Vcs1 pins	Apply voltage at Vcs1 = Vss + 0.60 V			V
Vin	Data Input Interface (Din)	DC Coupling (See DC Characteristics)			—
Vout	Data Output Interface (Q, $\overline{Q}$)	DC Coupling (See DC Characteristics) or AC Coupling (See AC Characteristics), Terminate to GND through 50Ω			—
MR	Input Data Mark Ratio	1/2			—

DC CHARACTERISTICS

(Vss = - 3.75 V ~ - 3.40 V, GND = 0.0 V, Vcs0, Vcs1 : OPEN, Tc = 0 ~ 85 °C (1))

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
VOH	Output Voltage, High (Q, $\overline{Q}$)	- 0.1	0.0		V
VOL	Output Voltage, Low (Q, $\overline{Q}$)		- 0.9	- 0.85	V
VIH	Input Voltage, High (Din)	- 0.2	0.0		V
VIL	Input Voltage, Low (Din)		- 0.9	- 0.75	V
Iss	Power Supply Current		500	800	mA (2)

Notes

(1) Tc : temperature at package base.

(2) Includes load current. Excludes current through input termination resistors, all of which have 50-ohm resistors.

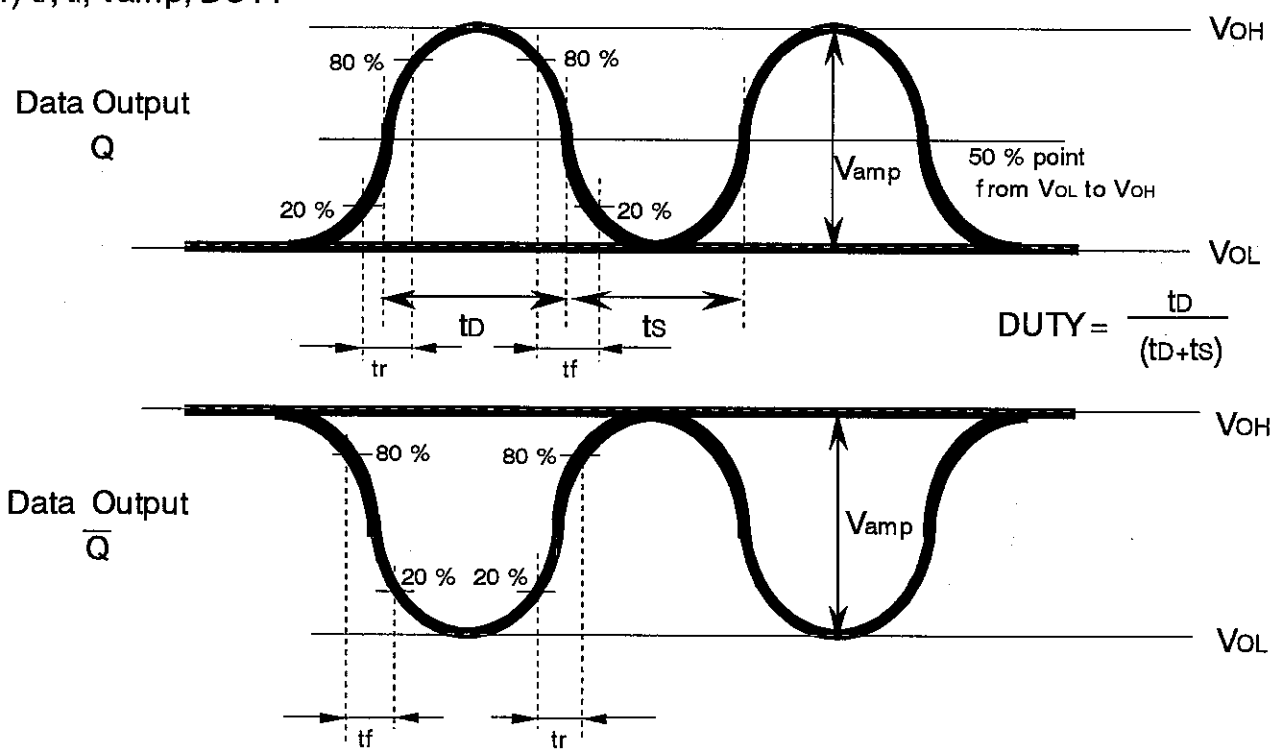
AC CHARACTERISTICS

(Vss = - 3.75 V ~ - 3.40 V, GND = 0.0 V, Tc = 0 ~ 85 °C, Vref : Adjust in the range from - 0.75 V to - 0.2 V, V_{CS0}, V_{CS1} : Adjust in the range from open circuit voltage to Vss + 0.3 V, PN = 31, MR = 1/2)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
fd	Input Data Bit Rate		9.95328		Gb/s	
V_{OH}	Output Voltage, High (Q)	- 0.25	- 0.15		V	(1), (2)
	Output Voltage, High ($\overline{Q}$)	- 0.15	- 0.05		V	(1), (2)
V_{OL}	Output Voltage, Low (Q)		- 1.05	- 0.75	V	(1), (2)
	Output Voltage, Low ($\overline{Q}$)		-0.95	- 0.75	V	(1), (2)
Vamp	Output Voltage Amplitude (Q, $\overline{Q}$)	0.7	0.8		V_{p-p}	(1), (3)
tr	Output Rise Time (Q, $\overline{Q}$, 20-80%)		20	35	ps	(1), (2)
tf	Output Fall Time (Q, $\overline{Q}$, 20-80%)		20	30	ps	(1), (2)
DUTY	Duty Cycle (Q)	45	55	70	%	(1), (2)
	Duty Cycle ($\overline{Q}$)	40	55	65	%	(1), (2)

Notes

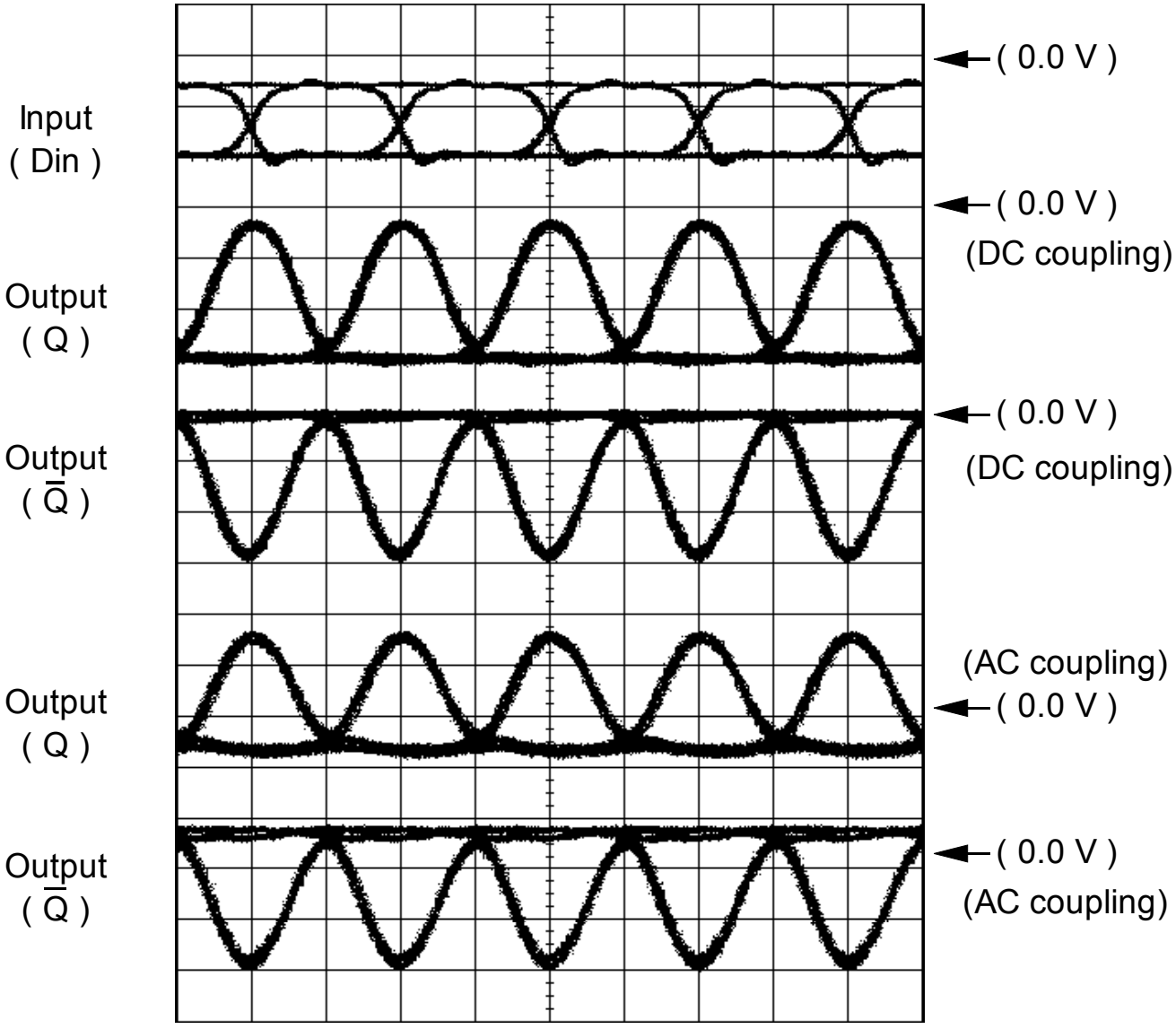
(1) tr, tf, Vamp, DUTY



(2) DC coupling 50 Ω to GND.

(3) AC coupling 50 Ω to GND.
Measured by using Picosecond Pulse Labs. DC block (Model 5501A)

SAMPLE INPUT AND OUTPUT WAVEFORMS (9.95 Gb/s)

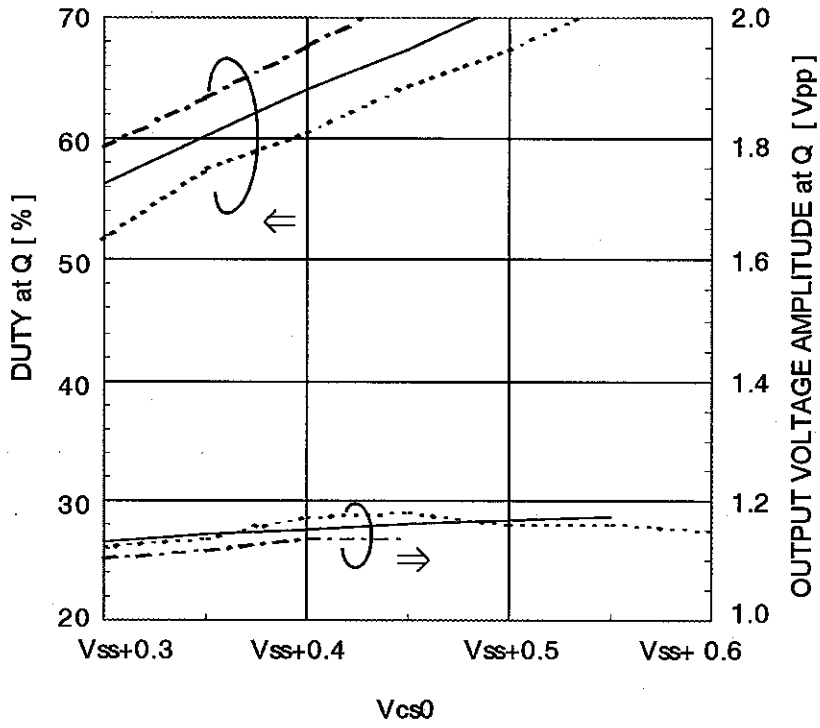


Measurement Conditions

Ta = 25 ℃
Vss = - 3.5 V
Vref = - 0.51 V
Vcs_0 = Vss + 0.30 V
Vcs_1 = Vss + 0.60 V
Signal outputs connected to the 50-ohm impedance pins of a sampling oscilloscope .
Results given here were obtained using the NEL test fixture.

SAMPLE DUTY ADJUST CHARACTERISTICS (OUTPUT Q)

Vss = - 3.5 V



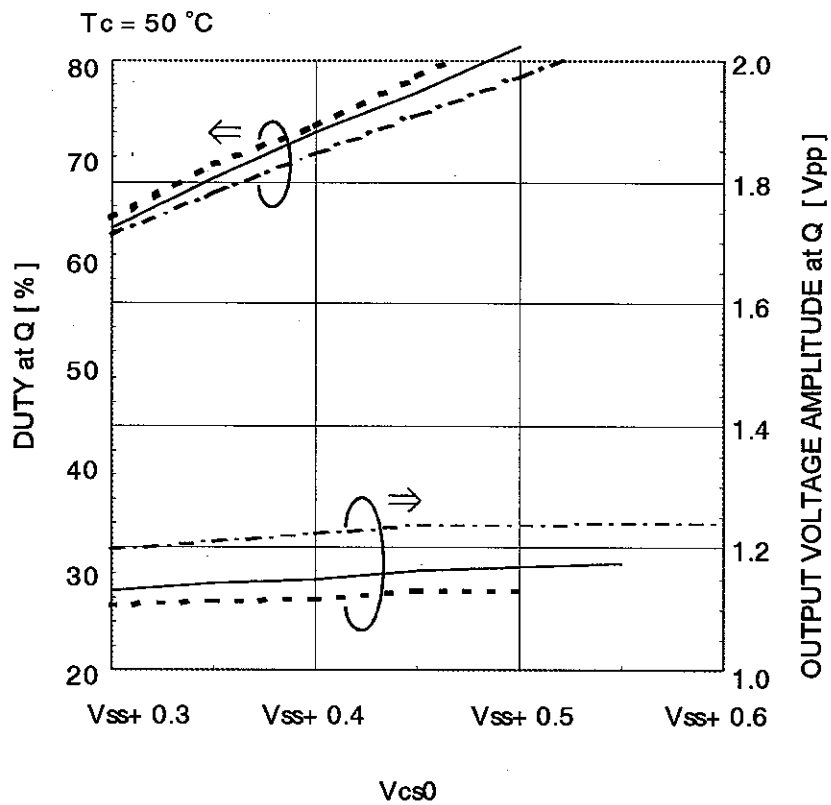
- - - - - - : Tc = 0 °C
——— : Tc = 50 °C
— - — - - : Tc = 75 °C

Measurement Conditions

Vref = - 0.51 V
Vcs1 = Vss + 0.6 V
Din : PN = 31, MR 1 / 2
9.95 Gb / s
VIH = - 0.2 V VIL = - 0.75 V

Results given here were obtained using the NEL test fixture.

Tc = 50 °C



- - - - - - : Vss = - 3.4 V
——— : Vss = - 3.5 V
— - — - - : Vss = - 3.75 V

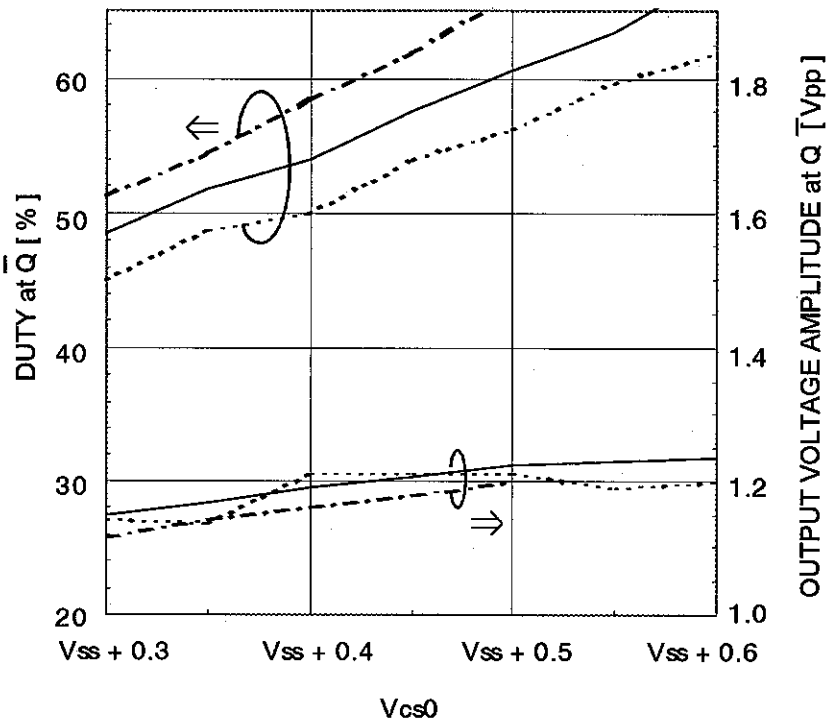
Measurement Conditions

Vref = - 0.51 V
Vcs1 = Vss + 0.6 V
Din : PN = 31, MR 1 / 2
9.95 Gb / s
VIH = - 0.2 V VIL = - 0.75 V

Results given here were obtained using the NEL test fixture.

SAMPLE DUTY ADJUST CHARACTERISTICS (OUTPUT $\overline{Q}$)

Vss = - 3.5 V



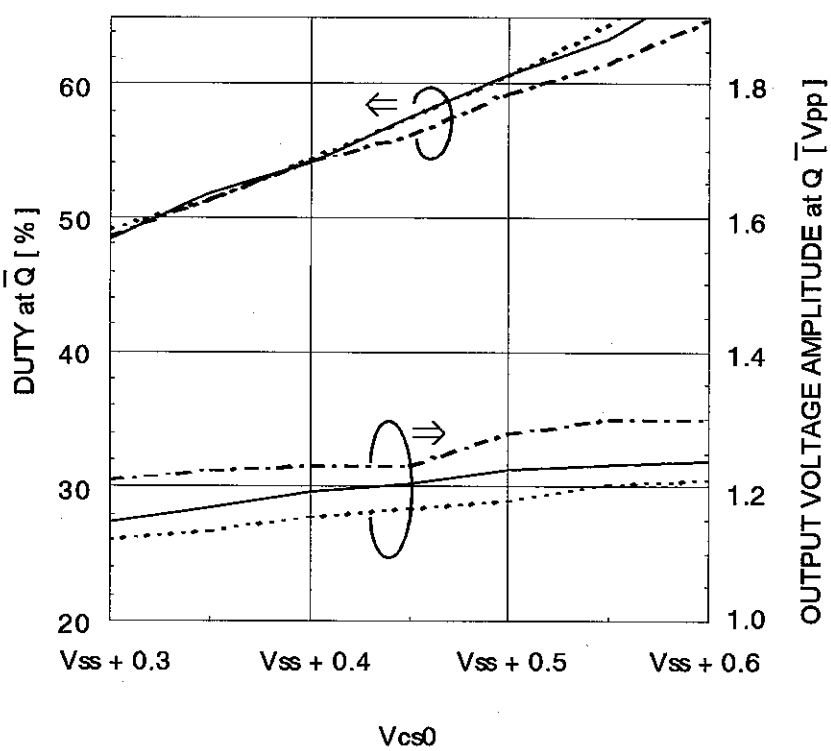
- - - - - - : Tc = 0 °C
——— : Tc = 50 °C
— - — - - : Tc = 75 °C

Measurement Conditions

Vref = - 0.51 V
Vcs1 = Vss + 0.6 V
Din : PN = 31, MR 1 / 2
9.95 Gb / s
VIH = - 0.2 V VIL = - 0.75 V

Results given here were obtained using the NEL test fixture.

Tc = 50 °C



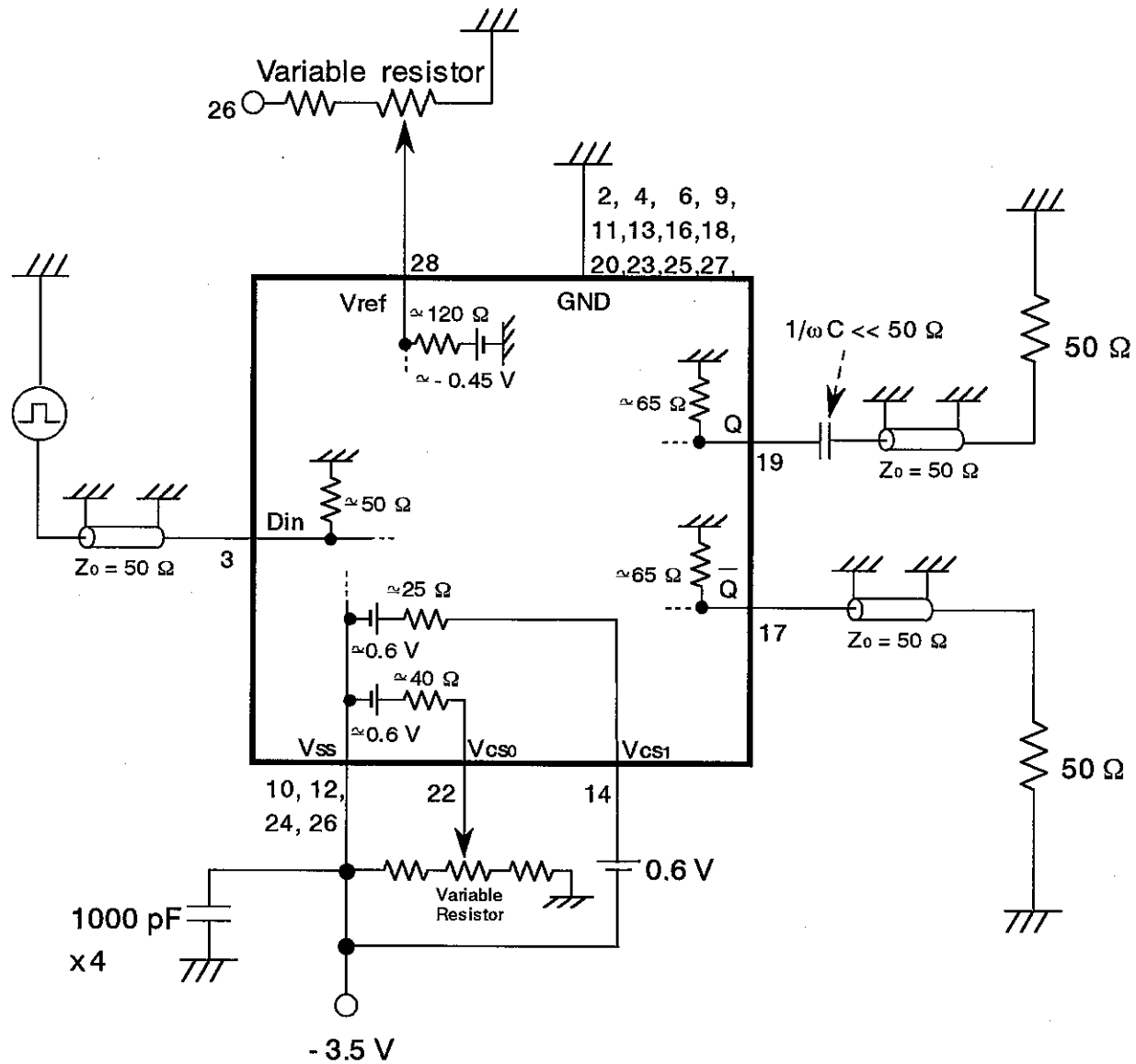
- - - - - - : Vss = - 3.4 V
——— : Vss = - 3.5 V
— - — - - : Vss = - 3.75 V

Measurement Conditions

Vref = - 0.51 V
Vcs1 = Vss + 0.6 V
Din : PN = 31, MR 1 / 2
9.95 Gb / s
VIH = - 0.2 V VIL = - 0.75 V

Results given here were obtained using the NEL test fixture.

SAMPLE IMPLEMENTATION



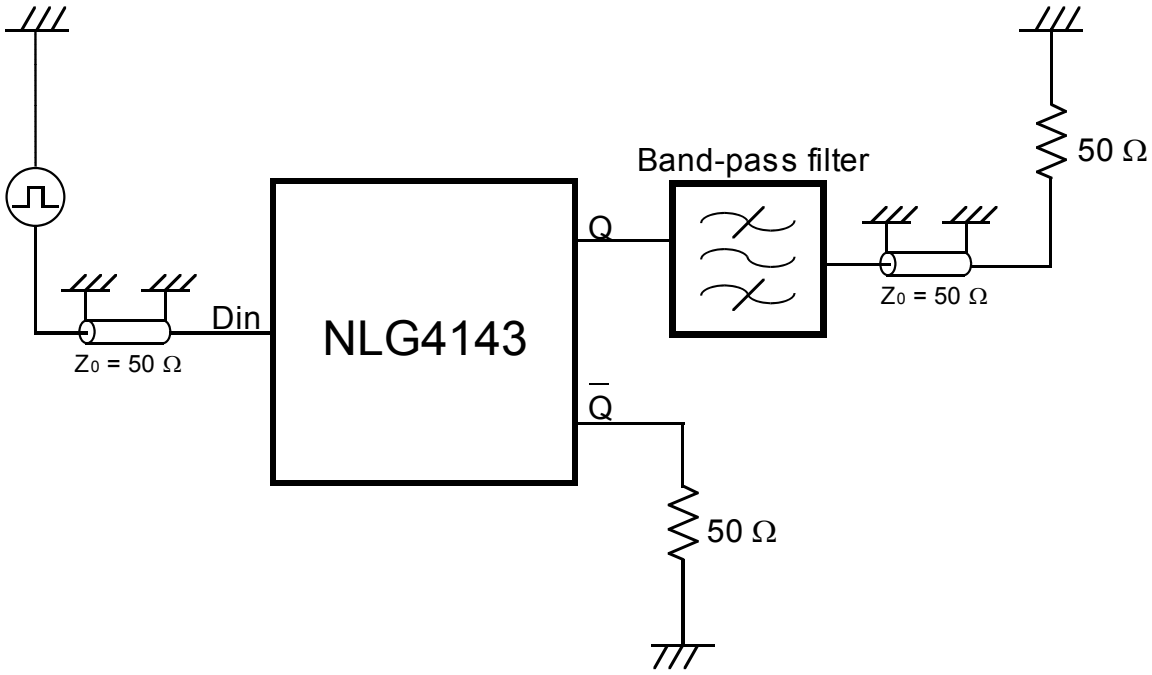
Notes

(1) Numbers represent pin numbers

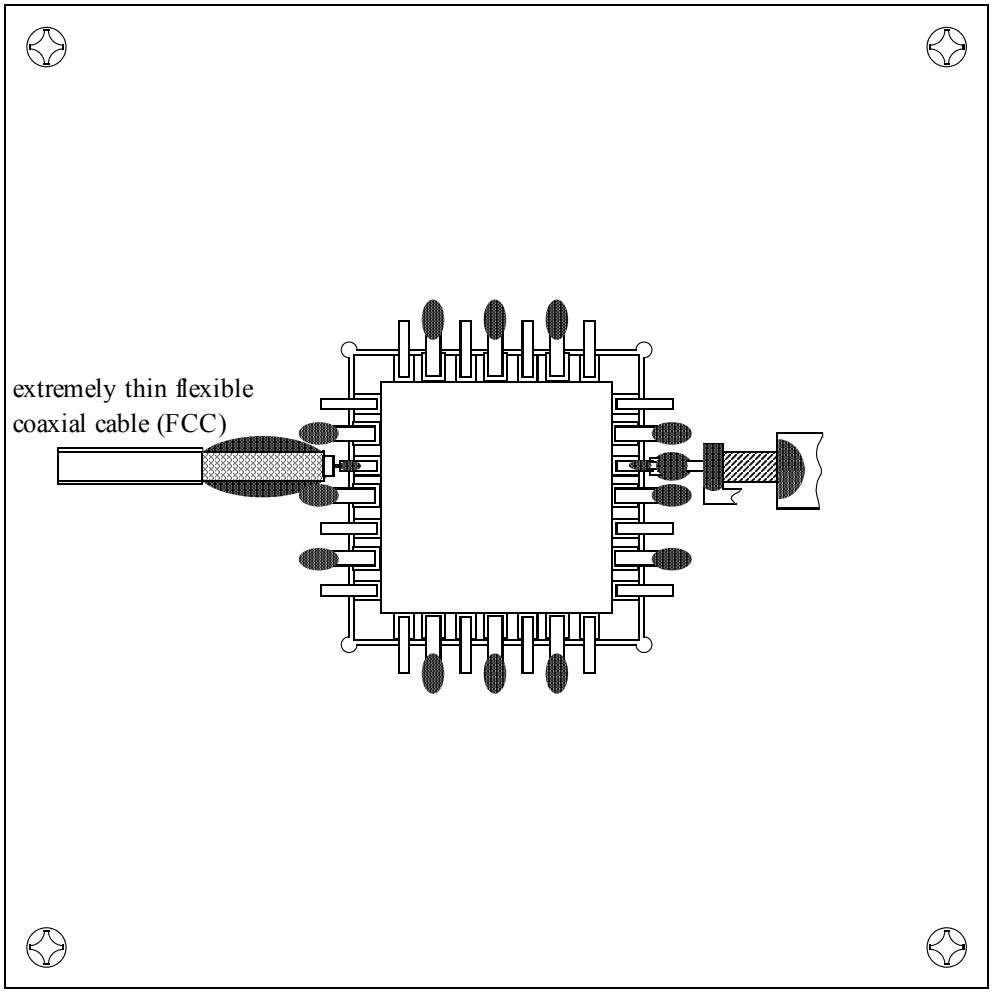
(2) Either AC coupling or DC coupling can be used for all outputs (Q, $\overline{Q}$) .

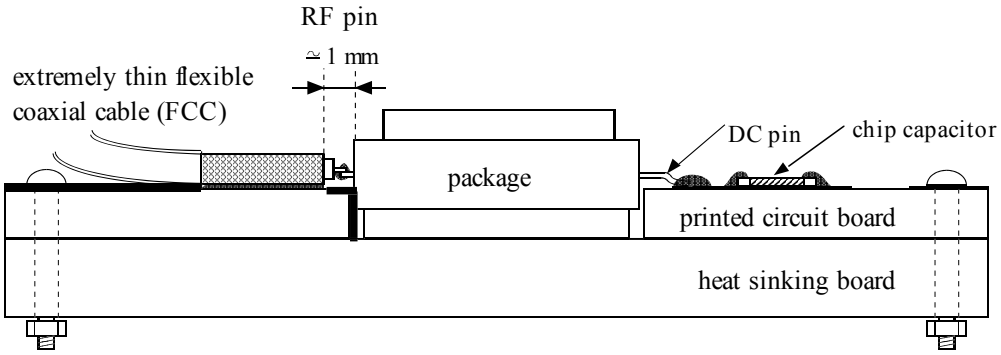
Although not shown here, in place of the above variable resistor, the Vref pin can be connected directly to an external power supply. In this case, apply approximately - 0.5 V.

SAMPLE IMPLEMENTATION
FOR CLOCK RECOVERY FUNCTION



SAMPLE MOUNTING

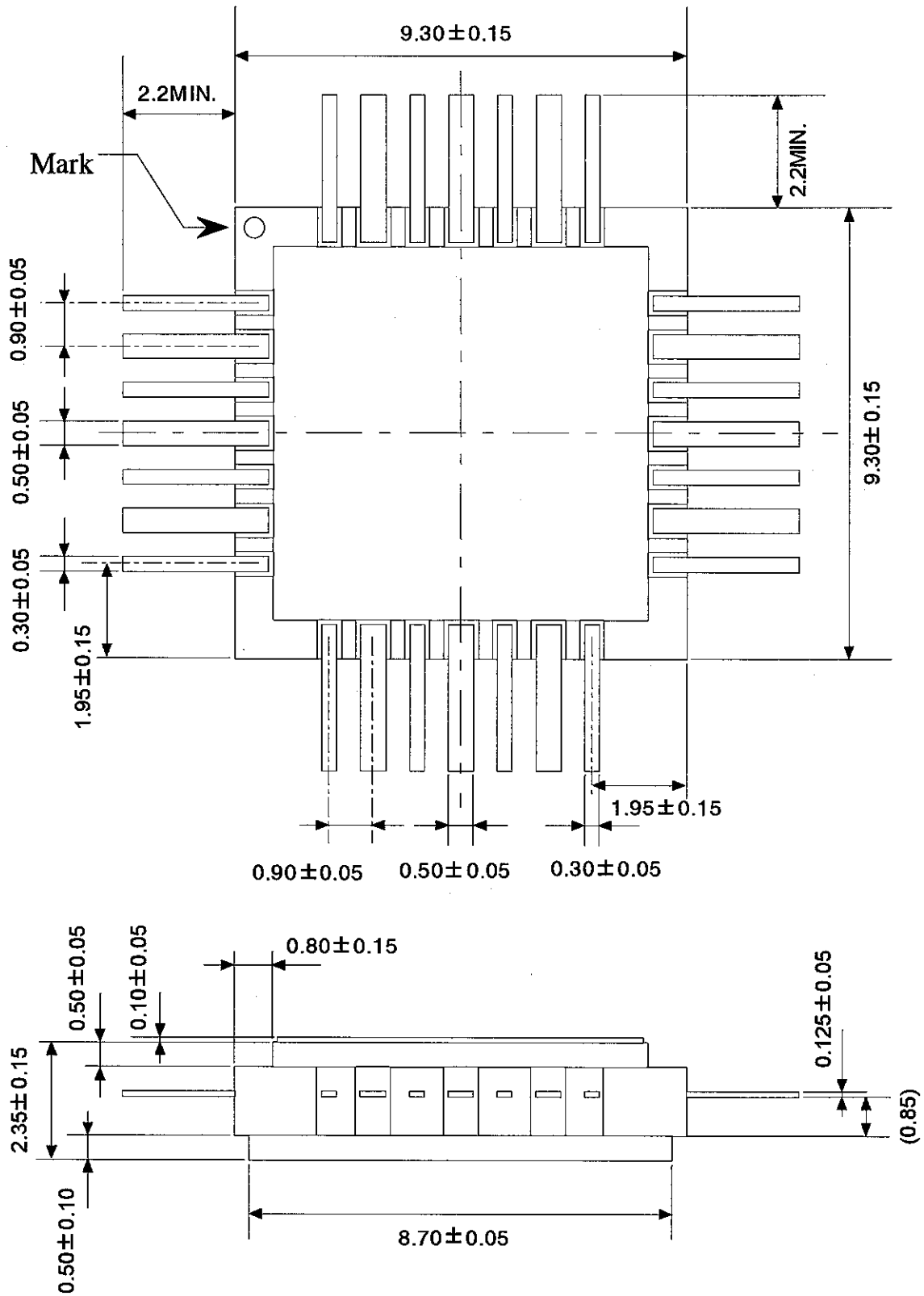




: solder

Caution : The package base should be connected to the ground.

TB 28 - PIN PACKAGE DIMENSION (mm)



HANDLING INSTRUCTIONS

Since the NLG4143 is fabricated with GaAs MESFET's (Metal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro-static discharge.

(1) Power Supply Sequence

The following power supply sequence is recommended.

1) Set supply voltages Vss, Vref, Vcs0, Vcs1 and GND to 0 V.
2) Apply Vref and Vss.
3) Apply Vcs0 and Vcs1.

RF signal is recommended to be applied while power supplying and biasing.

(2) Handling Precautions

1) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
2) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M-ohm resistors.
3) Ground all test equipment.
4) Ground all soldering iron tops.
5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

MEMO

Caution

1. In order to improve products and technology, specifications are subject to change without notice.

2. When using the products, be sure the latest information and specifications are used.

3. Circuit drawings etc. shall be provided for the purpose of information only on application examples not for actual installation of equipment. NTT Electronics Corp. shall not assume any liability for damage that may result from the use of these circuit drawings etc. NTT Electronics Corp. shall not assent to or guarantee any rights of execution for patent rights of the third parties and other rights that may be raised for use of these circuit drawings.

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7. The product is controlled under the 'Foreign Exchange and Foreign Trade Law'. In the case of exporting this product, it is requested that you take necessary procedures to obtain prior approval from the Minister of Economy, Trade and Industry.

8. The product uses GaAs (gallium arsenide). GaAs powder and vapor are dangerous for humans. Do not break, cut, crush or chemically destroy the products. To dispose of the products, follow the relevant regulations and laws; do not mix with general industrial waste and domestic garbage.

9. Any questions should be directed to the Sales Department of NTT Electronics Corp.

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