NEL

NS GD E125A
29 Oct. 2001
PRELIMINARY

NLG4309
12.5 Gb/s 1：16 DEMUX
（LVDS INTERFACE）

The NLG4309 is an ultra-fast 1:16 demultiplexer. It divides serial input signal operating at up to 12.5 Gb/s into 16 parallel LVDS output signals as fast as 781.25 Mb/s（MIN.）.
It is designed with LSCFL（Low-power Source Coupled FET Logic）.
Owing to built-in 50-ohm termination resistors, external termination resistors are unnecessary for impedance matching.
The NLG4309 is fabricated using the 0.15-μm gate length A-SAINT（**A**dvanced **S**elf-**A**ligned **I**mplantation for N^+ layer **T**echnology）process.

FEATURES

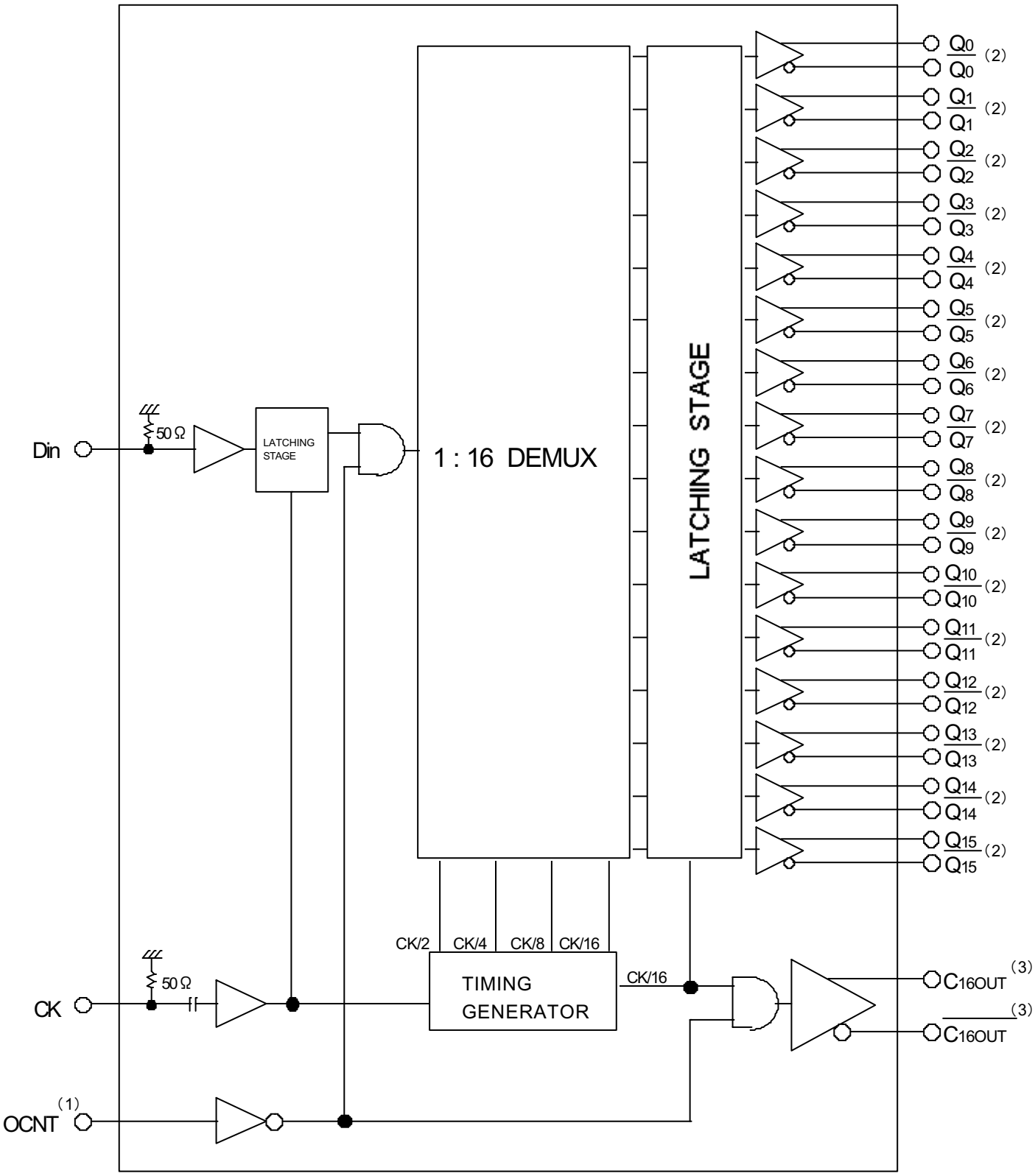
Ultra-high speed：maximum clock frequency f_{MAX}：12.5 GHz ［MIN.］
minimum clock frequency f_{MIN}：2 GHz ［MAX.］
output rise time tr = 200 ps（20-80％）［TYP.］
output fall time tf = 190 ps（20-80％）［TYP.］

High reliability ：Hermetically-sealed package

APPLICATIONS

- Serial-to-parallel converters
- High speed testers
- Digital transmission system receivers
- Computer links
- Board links

FUNCTIONAL DIAGRAM



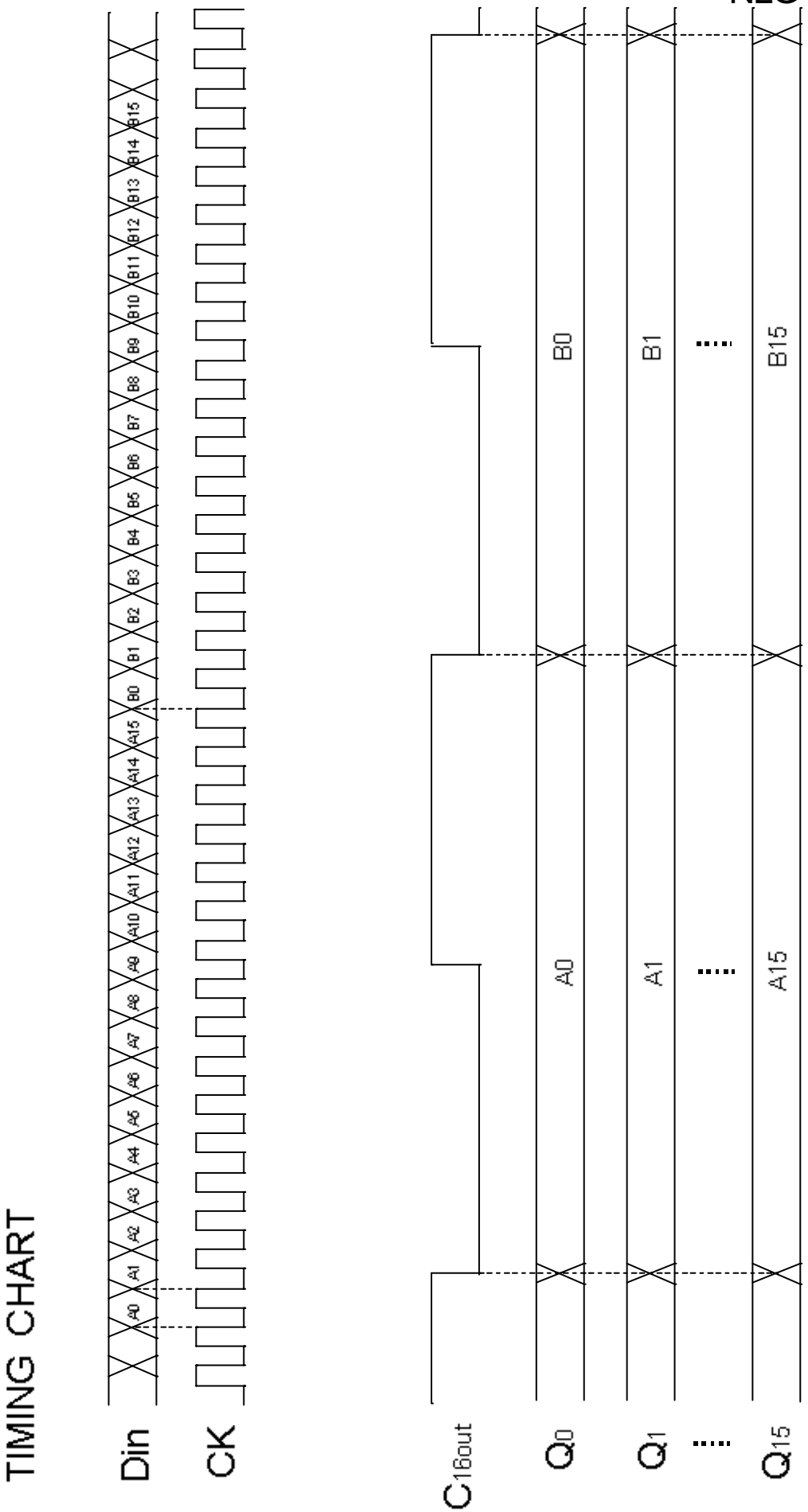
Notes

(1) Output control terminal (LV-TTL input)
When input is high level, $Q_0 \sim Q_{15}$ and C_{16OUT} become low level, and $\overline{Q_0} \sim \overline{Q_{15}}$ and $\overline{C_{16OUT}}$ become high level.

(2) Data output terminals (LVDS output)

(3) 1/16 clock output terminals (LVDS output)

TIMING CHART



PIN CONNECTION TABLE

No.	NAME	FUNCTION	No.	NAME	FUNCTION
1	GND	Ground (0.0V)	43	T_{CMON}	Case Temperature Monitor
2	V_{DD}	Power Supply 2 (+3.3 V)	44	V_{DD}	Power Supply 2 (+3.3 V)
3	Q_1	1/16 Data Output 1 (True) (3)	45	$\overline{Q_{14}}$	1/16 Data Output 14 (Comp.) (3)
4	$\overline{Q_1}$	1/16 Data Output 1 (Comp.) (3)	46	Q_{14}	1/16 Data Output 14 (True) (3)
5	Q_3	1/16 Data Output 3 (True) (3)	47	$\overline{Q_{12}}$	1/16 Data Output 12 (Comp.) (3)
6	$\overline{Q_3}$	1/16 Data Output 3 (Comp.) (3)	48	Q_{12}	1/16 Data Output 12 (True) (3)
7	Q_5	1/16 Data Output 5 (True) (3)	49	$\overline{Q_{10}}$	1/16 Data Output 10 (Comp.) (3)
8	$\overline{Q_5}$	1/16 Data Output 5 (Comp.) (3)	50	Q_{10}	1/16 Data Output 10 (True) (3)
9	Q_7	1/16 Data Output 7 (True) (3)	51	$\overline{Q_8}$	1/16 Data Output 8 (Comp.) (3)
10	$\overline{Q_7}$	1/16 Data Output 7 (Comp.) (3)	52	Q_8	1/16 Data Output 8 (True) (3)
11	GND	Ground (0.0V)	53	GND	Ground (0.0V)
12	Q_9	1/16 Data Output 9 (True) (3)	54	$\overline{Q_6}$	1/16 Data Output 6 (Comp.) (3)
13	$\overline{Q_9}$	1/16 Data Output 9 (Comp.) (3)	55	Q_6	1/16 Data Output 6 (True) (3)
14	Q_{11}	1/16 Data Output 11 (True) (3)	56	$\overline{Q_4}$	1/16 Data Output 4 (Comp.) (3)
15	$\overline{Q_{11}}$	1/16 Data Output 11 (Comp.) (3)	57	Q_4	1/16 Data Output 4 (True) (3)
16	Q_{13}	1/16 Data Output 13 (True) (3)	58	$\overline{Q_2}$	1/16 Data Output 2 (Comp.) (3)
17	$\overline{Q_{13}}$	1/16 Data Output 13 (Comp.) (3)	59	Q_2	1/16 Data Output 2 (True) (3)
18	Q_{15}	1/16 Data Output 15 (True) (3)	60	$\overline{Q_0}$	1/16 Data Output 0 (Comp.) (3)
19	$\overline{Q_{15}}$	1/16 Data Output 15 (Comp.) (3)	61	Q_0	1/16 Data Output 0 (True) (3)
20	V_{DD}	Power Supply 2 (+3.3 V)	62	V_{DD}	Power Supply 2 (+3.3 V)
21	GND	Ground (0.0V)	63	GND	Ground (0.0V)
22	GND	Ground (0.0V)	64	GND	Ground (0.0V)
23	NC	No Internal Connection	65	V_{SS}	Power Supply 1 (- 3.5 V)
24	GND	Ground (0.0V)	66	NC	No Internal Connection
25	V_{SS}	Power Supply 1 (- 3.5 V)	67	NC	No Internal Connection
26	GND	Ground (0.0V)	68	NC	No Internal Connection
27	Vrefd	Data Input Ref. (1)	69	NC	No Internal Connection
28	GND	Ground (0.0V)	70	GND	Ground (0.0V)
29	Din	Data Input	71	$\overline{C_{16OUT}}$	1/16 Clock Output (Comp.) (3)
30	GND	Ground (0.0V)	72	GND	Ground (0.0V)
31	V_{SS}	Power Supply 1 (- 3.5 V)	73	C_{16OUT}	1/16 Clock Output (True) (3)
32	GND	Ground (0.0V)	74	GND	Ground (0.0V)
33	CK	Clock Input	75	OCNT	Output Control Input
34	GND	Ground (0.0V)	76	GND	Ground (0.0V)
35	Vrefc	Clock Input Ref. (2)	77	NC	No Internal Connection
36	GND	Ground (0.0V)	78	GND	Ground (0.0V)
37	NC	No Internal Connection	79	NC	No Internal Connection
38	GND	Ground (0.0V)	80	NC	No Internal Connection
39	V_{SS}	Power Supply 1 (- 3.5 V)	81	NC	No Internal Connection
40	GND	Ground (0.0V)	82	NC	No Internal Connection
41	NC	No Internal Connection	83	V_{SS}	Power Supply 1 (- 3.5 V)
42	GND	Ground (0.0V)	84	GND	Ground (0.0V)

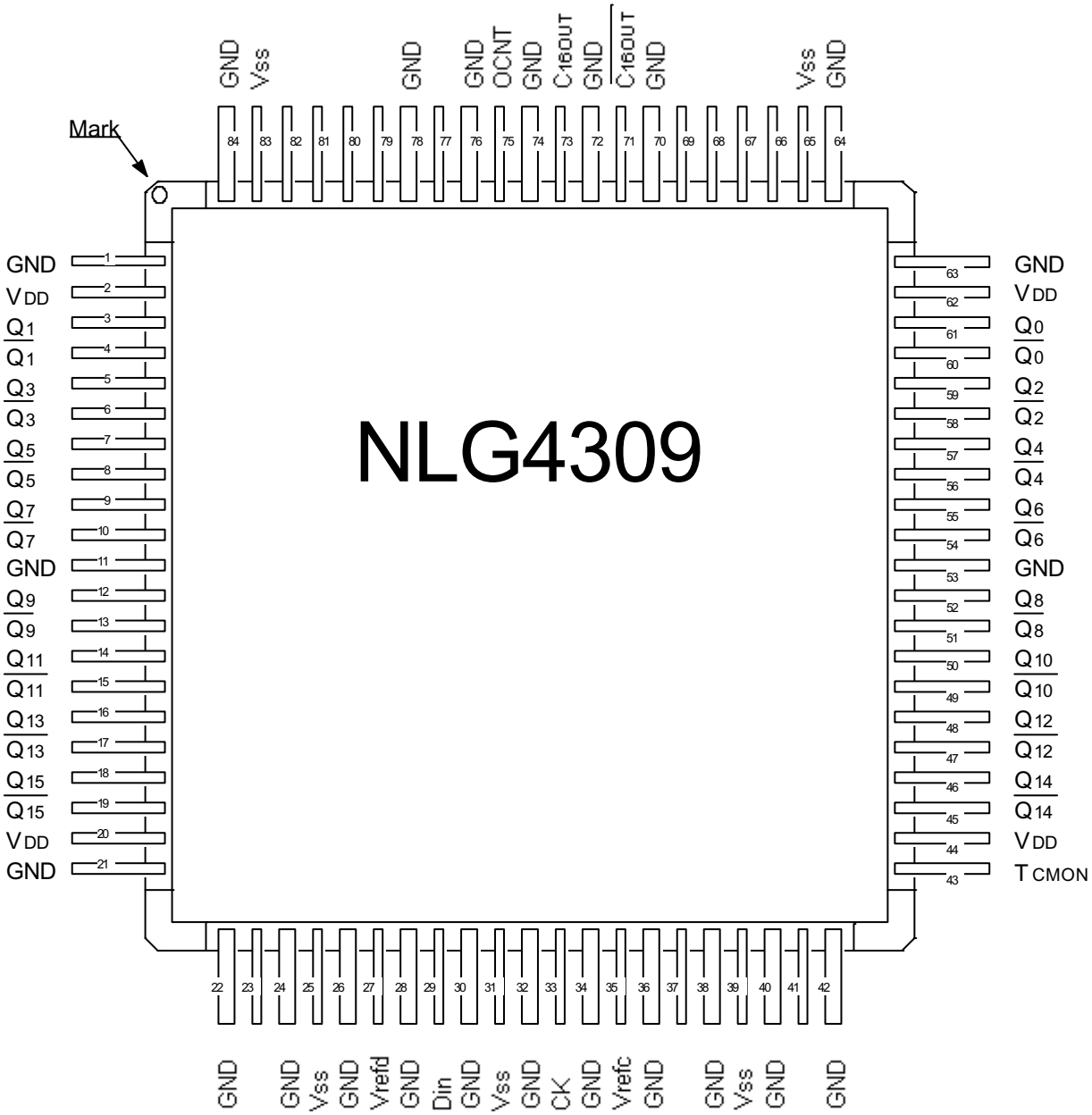
Notes

(1) V_{refd} : Internally generated reference voltage that determines the data input threshold level.
By applying - 0.75 to - 0.2 V externally to this pins, an arbitrary data input threshold voltage can be established.

(2) V_{refc} : Internally generated reference voltage that determines the clock input threshold level.

(3) Terminate unused output pins between true output and complementary output through 100-ohm resistor.

CONNECTION DIAGRAM（TOP VIEW）



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{SS}	Power Supply Voltage 1	+ 0.5 V ～ - 4.0 V
V_{DD}	Power Supply Voltage 2	+ 4.0 V ～ - 0.5 V
Vindin	Applied Voltage at Data Input (Din)	+ 0.3 V ～ - 1.6 V
Vin	Applied Voltage Amplitude at Clock Input (CK)	1.6 Vp-p
Vinck	Applied Voltage at Clock Input (CK)	+ 1.6 V ～ - 1.6 V
V_{inTTL}	Applied Voltage at OCNT Input (OCNT)	+ 4.0 V ～ - 0.5 V
V_{outD}	Applied Voltage at Signal Outputs under Bias (Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$, C_{16OUT}, $\overline{C_{16OUT}}$)	+ 3.3 V ～ 0.0 V
Vrefd	Applied Voltage at Vrefd pin	+ 0.3 V ～ - 1.6 V
Vrefc	Applied Voltage at Vrefc pin under Bias	- 1.0 V ～ - 2.5 V
V_{TCMON}	Applied Voltage at Case Temperature Monitor pin	- 1.0 V ～ + 1.0 V
Tstor	Storage Temperature	- 60 ℃ ～ +150 ℃
Tc(1)	Case Temperature under Bias	- 60 ℃ ～ +125 ℃

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{SS}	Power Supply Voltage 1	- 3.75	- 3.5	- 3.4	V
V_{DD}	Power Supply Voltage 2	+3.1	+3.3	+3.5	V
Vrefd	Data Input Reference Voltage	Adjust in the range from -0.75 V to -0.2 V			V
Vrefc	Clock Input Reference Voltage	Normally Open			V
Din	Data Input Interface	DC Coupling (See DC Characteristics)			—
CK	Clock Input Interface	DC Coupling (See DC Characteristics) or AC Coupling (See AC Characteristics)			—
OCNT	Output Control Input Interface	Low-voltage TTL (LV-TTL) logic (See DC Characteristics)			—
OUT	Data Output, 1/16 Clock Output Interface (Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$, C_{16OUT}, $\overline{C_{16OUT}}$)	Low-voltage differential signals (LVDS), Connect 100 Ω between true output and complementary output (See DC Characteristics)			—
T_{CMON}	Case Temperature Monitor	Connect to a DC voltmeter for estimating case temperature. Relationship between T_{CMON} and case temperature is shown in page 17.			—

Notes

(1) Tc : temperature at package base.

DC CHARACTERISTICS

(V_{SS} = -3.75 V ～ -3.4 V, V_{DD} = +3.1 V ～ +3.5 V, GND = 0.0 V, Tc = 0 ～ 85℃ (1))

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
V_{IH}	Input Voltage, High (Din, CK)	-0.2	0.0		V	
V_{IL}	Input Voltage, Low (Din, CK)		- 0.9	-0.75	V	
V_{ODH}	Output Voltage, High (Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$, C_{16OUT}, $\overline{C_{16OUT}}$)		+1.45	+2.0	V	(2)
V_{ODL}	Output Voltage, Low (Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$, C_{16OUT}, $\overline{C_{16OUT}}$)	+0.6	+1.15		V	(2)
V_{OD}	Differential Output Voltage	0.18	0.3	0.5	V	(2)
V_{OS}	Output Offset Voltage	+0.7	+1.3	+1.9	V	(2)
V_{IHTTL}	LV-TTL Input Voltage, High (OCNT)	+2.0		+3.3	V	
V_{ILTTL}	LV-TTL Input Voltage, Low (OCNT)	0.0		+0.8	V	
I_{SS}	Power Supply Current (V_{SS})		0.68	0.91	A	
I_{DD}	Power Supply Current (V_{DD})		140	200	mA	

AC CHARACTERISTICS

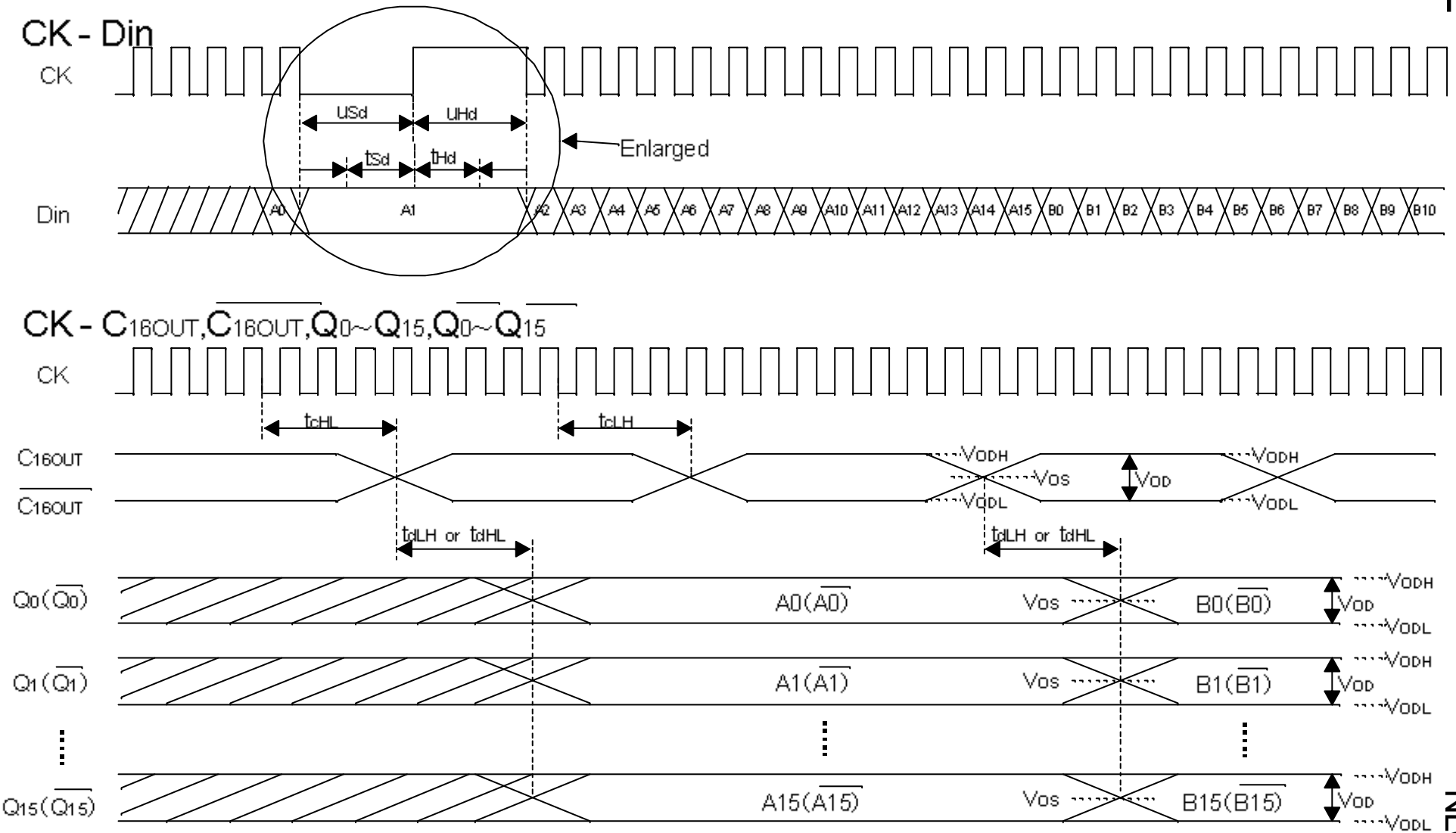
(V_{SS} = -3.75 V ～ -3.4 V, V_{DD} = +3.1 V ～ +3.5 V, GND = 0.0 V, Tc = 0 ～ 85℃ (1),
Vrefd: Adjust in the range from -0.75 V to -2.0 V, Vrefc: Open)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
Vin	Minimum Clock Input Voltage Amplitude			0.5	Vp-p	
f_{MAX}	Maximum Clock Frequency	12.5			GHz	(3)
f_{MIN}	Minimum Clock Frequency			2	GHz	(3)
tr	Output Rise Time (Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$ 20-80%)		200	360	ps	
tf	Output Fall Time (Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$ 20-80%)		190	360	ps	
tr_C	Output Rise Time (C_{16OUT}, $\overline{C_{16OUT}}$ 20-80%)		110	190	ps	
tf_C	Output Fall Time (C_{16OUT}, $\overline{C_{16OUT}}$ 20-80%)		100	160	ps	
t_{dLH}	Output Rise Delay (C_{16OUT} - Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$)	160	370	590	ps	(2),(4)
t_{dHL}	Output Fall Delay (C_{16OUT} - Q_0～Q_{15}, $\overline{Q_0}$～$\overline{Q_{15}}$)	160	370	590	ps	(2),(4)
t_{cLH}	Output Rise Delay (CK - C_{16OUT}, $\overline{C_{16OUT}}$)	500	620	730	ps	(2)
t_{cHL}	Output Fall Delay (CK - C_{16OUT}, $\overline{C_{16OUT}}$)	500	620	730	ps	(2)
t_{Sd}	Minimum Setup Time (Din - CK)		-5	10	ps	(2)
t_{Hd}	Minimum Hold Time (CK - Din)		25	45	ps	(2)

Notes

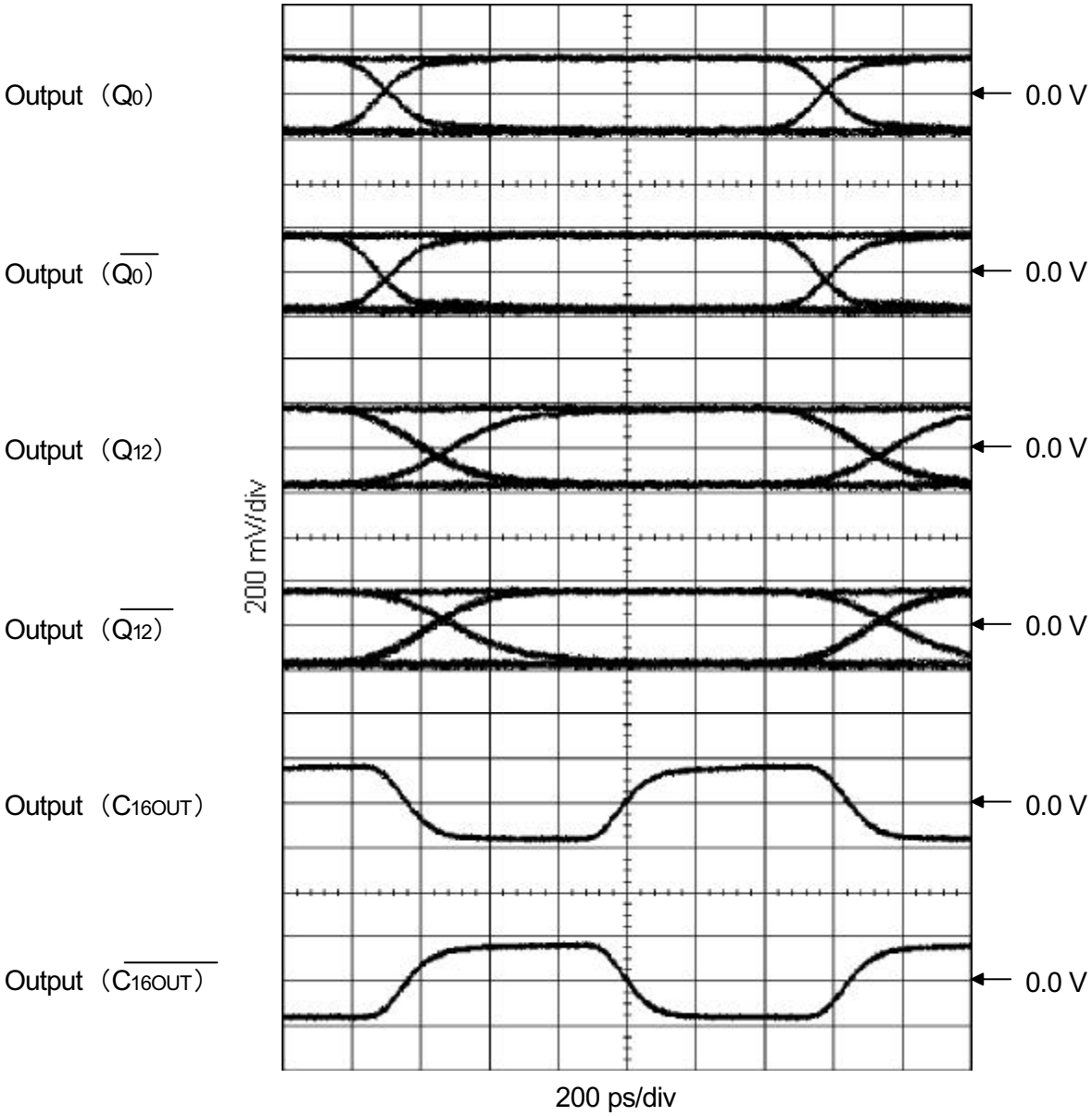
(1) Tc: temperature at package base.
(2) See page 8.
(3) Confirmed by error-free operation using a pseudo-random pattern having a word length of 2^{31}-1 bits.
(4) Includes channel-to-channel skew.

TIMING CHART (INCLUDING DELAY TIMES)



(See the timing chart on page 3 for a more complete logical description. Here, tSd and tHd are the minimum setup and hold times as defined on the previous page; uSd and uHd are the corresponding user setup and hold times.)

SAMPLE OUTPUT WAVEFORMS（12.5 Gb/s）



Measurement Conditions

VSS = - 3.5 V

VDD = + 3.3 V

Vrefd : Open

Vrefc : Open

OCNT = + 0.8 V

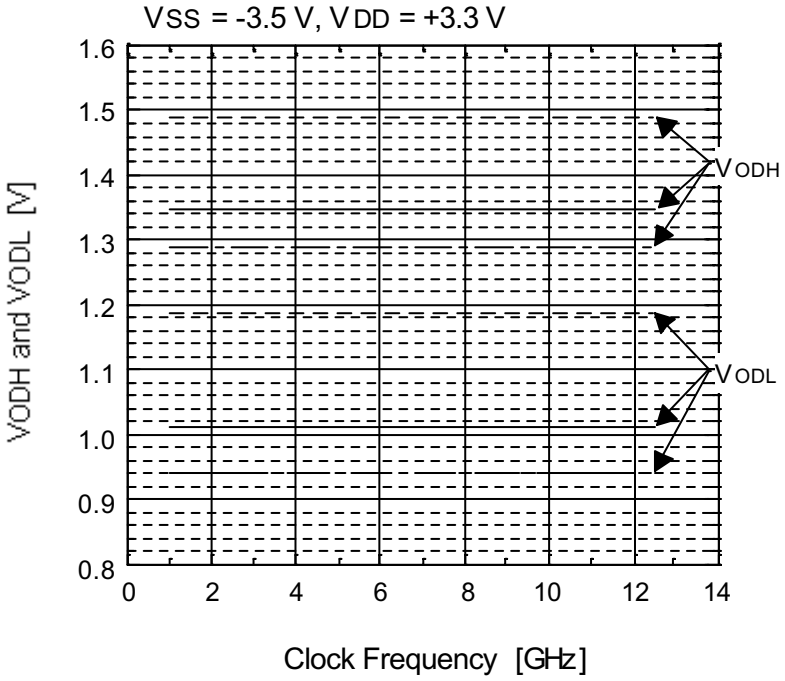
Din : 12.5 Gb/s, PN = 31, VIH = - 0.2 V, VIL = - 0.75 V

CK : 12.5 GHz, Vin = 0.5 Vp-p, DC coupling

Tc = 45 ℃

LVDS outputs (Q0～Q15, $\overline{Q0}$～$\overline{Q15}$, C16OUT , $\overline{C16OUT}$) connected to the 50-ohm impedance pins of a sampling oscilloscope via DC blocks. Results given here were obtained using the NEL test fixture.

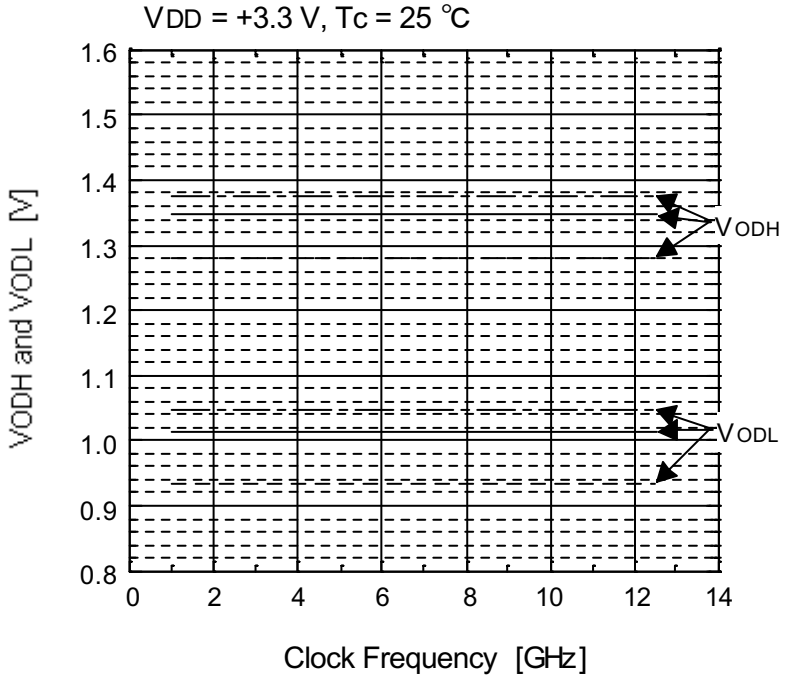
SAMPLE AC CHARACTERISTICS (Q0～Q15, $\overline{Q0}$～$\overline{Q15}$)



—·—·— : Tc = 0 ℃
———— : Tc = 25 ℃
– – – – – – : Tc = 85 ℃

Measurement Conditions

Din : VIH = -0.2 V, VIL = -0.75 V
CK : Vin = 0.5 Vp-p
Vrefd : Open
Vrefc : Open
OCNT = + 0.8 V
Results given here were obtained using the NEL test fixture.

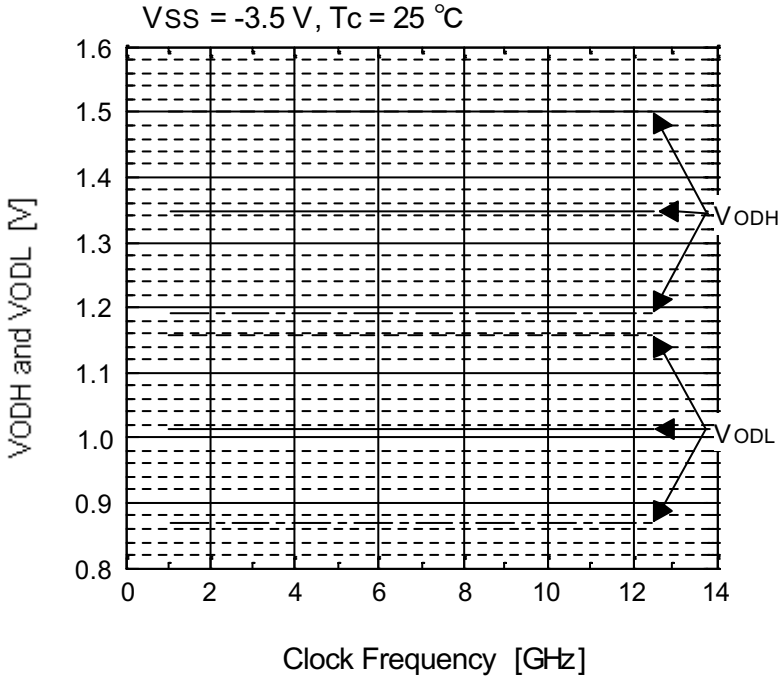


—·—·— : VSS = - 3.4 V
———— : VSS = - 3.5 V
– – – – – – : VSS = - 3.75 V

Measurement Conditions

Din : VIH = -0.2 V, VIL = -0.75 V
CK : Vin = 0.5 Vp-p
Vrefd : Open
Vrefc : Open
OCNT = + 0.8 V
Results given here were obtained using the NEL test fixture.

SAMPLE AC CHARACTERISTICS (Q0～Q15, $\overline{Q0}$～$\overline{Q15}$)

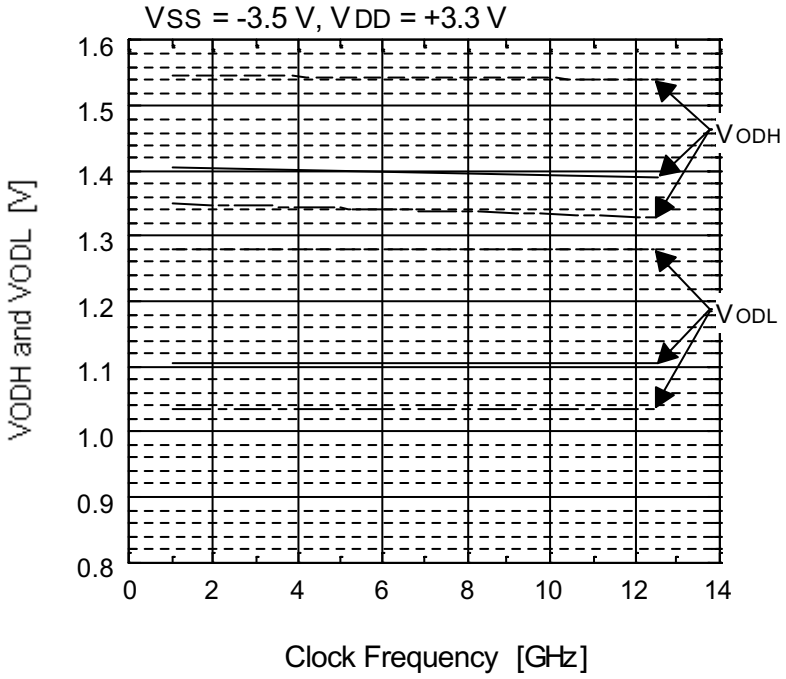


—·—·—· : VDD = + 3.1 V
———— : VDD = + 3.3 V
– – – – – – : VDD = + 3.5 V

Measurement Conditions

Din : VIH = -0.2 V, VIL = -0.75 V
CK : Vin = 0.5 Vp-p
Vrefd : Open
Vrefc : Open
OCNT = + 0.8 V
Results given here were obtained using the NEL test fixture.

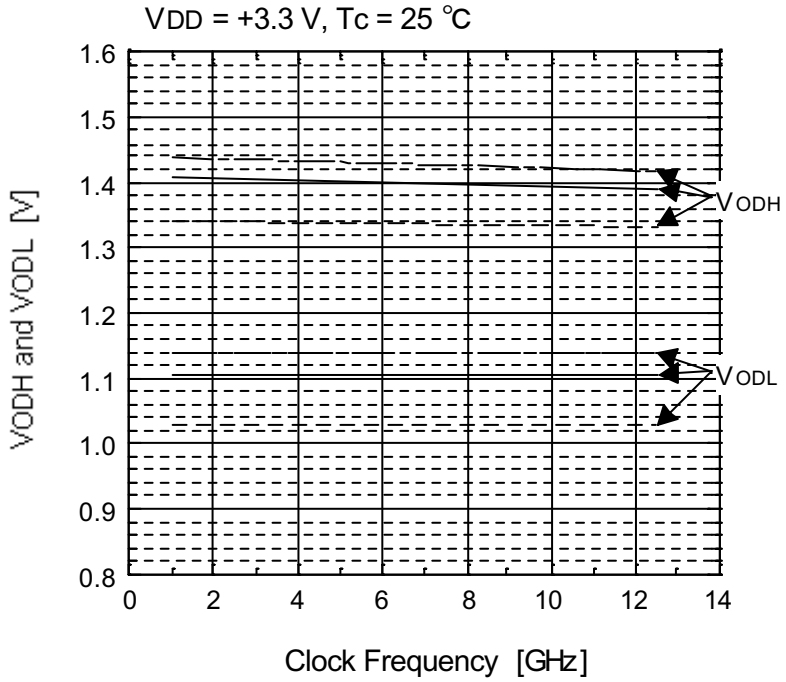
SAMPLE AC CHARACTERISTICS (C_{16OUT}, $\overline{C_{16OUT}}$)



—·—·—· : Tc = 0 ℃
———— : Tc = 25 ℃
– – – – – – : Tc = 85 ℃

Measurement Conditions

Din : V_{IH} = -0.2 V, V_{IL} = -0.75 V
CK : Vin = 0.5 Vp-p
Vrefd : Open
Vrefc : Open
OCNT = + 0.8 V
Results given here were obtained using the NEL test fixture.

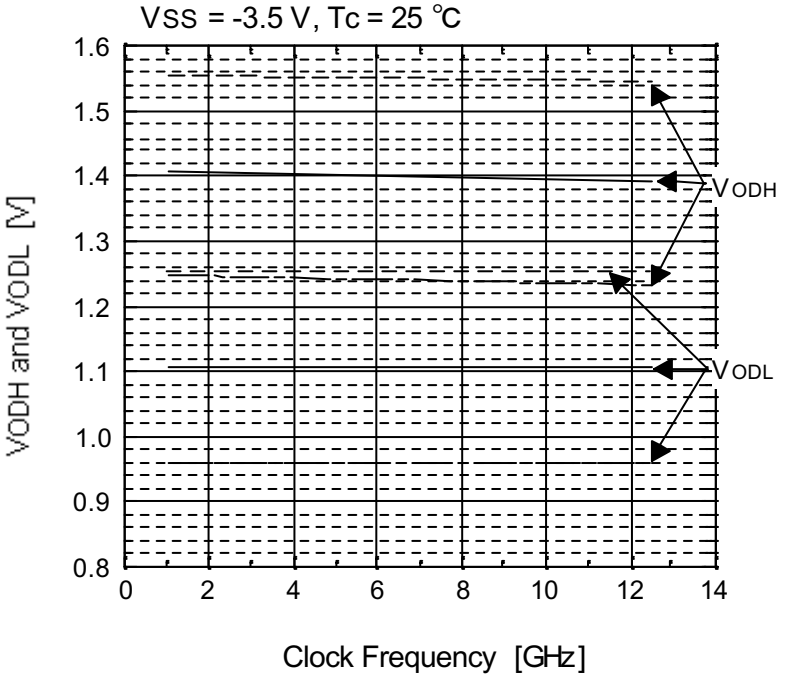


—·—·—· : VSS = - 3.4 V
———— : VSS = - 3.5 V
– – – – – – : VSS = - 3.75 V

Measurement Conditions

Din : V_{IH} = -0.2 V, V_{IL} = -0.75 V
CK : Vin = 0.5 Vp-p
Vrefd : Open
Vrefc : Open
OCNT = + 0.8 V
Results given here were obtained using the NEL test fixture.

SAMPLE AC CHARACTERISTICS (C_{16OUT}, $\overline{C_{16OUT}}$)

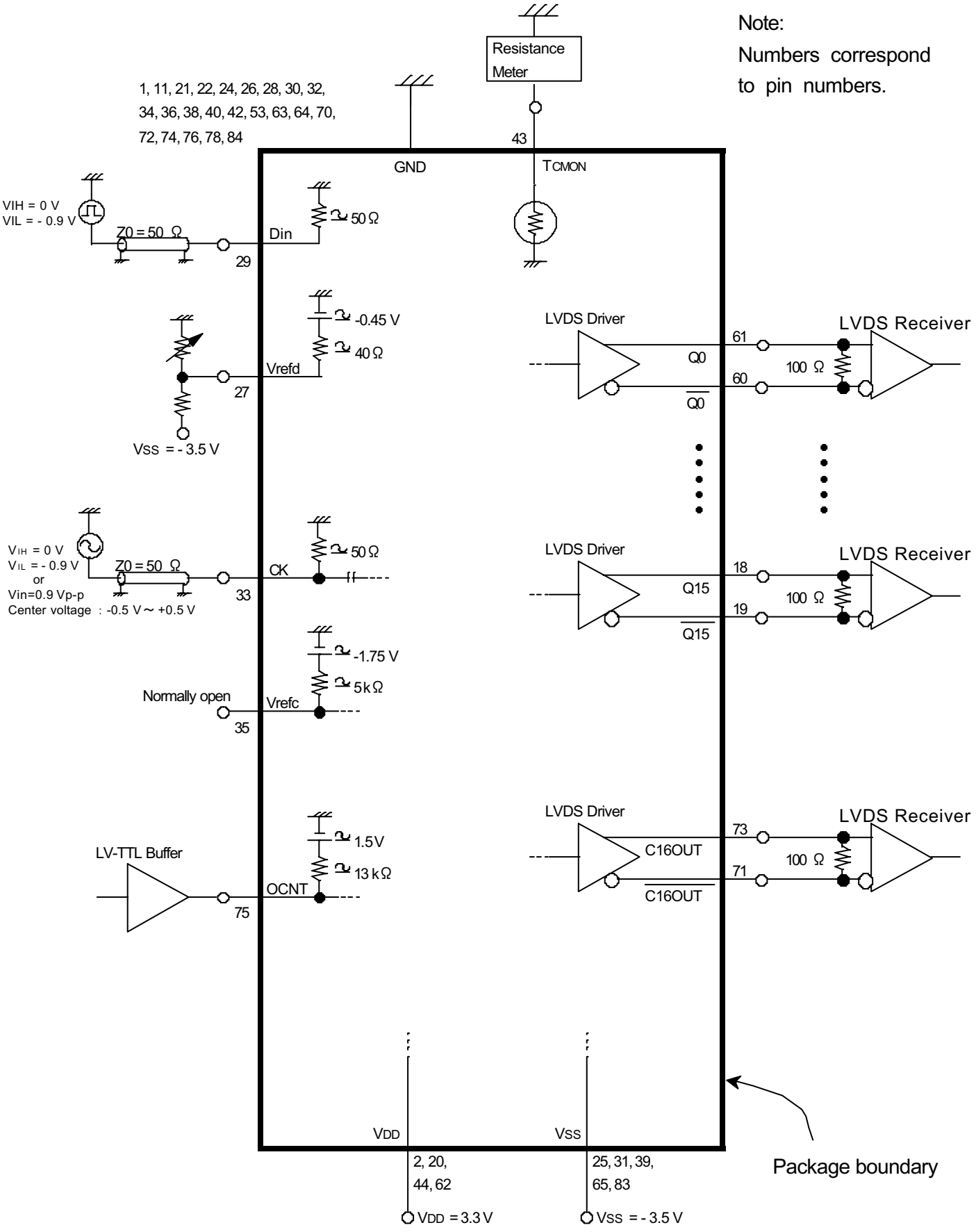


—·—·—· : V_{DD} = + 3.1 V
———— : V_{DD} = + 3.3 V
– – – – – – : V_{DD} = + 3.5 V

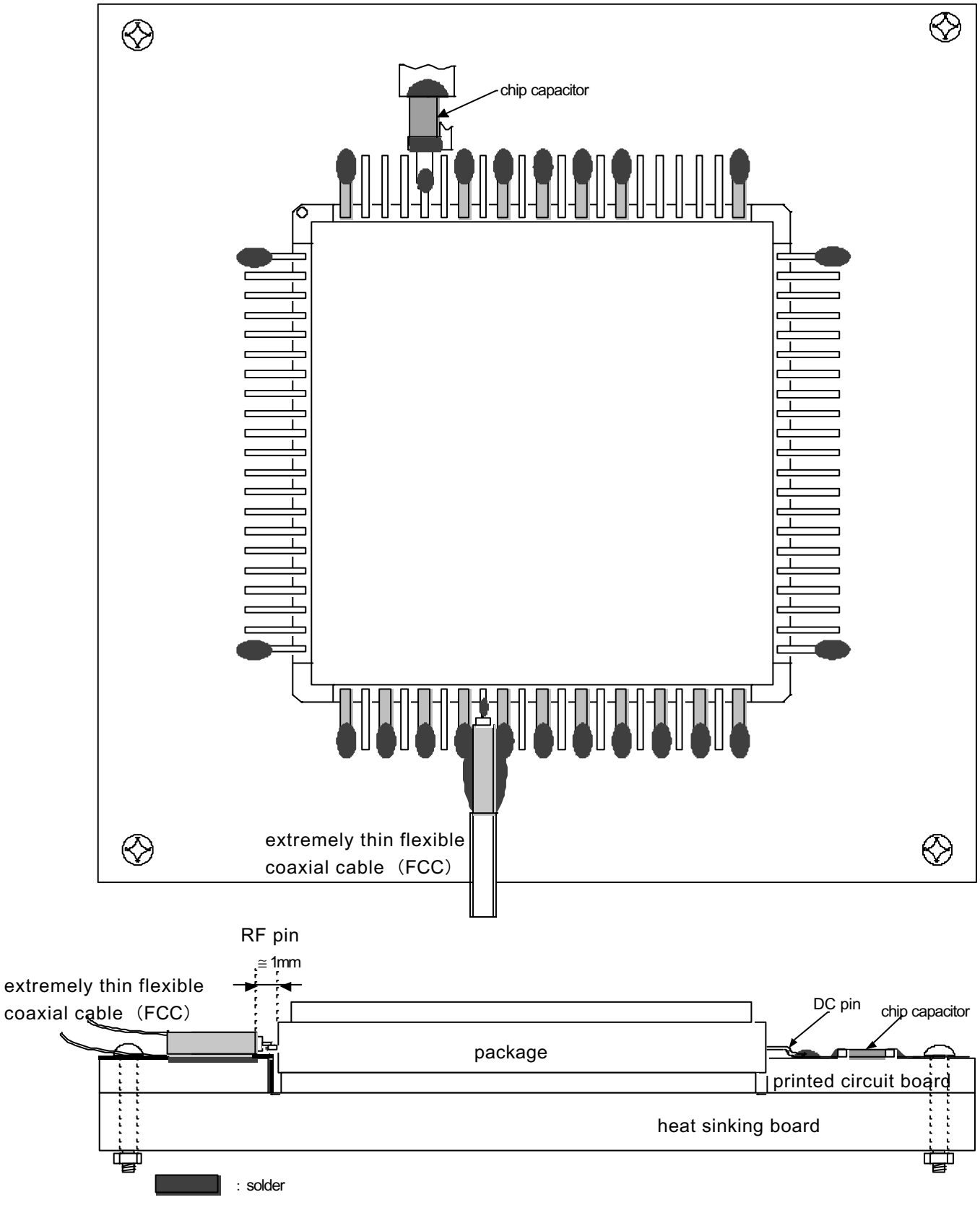
Measurement Conditions

Din : V_{IH} = -0.2 V, V_{IL} = -0.75 V
CK : Vin = 0.5 Vp-p
Vrefd : Open
Vrefc : Open
OCNT = + 0.8 V
Results given here were obtained using the NEL test fixture.

SAMPLE IMPLEMENTATION



SAMPLE MOUNTING



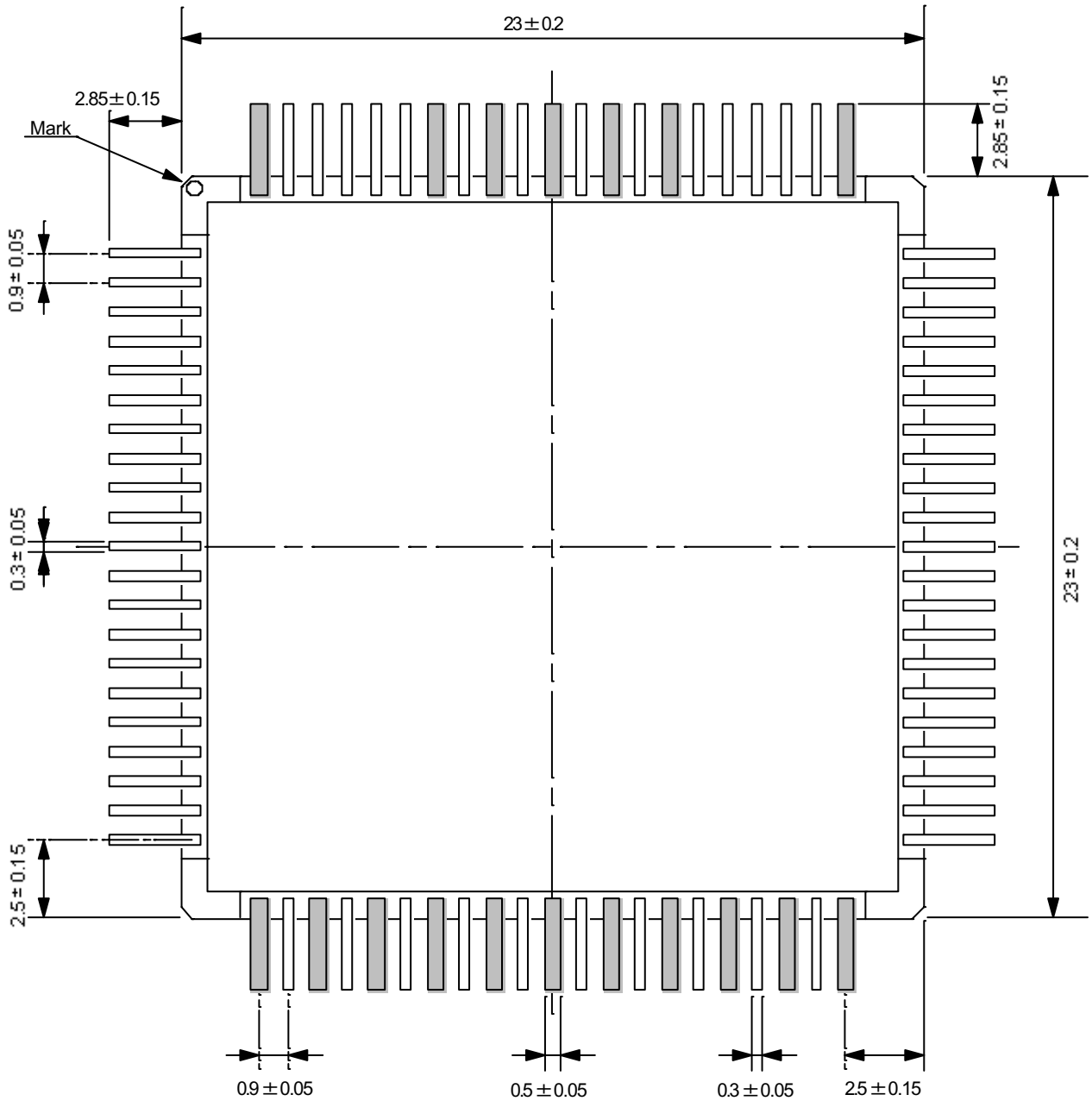
Caution : The package base should be connected to the ground.

TB84-F66 PACKAGE DIMENSION (mm)

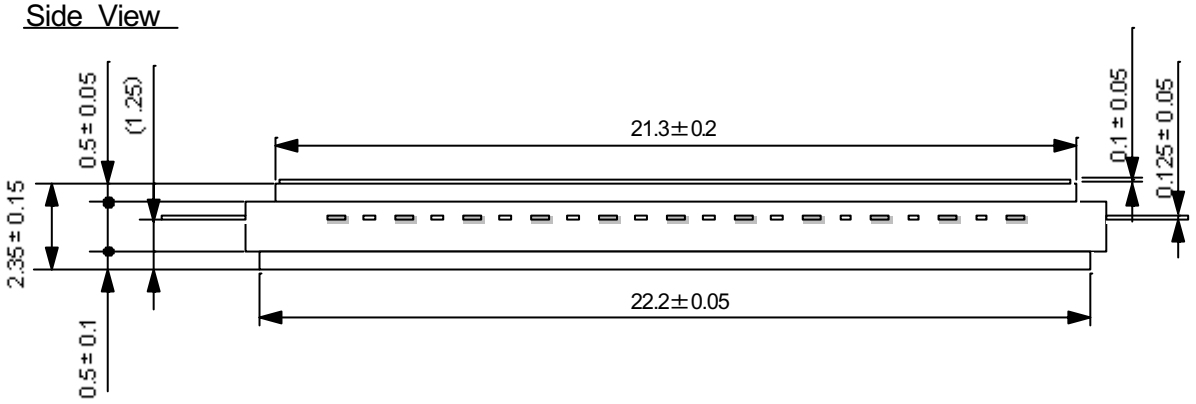
Top View

: GND pin (Pin width 0.5±0.05 mm)

: Signal and power pin (Pin width 0.3±0.05 mm)



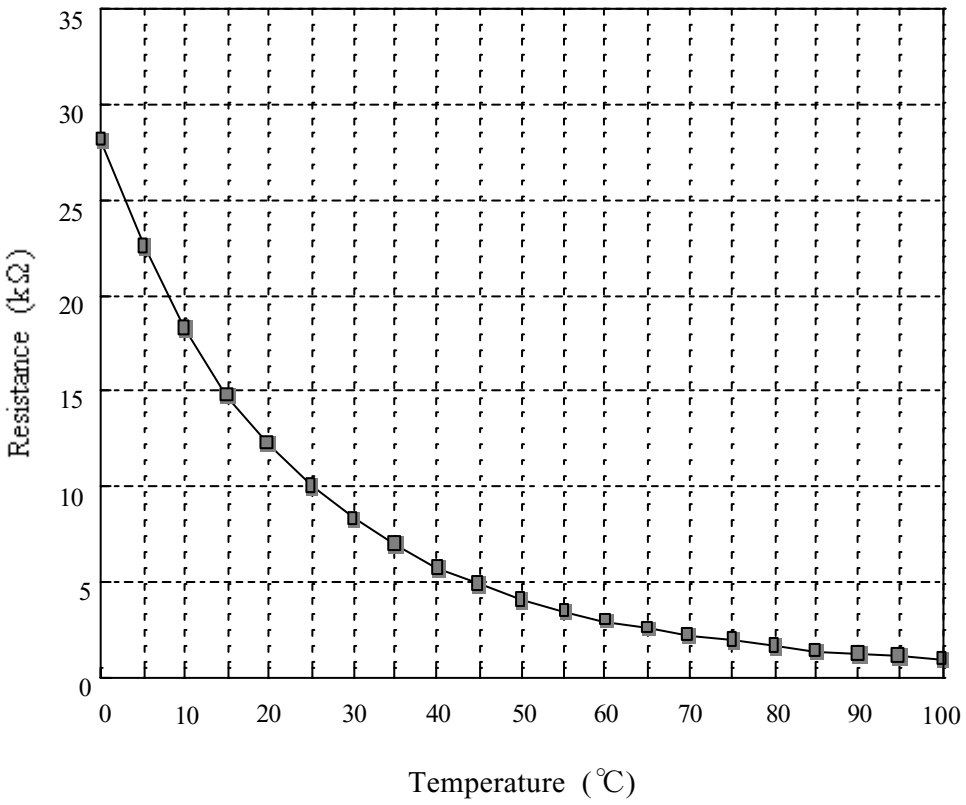
Side View



SAMPLE TEMPERATURE MONITOR

TCMON Resistance Value Versus Case Temperature

Temperature (℃)	Resistance (kΩ) TYP.	Temperature (℃)	Resistance (kΩ) TYP.
0	28.08	55	3.464
5	22.56	60	2.950
10	18.24	65	2.523
15	14.84	70	2.166
20	12.15	75	1.867
25	10.00	80	1.615
30	8.277	85	1.402
35	6.887	90	1.221
40	5.759	95	1.068
45	4.839	100	0.9362
50	4.085		



HANDLING INSTRUCTIONS

Since the NLG4309 is fabricated with GaAs MESFET's (Metal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro-static discharge.

Handling Precautions

1) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
2) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M-ohm resistors.
3) Ground all test equipment.
4) Ground all soldering iron tops.
5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

Caution

1. In order to improve products and technology, specifications are subject to change without notice.

2. When using the products, be sure the latest information and specifications are used.

3. Circuit drawings etc. shall be provided for the purpose of information only on application examples not for actual installation of equipment. NTT Electronics Corp. shall not assume any liability for damage that may result from the use of these circuit drawings etc. NTT Electronics Corp. shall not assent to or guarantee any rights of execution for patent rights of the third parties and other rights that may be raised for use of these circuit drawings.

4. To make a design, the products shall be used within the assured ranges with respect to maximum ratings, voltage, and radiation. NTT Electronics Corp. shall not take any responsibility for damage caused by neglecting the assured values or improper usage.

5. Though NTT Electronics Corp. makes every effort to improve quality and reliability, there is a risk that failure or malfunction may occur in semiconductors. It is therefore necessary that the purchasers should take responsibility for making a design that allows the products to operate safely on equipment and systems without any direct threat to the human body and/or property, should such failures or malfunction occur.

6. NTT Electronics Corp.'s semiconductor device products are designed to be used with multimedia networks communication equipment and related measuring equipment. They have not been developed for such equipment that may affect people's lives. Those who intend to use the products for special purposes that may affect human life as a result of failure or malfunction in the equipment using the products or that require extremely high reliability (e.g. life support, aircraft and space rockets, control in nuclear power facilities, submarine relays, control of operations, etc.) shall contact NTT Electronics Corp. before using the products. NTT Electronics Corp. shall not assume any liability for damage that may occur during operation of the products without prior consultation.

7. Some of the products are classified as strategic materials and the 'Foreign Exchange and Foreign Trade Control Act' applies. Export of the applicable products necessitates obtaining approval from the Japanese Government as required by law.

8. Some of the products use GaAs (gallium arsenide). GaAs powder and vapor are dangerous for humans. Do not break, cut, crush or chemically destroy the products. To dispose of the products, follow the relevant regulations and laws; do not mix with general industrial waste and domestic garbage.

9. Any questions should be directed to the Sales Department of NTT Electronics Corp.