NEL

NS CS E058
May 6, 1997

NLG4131
2 : 1 MUX

The NLG4131 is an ultra-fast 2:1 Multiplexer . Its operative output data speed range is from 8.0 to 11.3 Gb/s [Tc = 25 ℃ , TYP.] .
Designed with LSCFL (Low-power Source Coupled FET Logic) , it uses SCFL I/O levels (V_H : 0.0 V, V_L : - 0.9 V) .
Owing to built-in 50-ohm termination resistors between signal input pins and ground (GND) , external termination resistors are unnecessary for impedance matching .
The NLG4131 is fabricated using the 0.15- μ m gate length A-SAINT (Advanced Self-Aligned Implantation for N^+ layer Technology) process .

FEATURES

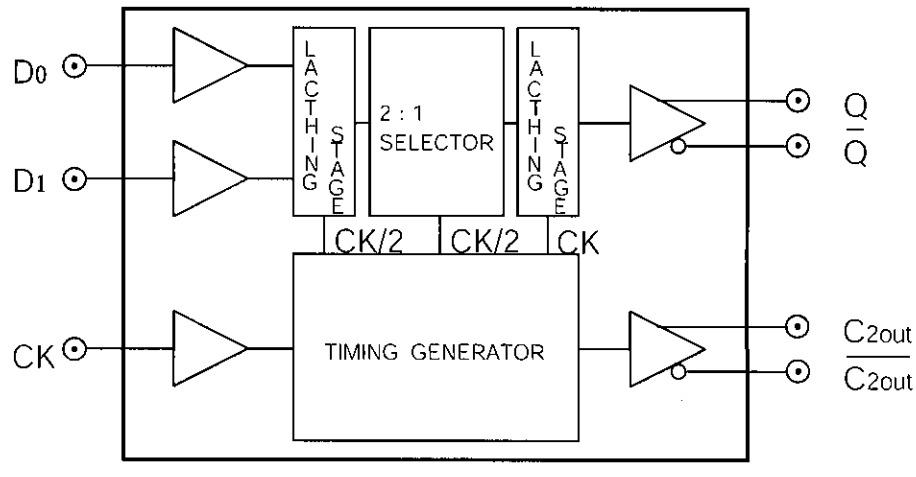
Ultra-high speed : minimum clock frequency f_{MIN} : 8.0 GHz [Tc = 25 ℃ , TYP.]
maximum clock frequency f_{MAX} : 11.3 GHz [Tc = 25 ℃ , TYP.]
output rise time tr = 35 ps (20-80%) [Tc = 25 ℃ , TYP.]
output fall time tf = 30 ps (20-80%) [Tc = 25 ℃ , TYP.]

High Reliability : hermetically-sealed package

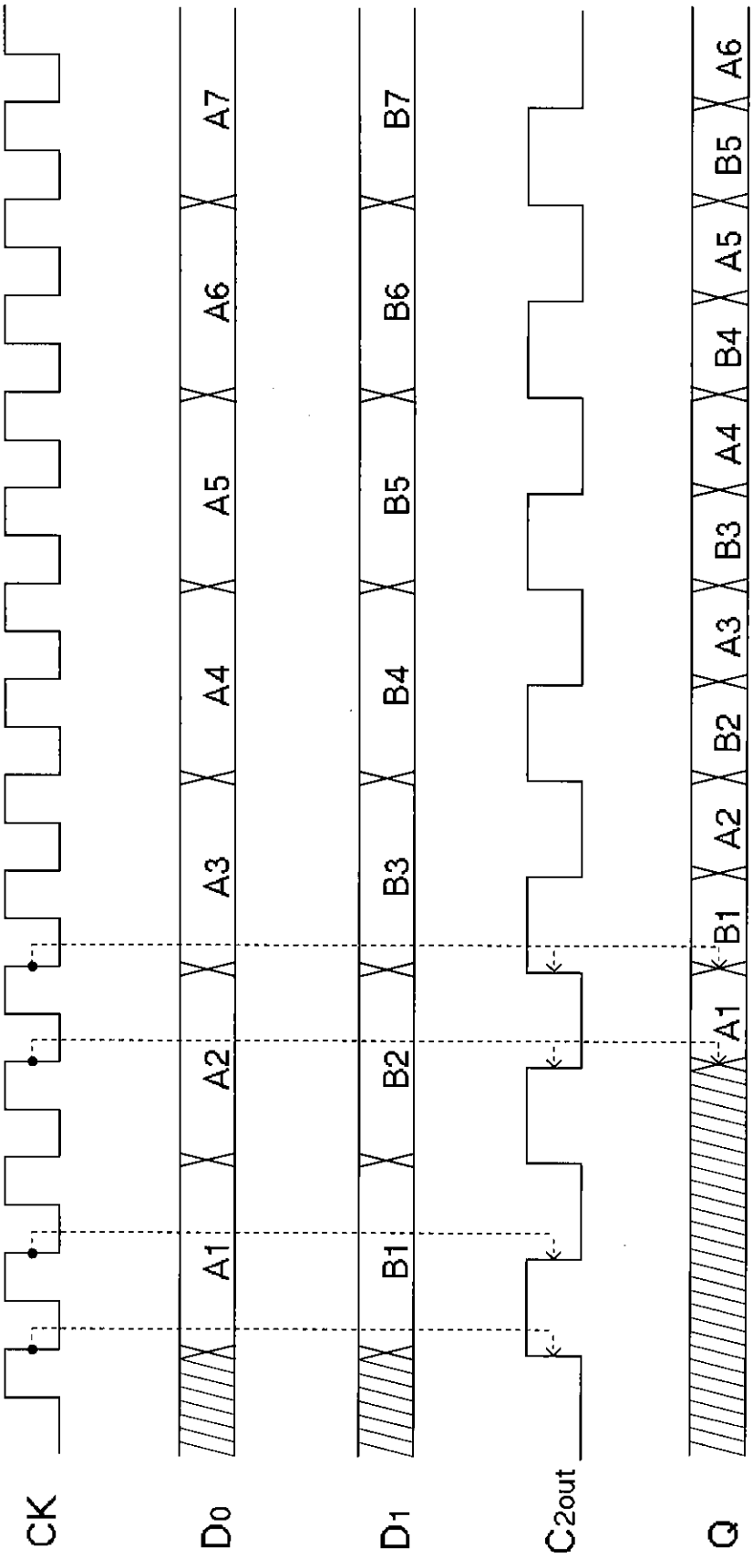
APPLICATIONS

- 2:1 Multiplexer
- Basic circuit for multi-bit multiplexer

FUNCTIONAL DIAGRAM



TIMING CHART



PIN CONNECTION TABLE

PIN No.	NAME	FUNCTION	PIN No.	NAME	FUNCTION
1	Vref0	Data Input Ref. (1)	15	N.C.	No Internal Connection
2	GND	Ground (0.0V)	16	GND	Ground (0.0V)
3	C2out	1/2 Clock Output (True)	17	Q	Data Output (True)
4	GND	Ground (0.0V)	18	GND	Ground (0.0V)
5	$\overline{C2out}$	1/2 Clock Output (Comp.)	19	$\overline{Q}$	Data Output (Comp.)
6	GND	Ground (0.0V)	20	GND	Ground (0.0V)
7	Vcsout	Output Swing Adjust (2)	21	N.C.	No Internal Connection
8	Vss	Power Supply (-3.5V)	22	Vss	Power Supply (-3.5V)
9	GND	Ground (0.0V)	23	GND	Ground (0.0V)
10	CK	Clock Input	24	D0	Data input 0
11	GND	Ground (0.0V)	25	GND	Ground (0.0V)
12	Vref1	Clock Input Ref. (1)	26	D1	Data Input 1
13	GND	Ground (0.0V)	27	GND	Ground (0.0V)
14	Vss	Power Supply (-3.5V)	28	Vss	Power Supply (-3.5V)

Notes

(1) Vref0,Vref1 : Internally generated reference voltage that determines the signal input threshold level. By applying - 0.75 V to - 0.2 V externally to this pin, an arbitrary signal input threshold voltage can be established.

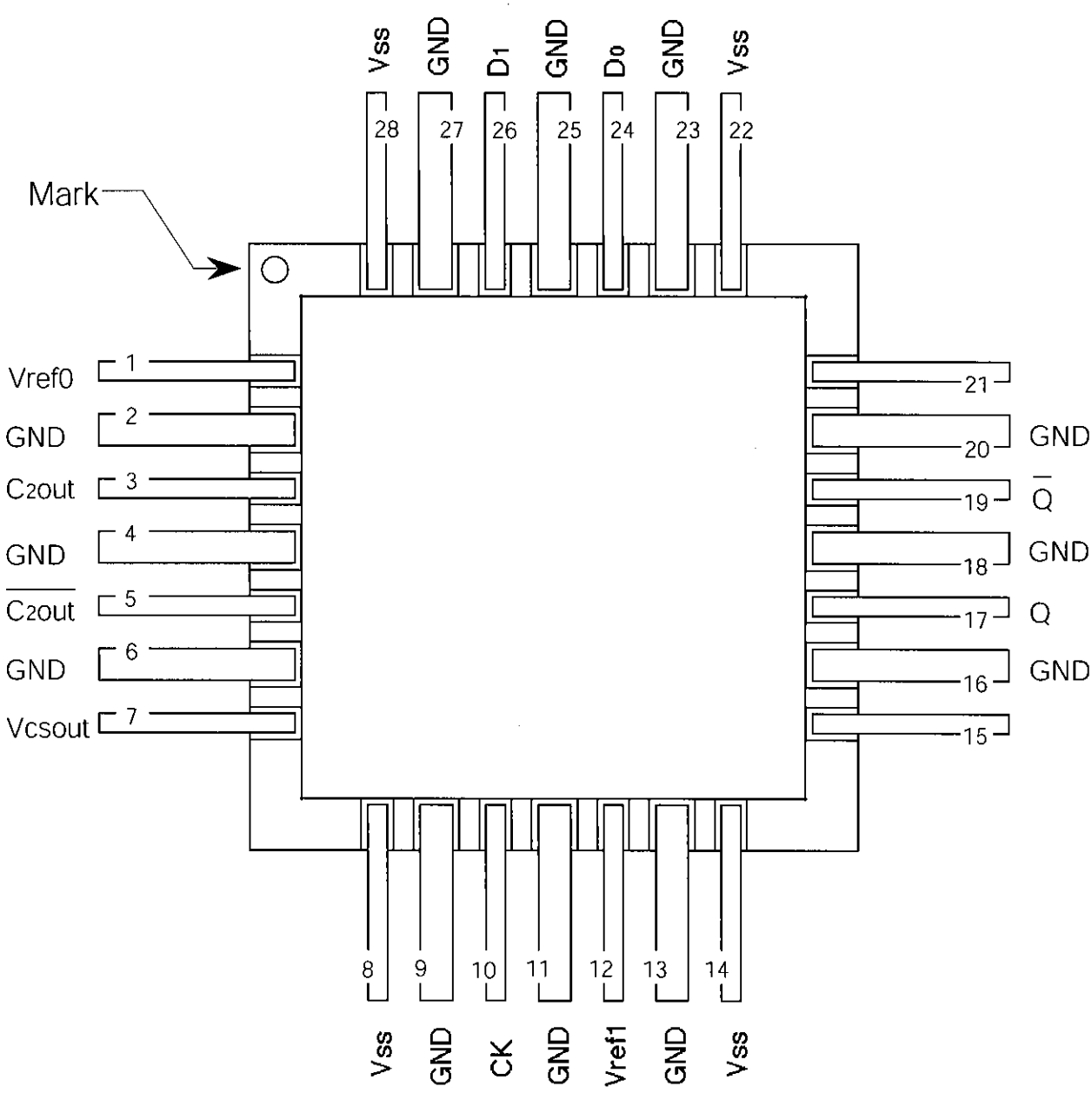
(2) Vcsout : Output swing adjustment pin. Generally left unconnected. To decrease the output swing, connect a resistor between Vcsout pin and Vss pin as shown in sample implementation (See page 12). Output swing can not be increased.

ATTENTION

Please pay attention not to touch the Vcsout pin to the GND or the other pins while applying the Vss voltage, otherwise the IC would be damaged.

(3) Terminate unused output pins in 50 ohm.

CONNECTION DIAGRAM (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
V_{SS}	Power Supply Voltage	0.0 V ~ - 4.0 V
V_{IN}	Applied Voltage at Signal Inputs (D_0, D_1, CK)	+ 0.3 V ~ - 1.6 V
Vout	Applied Voltage at Signal Outputs (Q, $\overline{Q}$, $C2_{out}$, $\overline{C2_{out}}$)	+ 0.2 V ~ - 1.75 V
Vcsout	Applied Voltage at V_{csout} pin	Open Circuit Voltage ~ V_{SS}
Vref0, Vref1	Applied Voltage at V_{ref0} and V_{ref1} pin	+ 0.3 V ~ - 1.6 V
Tstor	Storage Temperature	- 60 ℃ ~ + 150 ℃
Tc (1)	Case Temperature under Bias	- 60 ℃ ~ + 125 ℃

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_{SS}	Power Supply	- 3.4	- 3.5	- 3.75	V
Vref0	Data Input Reference	- 0.2	- 0.5	- 0.75	V
Vref1	Clock Input Reference	- 0.2	- 0.5	- 0.75	V
Vcsout	Output Swing Adjust	Normally Open			V

DC CHARACTERISTICS

(V_{SS}=- 3.4 V ~ - 3.75 V. GND = 0.0 V. T_c = 0 ~ 85 ℃ (1))

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
V_{OH}	Output Voltage, High	- 0.1	0.0		V	
V_{OL}	Output Voltage, Low		- 0.9	- 0.85	V	
V_{IH}	Input Voltage, High	- 0.2	0.0		V	
V_{IL}	Input Voltage, Low		- 0.9	- 0.75	V	
I_{SS}	Power Supply Current		650	910	mA	(2)
Pd	Power Dissipation		2.3	3.4	W	(2)

Notes

(1) T_c : Temperature at package base.

(2) : Includes load current. Excludes current through input termination resistors, all of which have a value of 50 - ohms.

AC CHARACTERISTICS

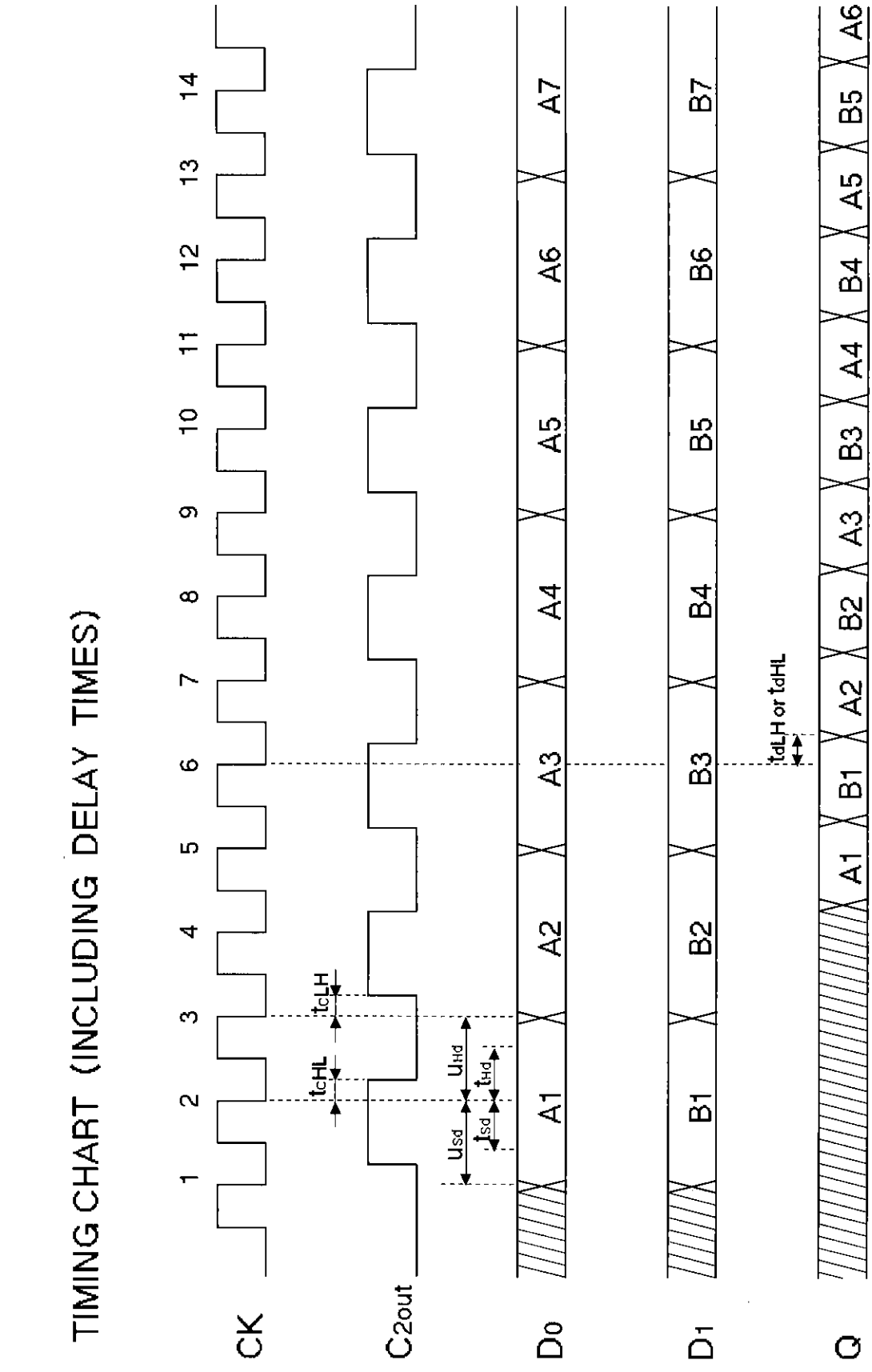
(Vss = - 3.5 V, GND = 0.0 V, Vref0 = - 0.2 ~ - 0.75 V, Vref1 = - 0.2 ~ - 0.75V)

SYMBOL	PARAMETER	Tc=0℃			Tc=25℃			Tc=85℃			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
f_{MIN}	Minimum Clock Frequency		8.1	9.5		8.0	9.4		7.7	9.1	GHz
f_{MAX}	Maximum Clock Frequency	11.2	11.7		10.8	11.3		10.3	10.8		GHz
tr $(Q,\overline{Q})$	Output Rise Time (20-80%)		35	50		35	50		40	55	ps
tf $(Q,\overline{Q})$	Output Fall Time (20-80%)		25	40		30	45		35	50	ps
tr $(C_{2out}, \overline{C_{2out}})$	Output Rise Time (20-80%)		40	60		45	65		50	70	ps
tf $(C_{2out}, \overline{C_{2out}})$	Output Fall Time (20-80%)		35	55		35	55		40	60	ps
t_{dLH}	Output Rise Delay (CK-Q,$\overline{Q}$)	210	245	280	210	245	280	215	250	285	ps
t_{dHL}	Output Fall Delay (CK-Q,$\overline{Q}$)	215	250	285	215	250	285	220	255	290	ps
t_{cLH}	Output Rise Delay (CK-C2out,$\overline{C2out}$)	200	235	270	200	235	270	205	240	275	ps
t_{cHL}	Output Fall Delay (CK-C2out,$\overline{C2out}$)	200	235	270	200	235	270	205	240	275	ps
tsd	Minimum Setup Time ($Dn^{(1)}$- CK)		-90	-50		-90	-50		-95	-55	ps
tHd	Minimum Hold Time (CK- $Dn^{(1)}$)		115	175		115	175		125	185	ps

Note

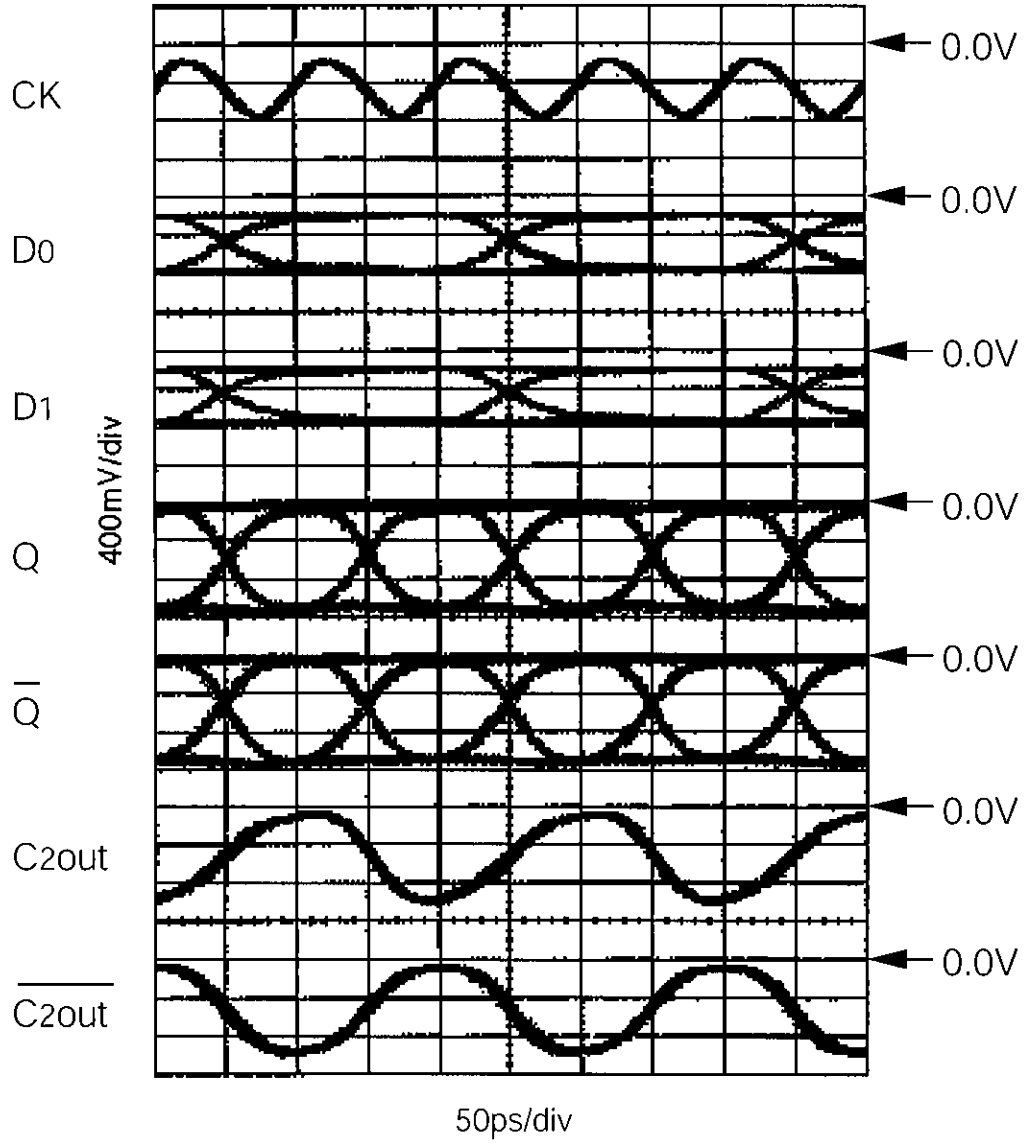
(1) Dn : n = 0, 1

TIMING CHART (INCLUDING DELAY TIMES)



(In the figure above, tSd and tHd are the minimum setup and hold times as defined on the previous page; USd and UHd are the corresponding user setup and hold times.)

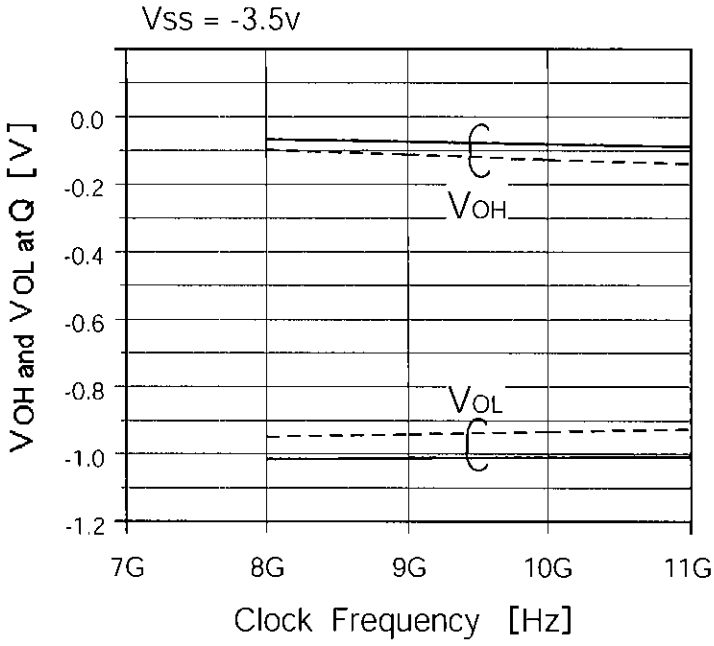
INPUT AND OUTPUT WAVEFORMS AT 10 Gb/s



Measurement Conditions

Vss = - 3.5 V, Vref0 = - 0.50 V, Vref1 = - 0.50 V, Vcsout : Open .
D0 : 5 Gb/s pseudo-random pattern having a word length of 2^{23} -1 bits .
D1 : 5 Gb/s pseudo-random pattern having a word length of 2^{23} -1 bits .
CK : 10 GHz signal .
Signal outputs connected to the 50-ohm impedance pin of a sampling oscilloscope .
Results given here were obtained using the NEL test fixture.

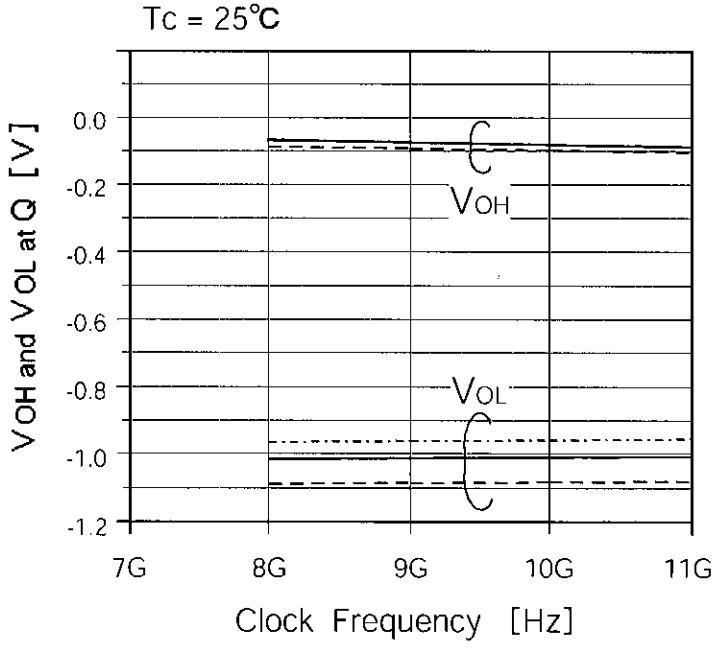
SAMPLE AC CHARACTERISTICS



-·-·-·- : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - : Tc = 85 ℃

Measurement Conditions

D0 = - 0.75 V
D1 = - 0.2 V
CK : VIH = - 0.2 V
and VIL = - 0.75 V
Vref0 : Open
Vref1 : Open
Vcsout : Open
Results given here were obtained using the NEL test fixture.

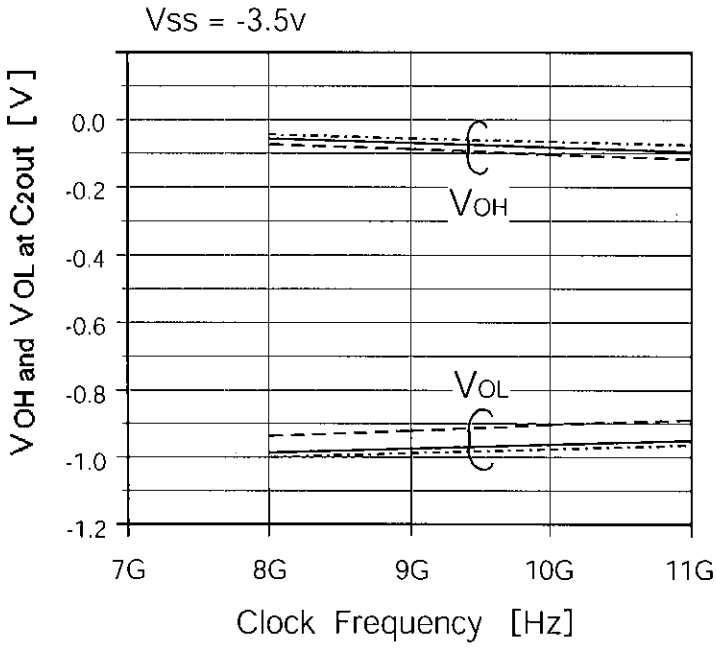


-·-·-·- : Vss = - 3.4 V
——— : Vss = - 3.5 V
- - - - - : Vss = - 3.75 V

Measurement Conditions

D0 = - 0.75 V
D1 = - 0.2 V
CK : VIH = - 0.2 V
and VIL = - 0.75 V
Vref0 : Open
Vref1 : Open
Vcsout : Open
Results given here were obtained using the NEL test fixture.

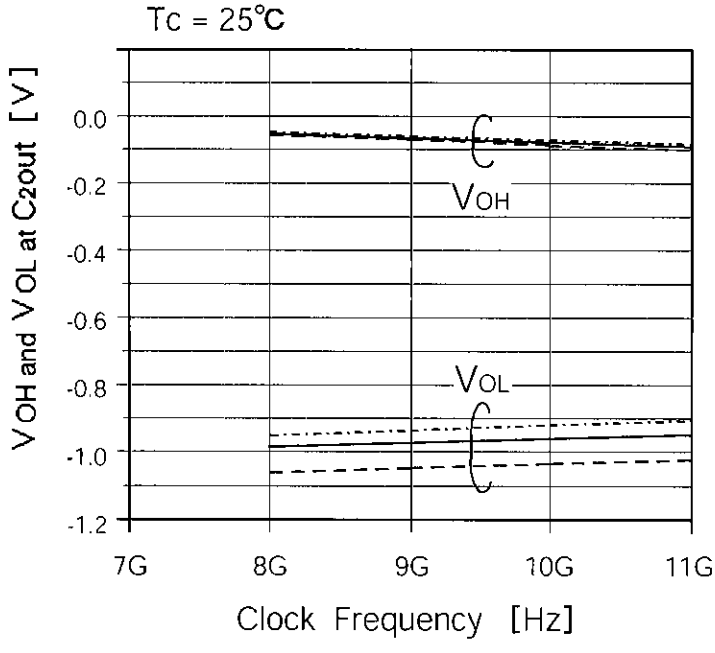
SAMPLE AC CHARACTERISTICS



-·-·-·- : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 85 ℃

Measurement Conditions

D0 = - 0.75 V
D1 = - 0.2 V
CK : VIH = - 0.2 V
and VIL = - 0.75 V
Vref0 : Open
Vref1 : Open
Vcsout : Open
Results given here were obtained using the NEL test fixture.

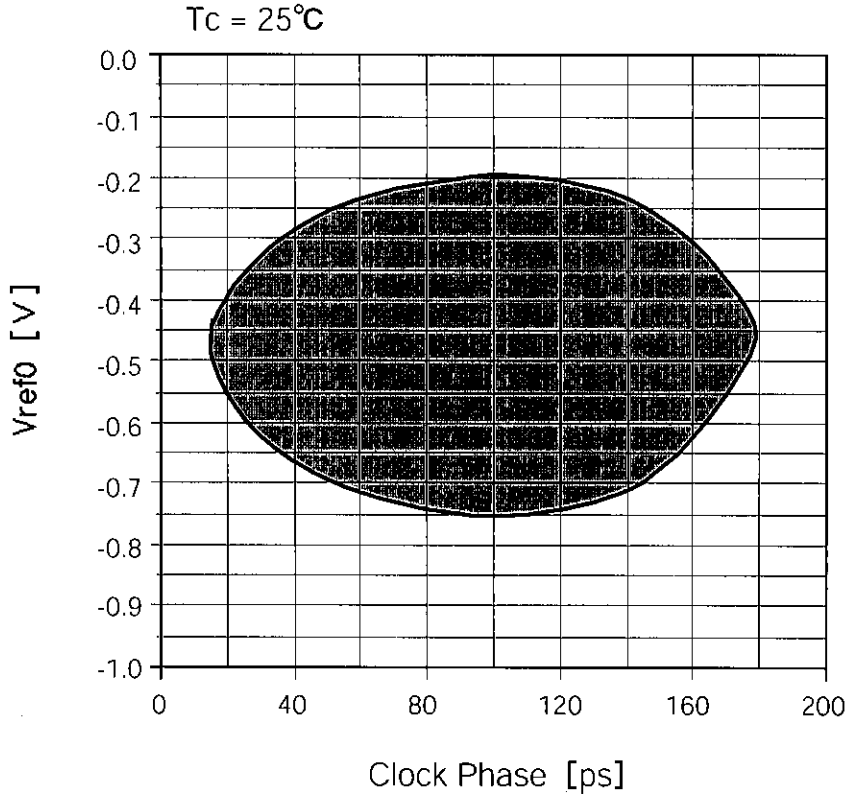


-·-·-·- : Vss = - 3.4 V
——— : Vss = - 3.5 V
- - - - - - : Vss = - 3.75 V

Measurement Conditions

D0 = - 0.75 V
D1 = - 0.2 V
CK : VIH = - 0.2 V
and VIL = - 0.75 V
Vref0 : Open
Vref1 : Open
Vcsout : Open
Results given here were obtained using the NEL test fixture.

SAMPLE INPUT DECISION MARGIN



: error-free operation area

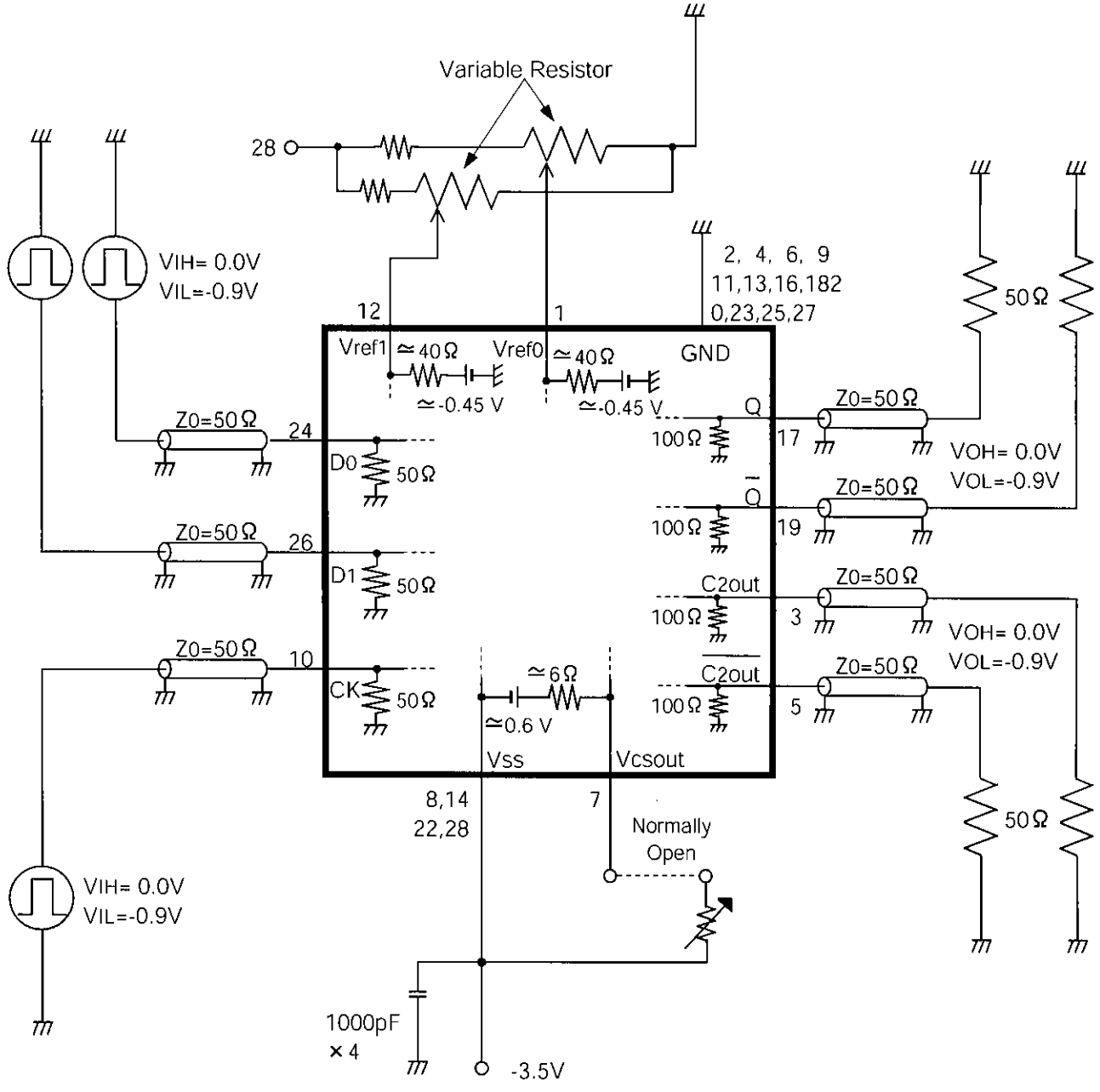
Measurement Conditions

D0, D1 : 5 Gb/s a pseudo-random pattern having a word length of 2^{23}-1 bits.
V_{IH} = -0.1 V, V_{IL} = -0.85 V
CK : 10 GHz V_{IH} = -0.1 V, V_{IL} = -0.85 V
Vss = - 3.50 V
Vref1 = - 0.57 V
Vcsout : Open
$\overline{Q}$: connected to an error detector (less than 1.0×10^{-9}).
Q : terminated in 50 ohm.

Result given here were obtained using the NEL test fixture.

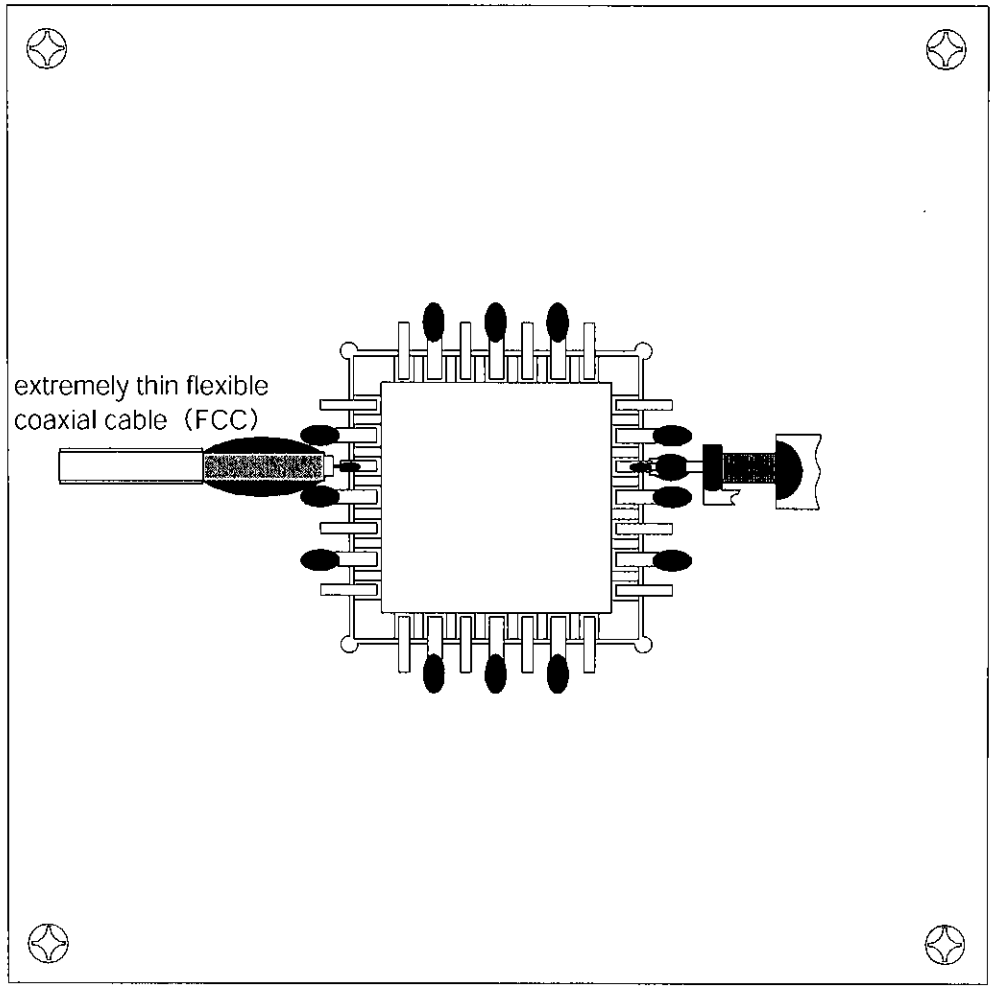
SAMPLE IMPLEMENTATION

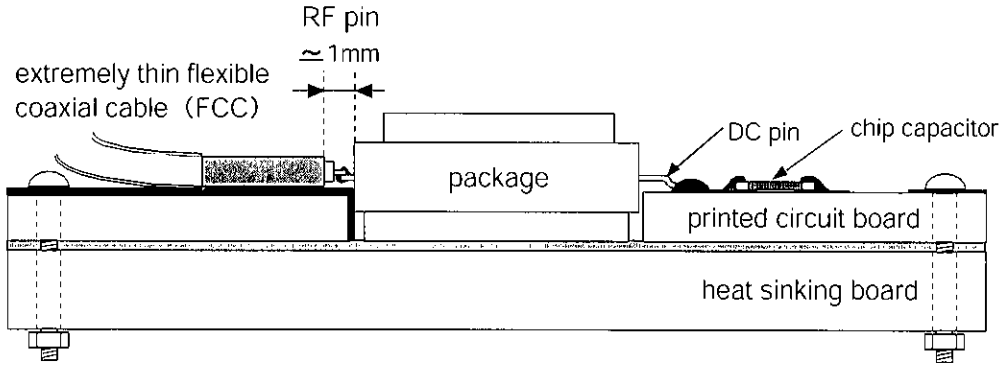
Note : Numbers represent pin numbers



Although not shown here, in place of the above variable resistor, the Vref0 and Vref1 pins can be connected directly to an external power supply. In this case, apply approximately - 0.5 V.

SAMPLE MOUNTING





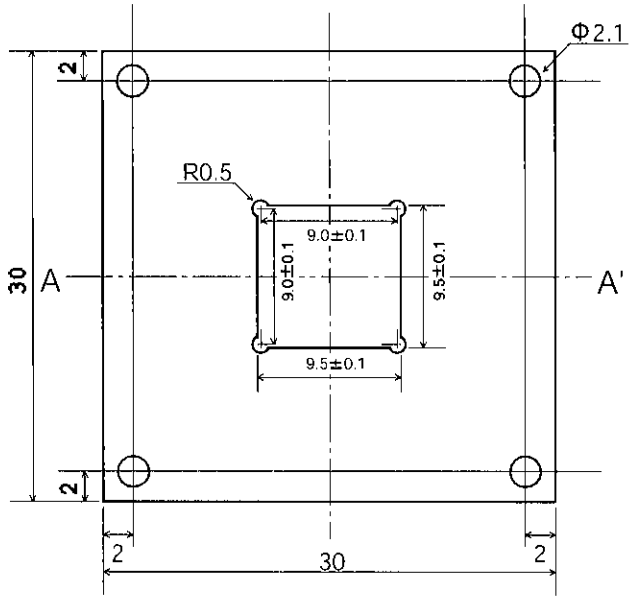
: conducting epoxy adhesive

: solder

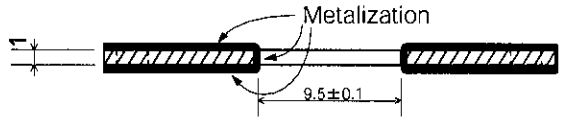
MOUNTING PARTS (unit : mm)

Printed Circuited Board

top view



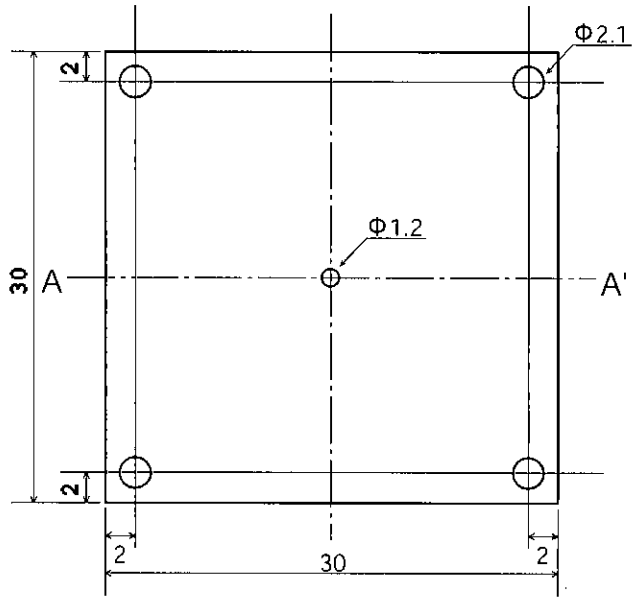
A-A' cross-sectional view



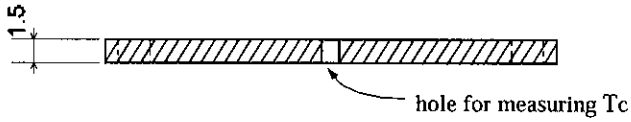
material : glass epoxy base coated
on both sides with a layer of metal and solder
(copper foil thickness : 18 μ m
solder thickness : 40～70 μ m)

Heat Sinking Board

top view



A-A' cross-sectional view



material : aluminum board

Solder

Sn : 60%, Φ0.6mm
(melting point : 190℃)

Conducting epoxy adhesive

Sumitomo bakelite CRM-1061

Screws for attaching the printed circuit board to the heat sinking board

4 M2×8, cross-type small screws

Nuts

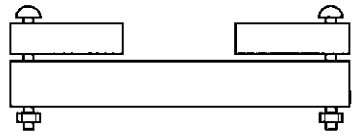
4 M2 hex nuts

Spring washers

4 M2 spring washers

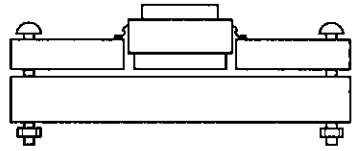
MOUNTING PROCEDURE

①



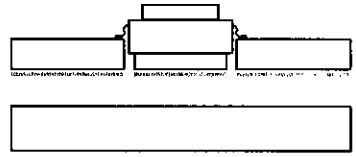
Temporarily fasten the printed circuit board to the heat sinking board with the screws.

②



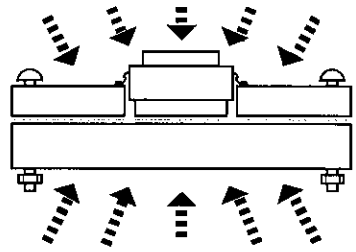
Insert the IC package into the center part of the printed circuit board. Solder the GND pins to the printed circuit board.

③



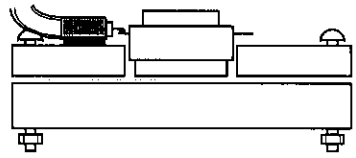
Unfasten the printed circuit board from the heat sinking board. Thinly paint the entire bottom surfaces of the printed circuit board and the IC with the conducting epoxy adhesive. Make sure that silver paste is not applied to the region between the printed circuited board and the IC.

④



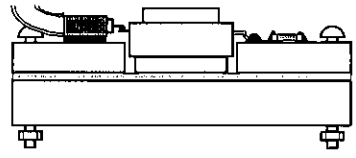
Again fasten the printed circuit board to the heat sinking board with the screws. Bake the fixture in an oven for 60 minutes at 150℃ (120℃～170℃) .

⑤



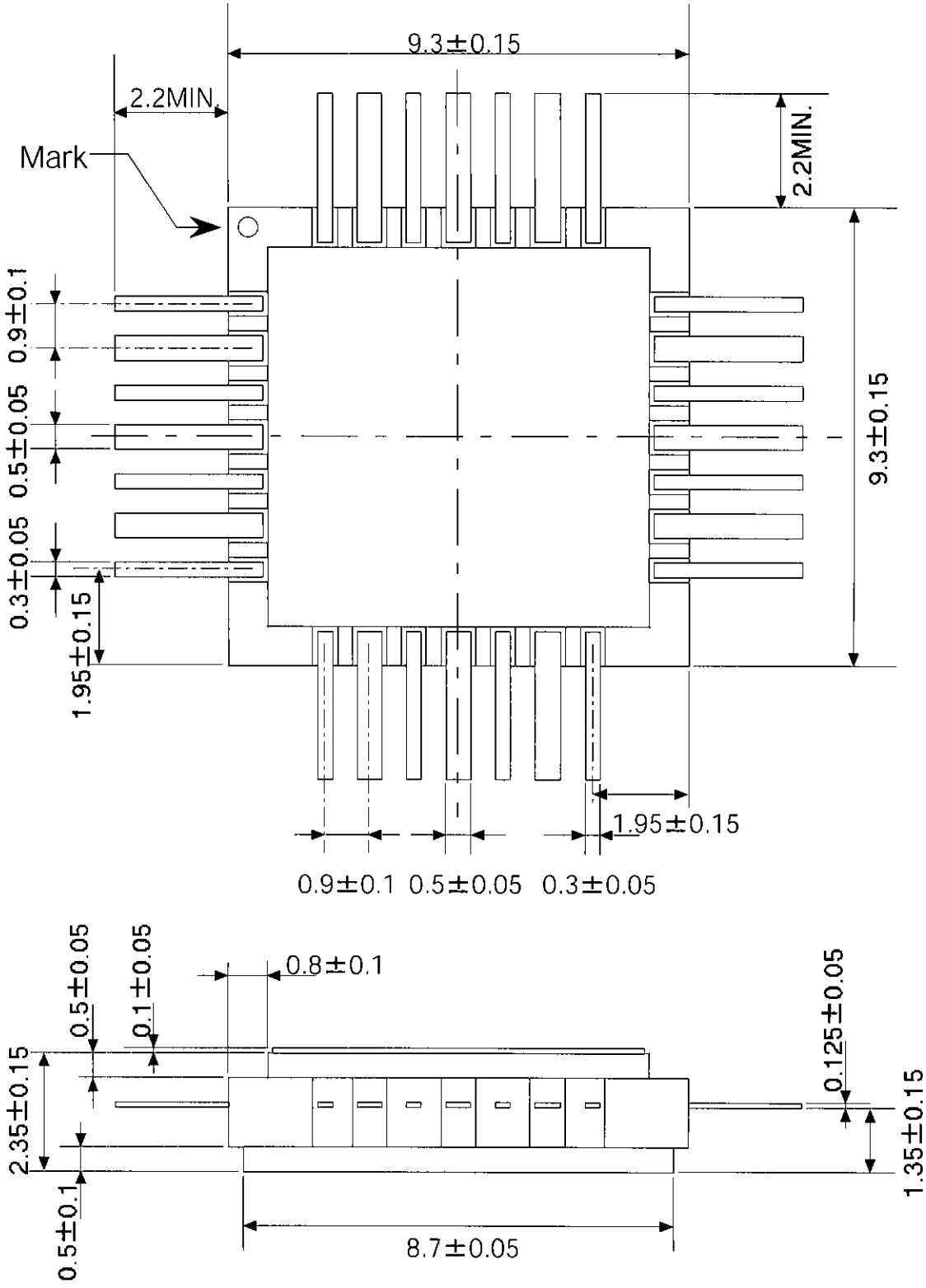
Take the fixture out of the oven. After the IC has cooled, solder the FCC to the input/output pins.

⑥



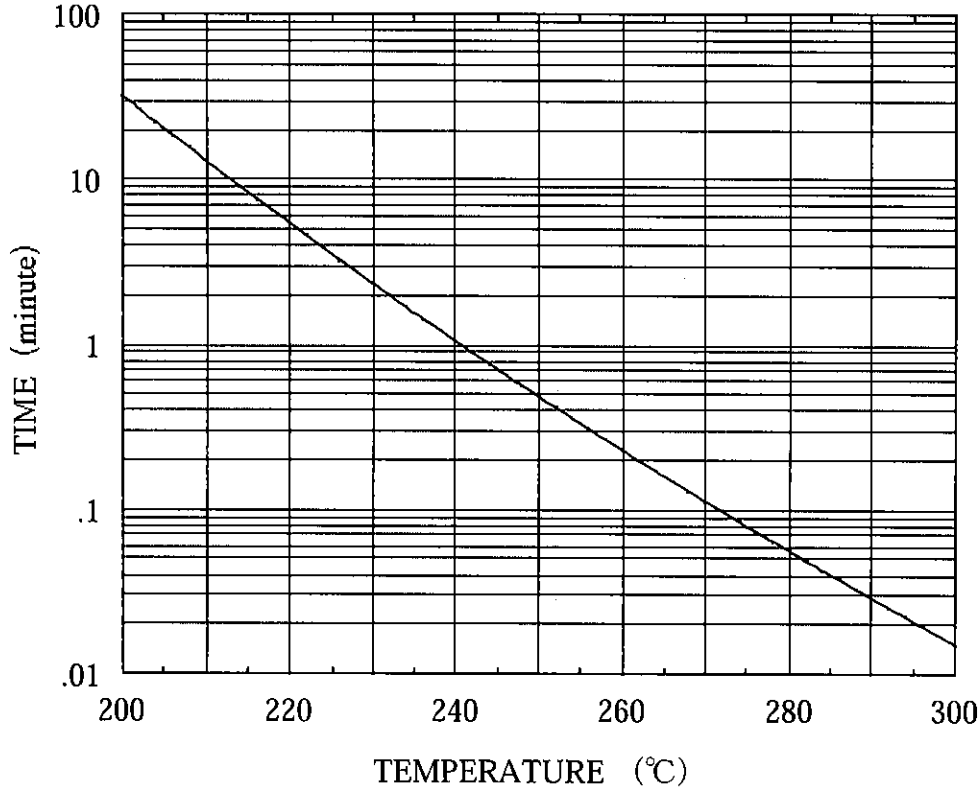
As the final step, solder the chip capacitors, chip resistors, etc., to the DC pins.

TB 28 - PIN PACKAGE DIMENSION (mm)



MAXIMUM TEMPERATURE AND TIME UNDER ASSEMBLING PROCESS

In assembling process, following maximum limited temperature and time condition should be kept.



Maximum limited time vs. temperature

OPERATING AND HANDLING INSTRUCTIONS

Since the NEL ICs are fabricated with GaAs MESFET's (MEtal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro - statics discharge.

(1) Power Supply Sequence

The following power supply sequence is recommended.

1) Set supply voltage Vss, Vref0, Vref1 and GND to 0V.

2) Apply Vref0.

3) Apply Vref1.

4) Apply Vss.

RF signals are recommended to be applied while power supplying and biasing.

(2) Handling precautions

1) Use a conductive working desk connected to ground (or, a conductive table top connected to ground).

2) Require all handling personnel to wear a conductive bracelet or wrist - strap connected to ground though a 1 M - ohm resistor.

3) Ground all test equipment.

4) Ground all soldering iron tips.

5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.