

NLG4023

25 Gb/s 2 : 1 SELECTOR

The NLG4023 is an ultra-fast 2 : 1 SELECTOR operating at up to 23 Gb/s.

Designed with LSCFL (Low-power Source Coupled FET Logic), it uses SCFL I/O levels ($V_H : 0.0\text{ V}$, $V_L : -0.9\text{ V}$).

Either AC or DC coupling can be used for the select signal input.

Owing to built-in 50-ohm termination resistors between signal input pins and ground (GND), external termination resistors are unnecessary for impedance matching.

The NLG4023 is fabricated using the 0.15- μm gate length A-SAINT (Advanced Self-Aligned Implantation for N^+ layer Technology) process.

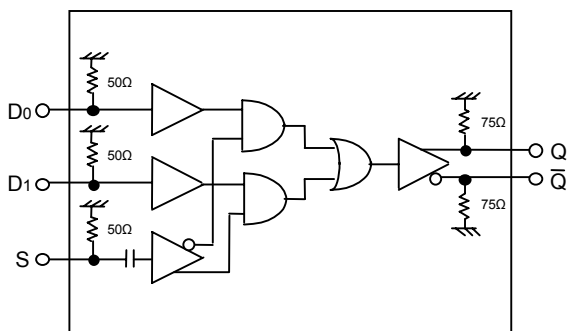
FEATURES

Ultra-high speed : maximum select signal frequency	f_{MAX}	: 12.5 GHz
minimum select signal frequency	f_{MIN}	: 2 GHz
output rise time	t_r	= 20 ps (20 – 80%)
output fall time	t_f	= 20 ps (20 – 80%)
High Reliability : hermetically-sealed package		

APPLICATION

- 2-1 Multiplexer
- Basic circuit for multi-bit multiplexer

FUNCTION DIAGRAM



TRUTH TABLE

D0	D1	S	Q	$\bar{Q}$
L	X	L	L	H
H	X	L	H	L
X	L	H	L	H
X	H	H	H	L

Note
X : Arbitrary

PIN CONNECTION TABLE

No.	NAME	FUNCTION	No.	NAME	FUNCTION
1	D0	Signal Input 0	15	GND	Ground (0.0 V)
2	GND	Ground (0.0 V)	16	GND	Ground (0.0 V)
3	Vrefs	S Input Ref. ⁽¹⁾	17	$\overline{Q}$	Signal Output (Comp.)
4	GND	Ground (0.0 V)	18	GND	Ground (0.0 V)
5	S	Select Signal Input	19	Q	Signal Output (True)
6	GND	Ground (0.0 V)	20	GND	Ground (0.0 V)
7	D1	Signal Input 1	21	GND	Ground (0.0 V)
8	VSS	Power Supply (-4.5 V)	22	VSS	Power Supply (-4.5 V)
9	GND	Ground (0.0 V)	23	GND	Ground (0.0 V)
10	Vref1	D1 Input Ref. ⁽²⁾	24	NC	No Internal Connection
11	GND	Ground (0.0 V)	25	GND	Ground (0.0 V)
12	GND	Ground (0.0 V)	26	Vref0	D0 Input Ref. ⁽³⁾
13	GND	Ground (0.0 V)	27	GND	Ground (0.0 V)
14	VSS	Power Supply (-4.5 V)	28	VSS	Power Supply (-4.5 V)

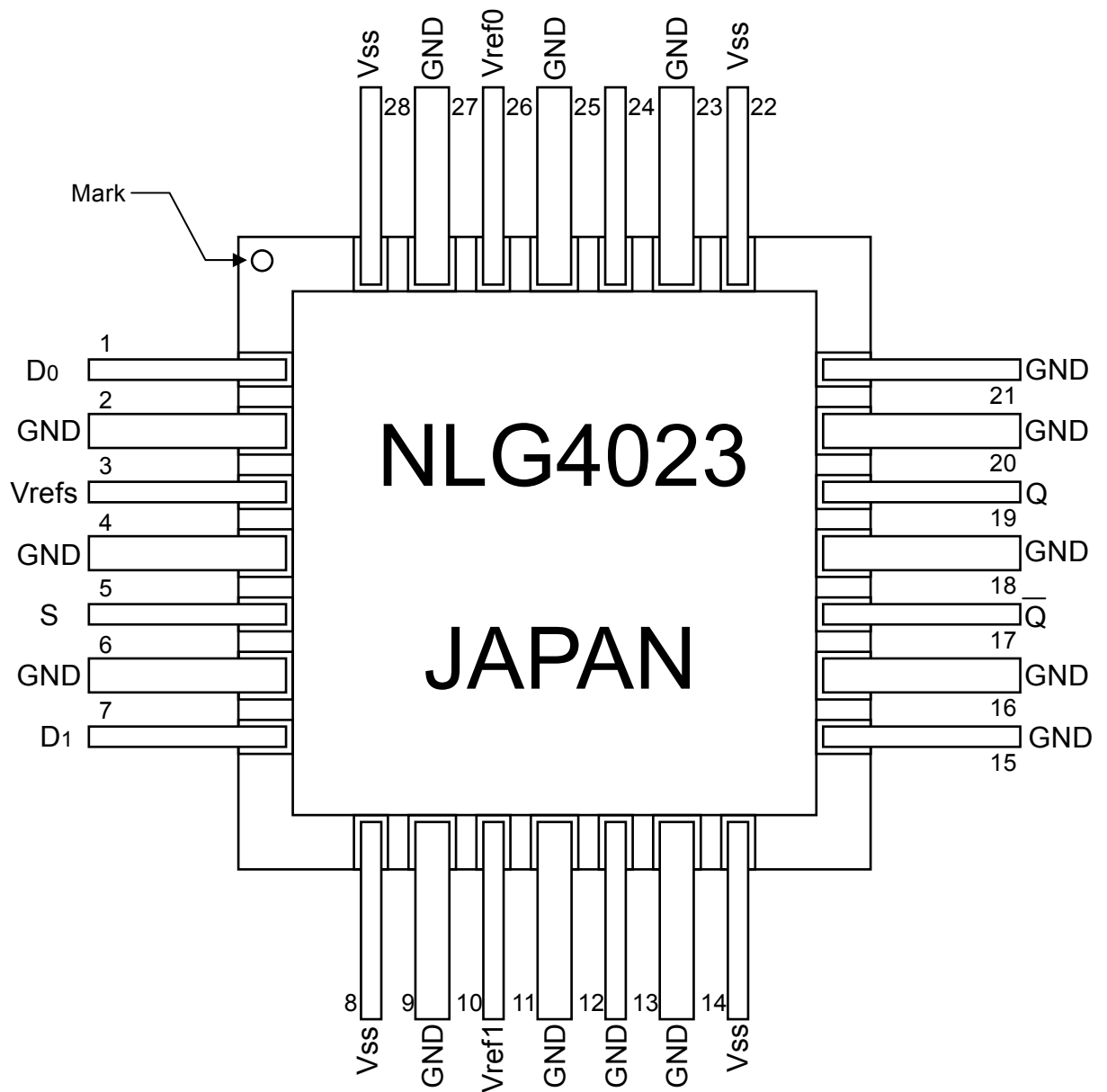
Notes

- (1) Vrefs : Internally generated reference voltage that determines the select signal input threshold level.
- (2) Vref1 : Internally generated reference voltage that determines the signal input 1 threshold level. By applying - 0.75 V to - 0.2 V externally to this pin, an arbitrary signal input 1 threshold voltage can be established.
- (3) Vref0 : Internally generated reference voltage that determines the signal input 0 threshold level. By applying - 0.75 V to - 0.2 V externally to this pin, an arbitrary signal input 0 threshold voltage can be established.
- (4) Terminate unused output pins to GND through 50-ohm resistors.

NEL

CONNECTION DIAGRAM (TOP VIEW)

NLG4023



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
VSS	Power Supply Voltage	+0.5 V ~ - 5.5 V
Vindin	Applied Voltage at Signal Inputs (D0 , D1)	+0.3 V ~ -1.6 V
Vin	Applied Voltage Amplitude at Select Signal Input (S)	1.6 Vp-p
Vins	Applied Voltage at Select Signal Input (S)	+ 1.6 V ~ - 1.6 V
Vout	Applied Voltage at Signal Outputs (Q, $\bar{Q}$)	+ 0.2 V ~ - 1.75 V
Vrefs	Applied Voltage at Vrefs under Bias	- 1.0 V ~ - 2.5 V
Vref0, Vref1	Applied Voltage at Vref0 and Vref1 pins	+ 0.3 V ~ - 1.6 V
Tstor	Storage Temperature	- 60 °C ~ +150 °C
Tc ⁽¹⁾	Case Temperature under Bias	- 60 °C ~ +125 °C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS
VSS	Power Supply Voltage	- 4.75	- 4.5	- 4.25	V
Vrefs	Select Signal Input Reference Voltage	Normally Open			V
Vref0 Vref1	Signal Input Reference Voltage	Adjust in the range from -0.75 V to -0.20 V			V
Dn	Signal Input Interface (D0, D1)	DC Coupling (See DC Characteristics)			—
S	Select Signal Input Interface (S)	DC Coupling or AC Coupling (See AC Characteristics)			—
OUT	Data Output Interface (Q, $\bar{Q}$)	DC Coupling , Terminate to GND through 50Ω			—

DC CHARACTERISTICS

(VSS = - 4.25 V ~ - 4.75 V, GND = 0.0 V, Tc = 0 ~ 85 °C ⁽¹⁾)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
V _{IH}	Input Voltage, High (D0, D1)	-0.2	0.0		V
V _{IL}	Input Voltage, Low (D0, D1)		- 0.9	-0.75	V
I _{SS}	Power Supply Current		750	990	mA
P _d	Power Dissipation		3.4	4.7	W

(2)

(2)

Note

(1) Tc : temperature at package base.

(2) : Includes load current. Excludes current through input termination resistors, all of which have 50 - ohms.

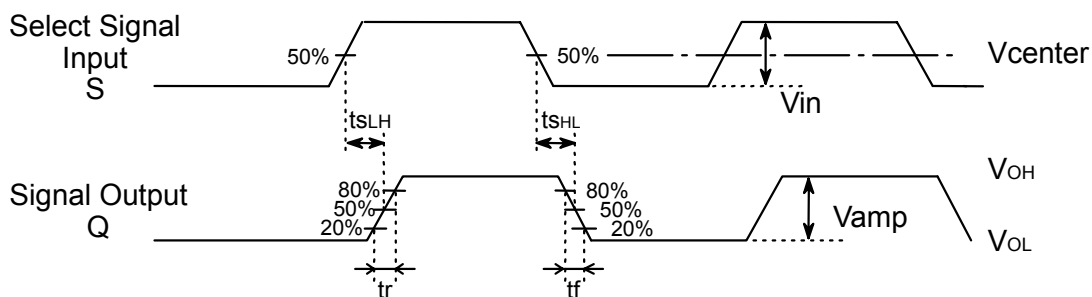
AC CHARACTERISTICS

($V_{SS} = -4.25 \text{ V} \sim -4.75 \text{ V}$, $GND = 0.0 \text{ V}$, V_{ref0} : Adjust in the range from -0.75 V to -0.2 V ,
 V_{ref1} : Adjust in the range from -0.75 V to -0.2 V , V_{refs} : Open, $T_c = 0 \sim 85 \text{ }^{\circ}\text{C}$)

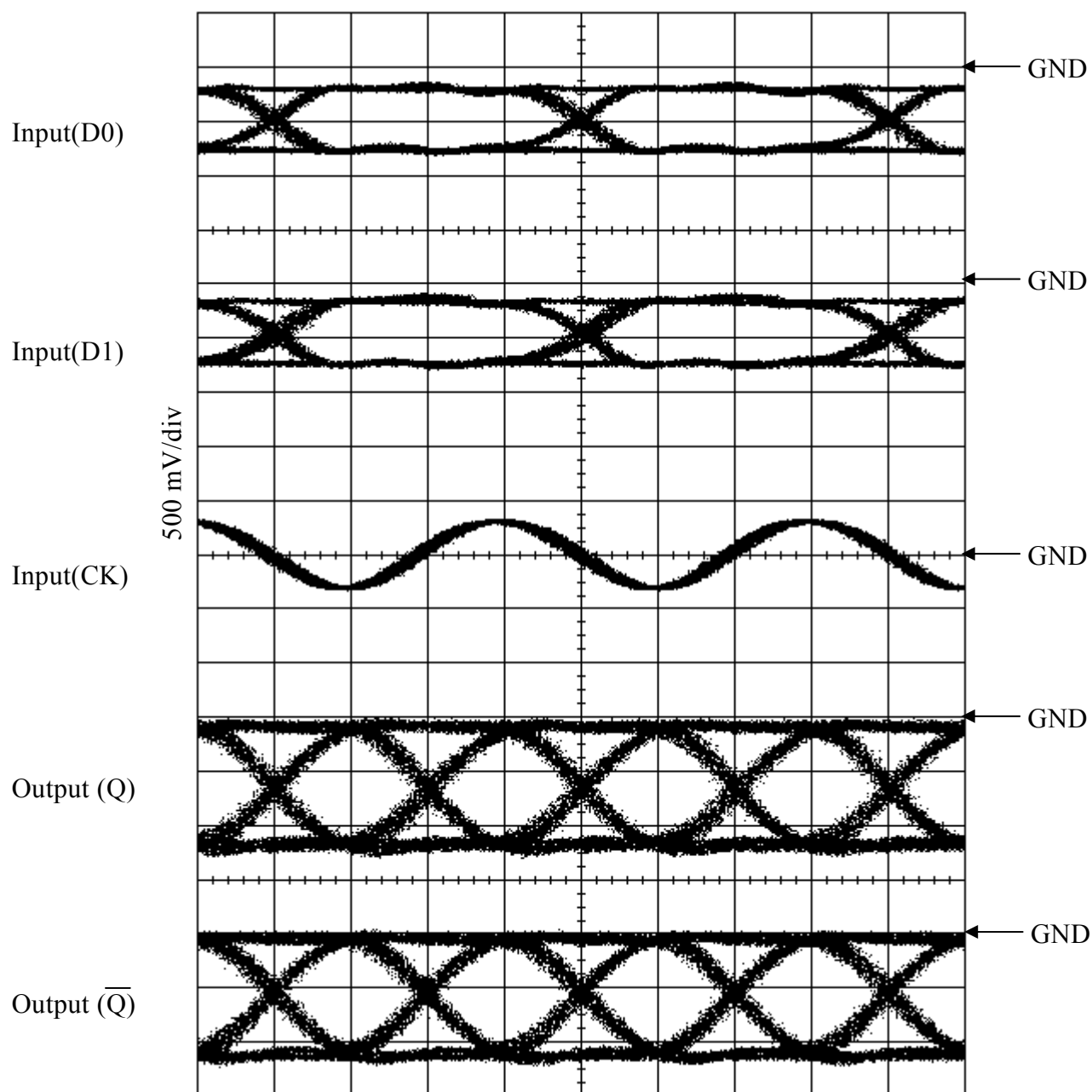
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
V_{in}	Minimum Select Signal Input Voltage Amplitude			0.6	Vp-p	(3)
V_{center}	Select Signal Input Center Voltage	-0.5	0.0	0.5	V	(3)
f_{MAX}	Maximum Select Signal Frequency	11.5	12.5		GHz	(1)
f_{MIN}	Minimum Select Signal Frequency			2.0	GHz	(1)
V_{amp}	Output Voltage Amplitude	0.7	1.0		Vp-p	(2) (3)
V_{OH}	Output Voltage, High (Q , $\bar{Q}$)	-0.2	-0.1		V	(2) (3)
V_{OL}	Output Voltage, Low (Q , $\bar{Q}$)		-1.1	-0.75	V	(2) (3)
t_r	Output Rise Time (Q , $\bar{Q}$)		20	25	ps	(2) (3)
t_f	Output Fall Time (Q , $\bar{Q}$)		20	25	ps	(2) (3)
t_{sLH}	Output Rise Delay (CK- Q , $\bar{Q}$)	170	195	220	ps	(3)
t_{sHL}	Output Fall Delay (CK- Q , $\bar{Q}$)	170	195	220	ps	(3)

Note

- (1) Confirmed by error-free operation using a pseudo-random pattern having a word length of $2^{31}-1$ bits .
- (2) Measurement Condition
: Output Pattern = 23.0 Gb/s pseudo-random pattern having a word length of $2^{31}-1$ bits
- (3)



SAMPLE INPUT AND OUTPUT WAVEFORMS (25 Gb/s)

Measurement Conditions

25 ps/div

Ta = 25 °C

Vss = - 4.5 V

Vref0 = - 0.45 V

Vref1 = - 0.45 V

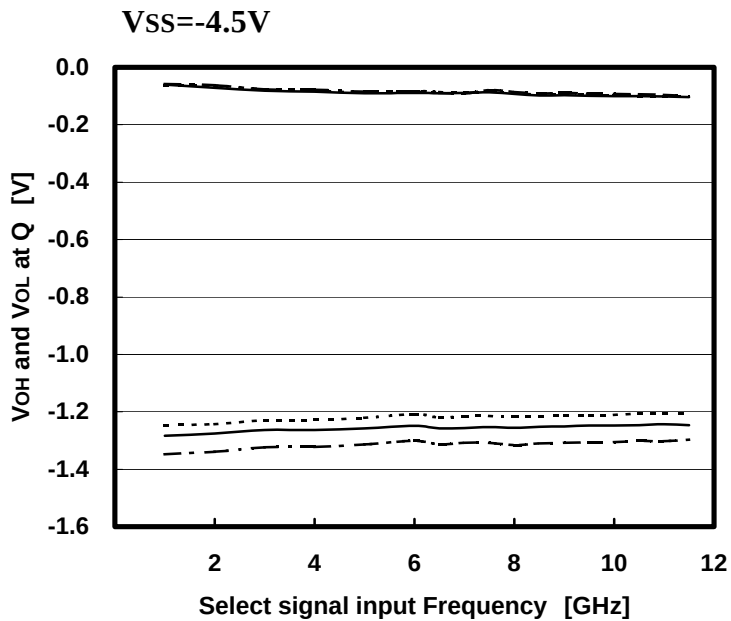
Vrefs : OPEN

D0, D1 : 12.5 Gb/s pseudo-random pattern having a word length of $2^{31}-1$ bits .

S : 12.5 GHz

Data outputs connected to the 50-ohm impedance pins of a sampling oscilloscope .

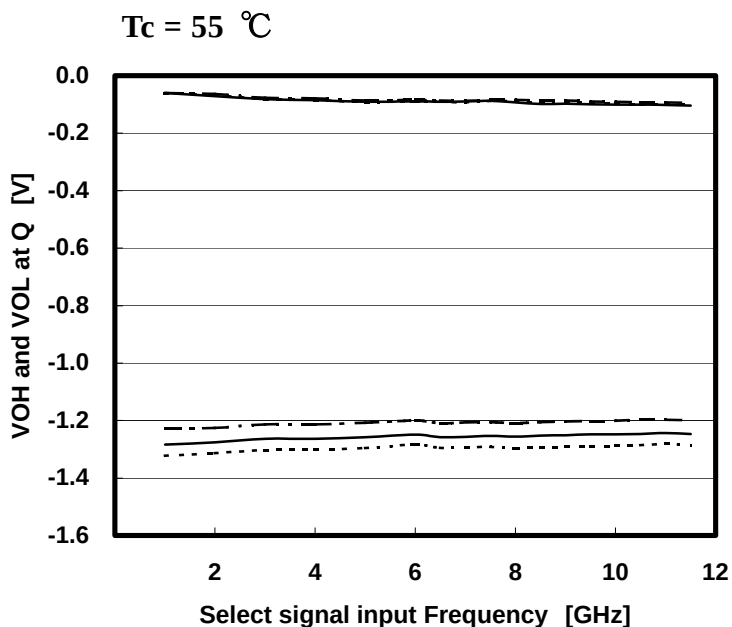
Results given here were obtained using the NEL test fixture.



Measurement Conditions

D0 : PN=31 , MR=1/2 ,
 $V_{IH} = -0.2V$, $V_{IL} = -0.75V$
 D1 : PN=31 , MR=1/2 ,
 $V_{IH} = -0.2V$, $V_{IL} = -0.75V$
 $S = 0.6V_{p-p}$
 $V_{ref0} = -0.5V$
 $V_{ref1} = -0.5V$

Results given here were obtained using the NEL test fixture.

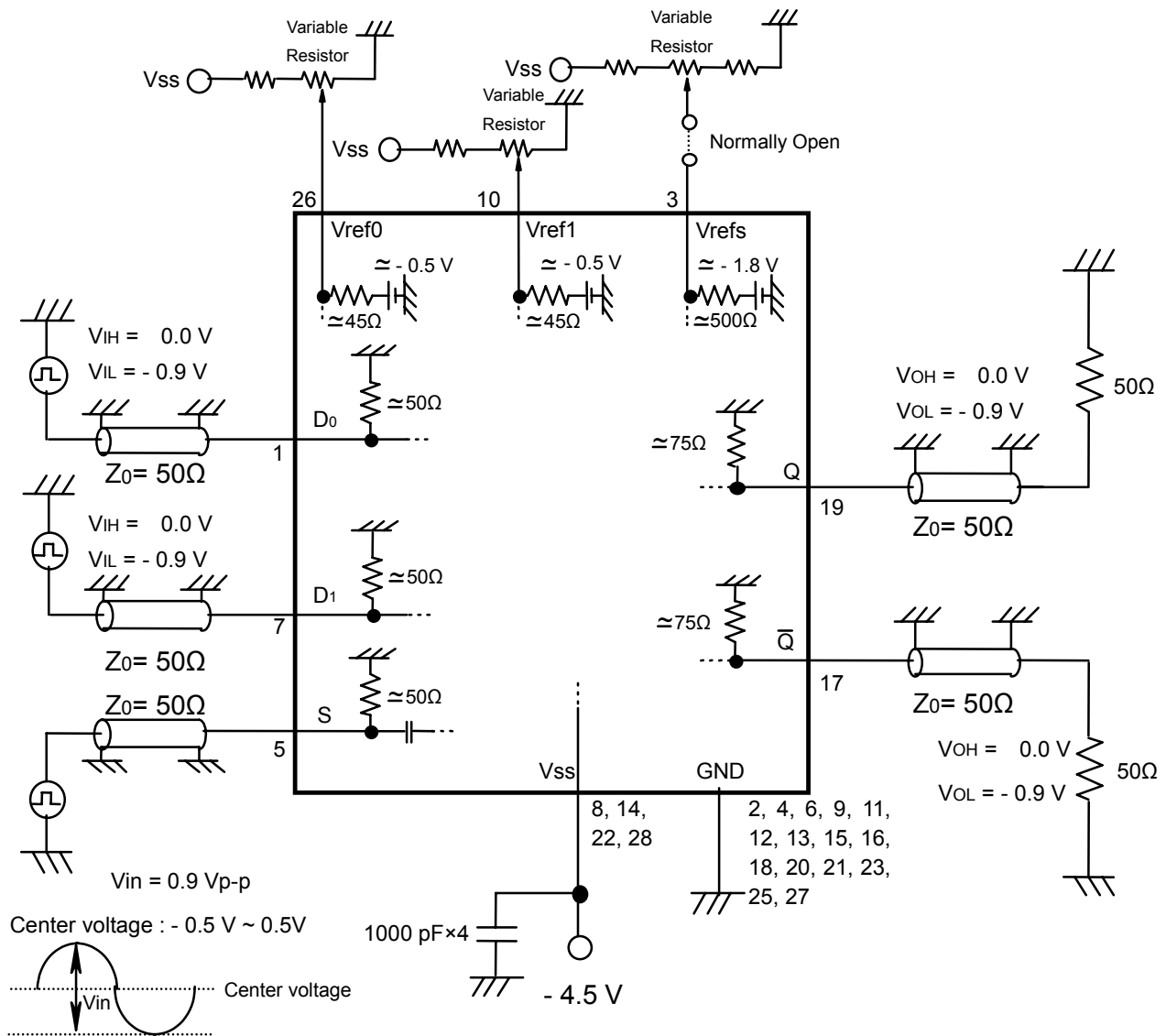


Measurement Conditions

D0 : PN=31 , MR=1/2 ,
 $V_{IH} = -0.2V$, $V_{IL} = -0.75V$
 D1 : PN=31 , MR=1/2 ,
 $V_{IH} = -0.2V$, $V_{IL} = -0.75V$
 $S = 0.6V_{p-p}$
 $V_{ref0} = -0.5V$
 $V_{ref1} = -0.5V$

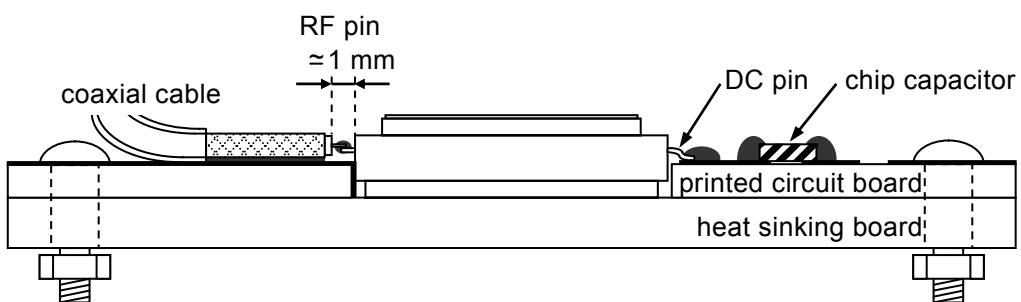
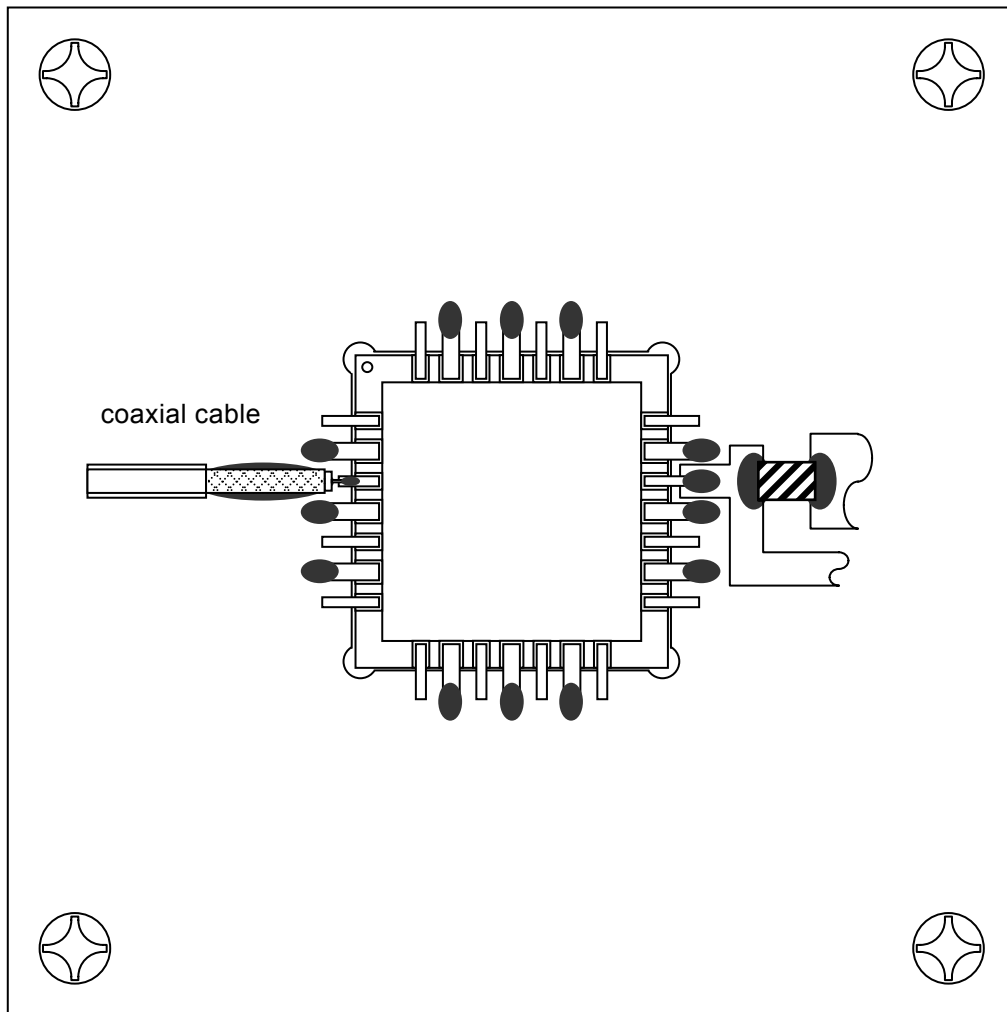
Results given here were obtained using the NEL test fixture.

Note : Numerical figures represent pin numbers



Although not shown here, in place of the above variable resistors, the Vref0, Vref1 and Vrefs pins can be connected directly to an external power supply .

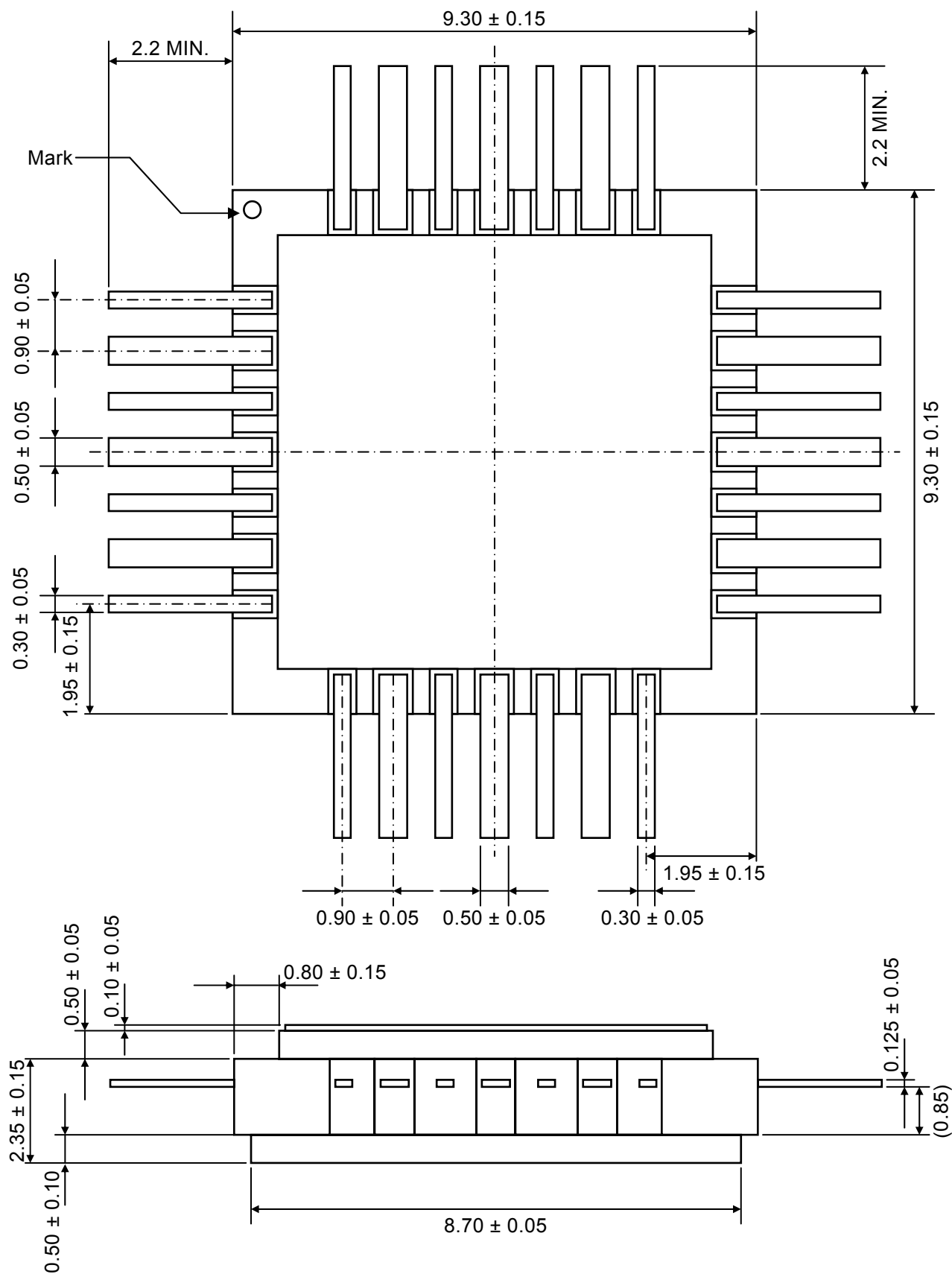
In this case, apply approximately - 0.5 V to the Vref0 and Vref1 pins , and - 1.8 V to the Vrefs pin .



■ : solder

Caution: The package base should be connected to the ground.

TB-28 - PIN PACKAGE DIMENSION (mm)



HANDLING INSTRUCTIONS

Since the NLG4023 is fabricated with GaAs MESFET's (Metal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro-static discharge.

- 1) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
- 2) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M Ω resistor.
- 3) Ground all test equipments.
- 4) Ground all soldering iron tops.
- 5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

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