NEL

NS GG E066
27 Jan. 1999
PRELIMINARY

NLG4001
20 Gb/s 2 - INPUT OR / NOR

The NLG4001 is an ultra-fast 2 input OR / NOR operating at up to 20 Gb/s (MIN.).
Designed with LSCFL (Low-power Source Coupled FET Logic), it uses SCFL I/O levels (V_H : 0.0 V, V_L : - 0.9 V) .
Owing to built-in 50-ohm termination resistors between signal input pins and ground (GND), external termination resistors are unnecessary for impedance matching.
The NLG4001 is fabricated using the 0.15-μm gate length A-SAINT (Advanced Self-Aligned Implantation for N^+ layer Technology) process .

FEATURES

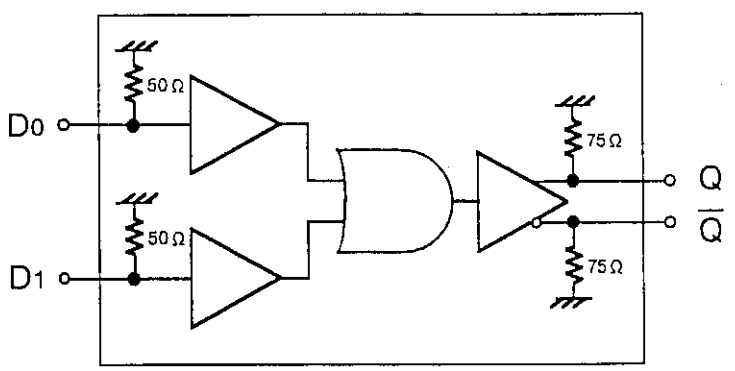
Ultra-high speed :	maximum operating speed	f_{MAX} : 20.0 Gb/s	[Tc = 25 ℃ , MIN.]
	output rise time	tr = 20 ps (20-80%)	[Tc = 25 ℃ , TYP.]
	output fall time	tf = 20 ps (20-80%)	[Tc = 25 ℃ , TYP.]

High Reliability : hermetically-sealed package

APPLICATIONS

- Basic circuit for various logic circuits
- Line Driver
- Line Receiver
- High Speed Comparator
- 2-phase clock generator
- Gating Circuit

FUNCTIONAL DIAGRAM



TRUTH TABLE

D0	D1	Q	$\overline{Q}$
L	L	L	H
L	H	H	L
H	L	H	L
H	H	H	L

PIN CONNECTION TABLE

PIN No.	NAME	FUNCTION	PIN No.	NAME	FUNCTION
1	D_0	Signal Input 0	15	GND	Ground (0.0 V)
2	GND	Ground (0.0 V)	16	GND	Ground (0.0 V)
3	GND	Ground (0.0 V)	17	$\overline{Q}$	Signal Output (Comp.)
4	GND	Ground (0.0 V)	18	GND	Ground (0.0 V)
5	GND	Ground (0.0 V)	19	Q	Signal Output (True)
6	GND	Ground (0.0 V)	20	GND	Ground (0.0 V)
7	D_1	Signal Input 1	21	GND	Ground (0.0 V)
8	Vss	Power Supply (- 4.5 V)	22	Vss	Power Supply (- 4.5 V)
9	GND	Ground (0.0 V)	23	GND	Ground (0.0 V)
10	Vref1	D_1 Input Ref.(1)	24	NC	No Internal Connection
11	GND	Ground (0.0 V)	25	GND	Ground (0.0 V)
12	GND	Ground (0.0 V)	26	Vref0	D_0 Input Ref.(2)
13	GND	Ground (0.0 V)	27	GND	Ground (0.0 V)
14	Vss	Power Supply (- 4.5 V)	28	Vss	Power Supply (- 4.5 V)

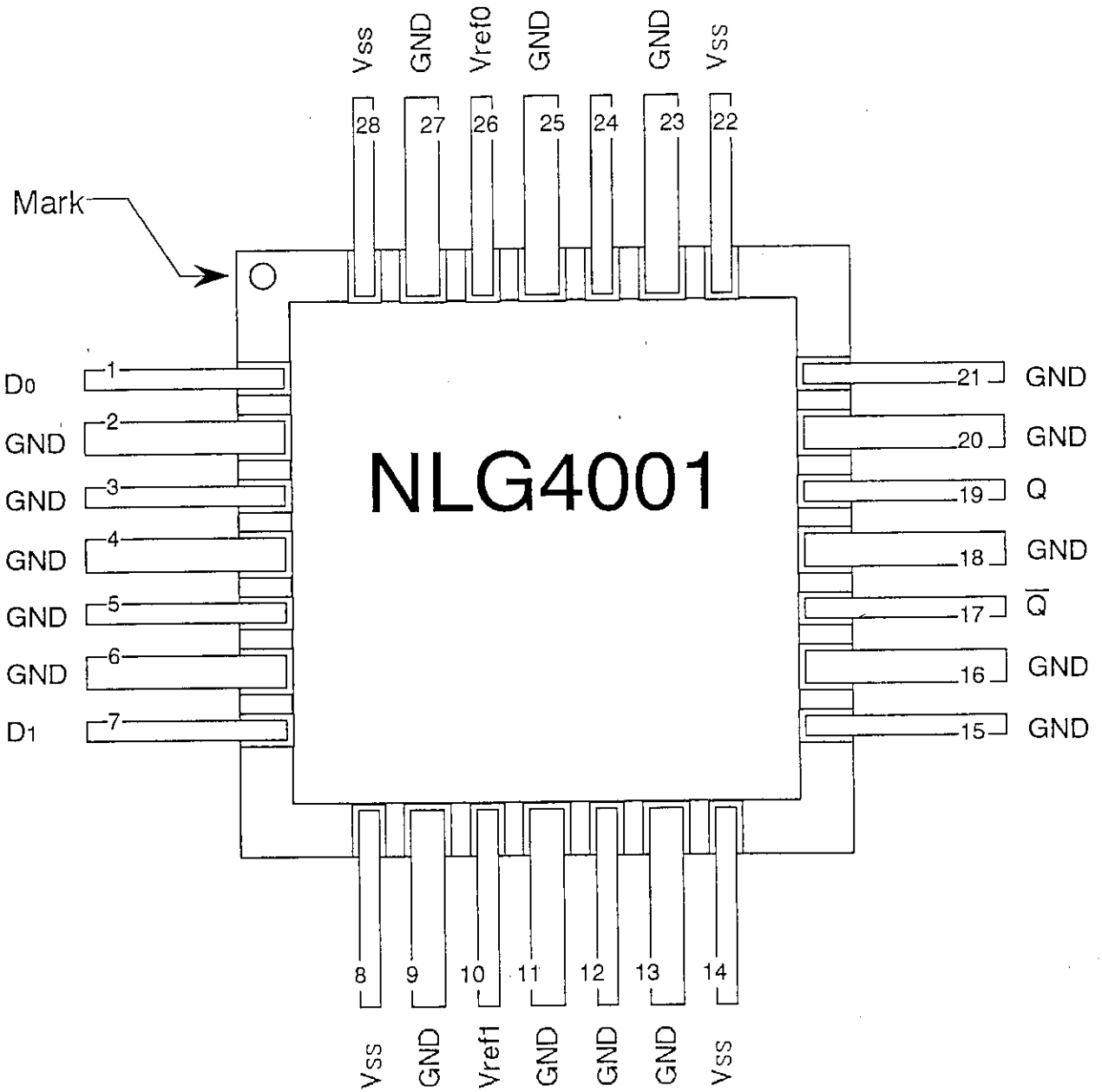
Notes

(1) Vref1 : Internally generated reference voltage that determines the signal input (D_1) threshold level. By applying - 0.75 V to - 0.2 V externally to this pin, an arbitrary signal input threshold voltage can be established.

(2) Vref0 : Internally generated reference voltage that determines the signal input (D_0) threshold level. By applying - 0.75 V to - 0.2 V externally to this pin, an arbitrary signal input threshold voltage can be established.

(3) Terminate unused output pins to GND through 50-ohm resistors.

CONNECTION DIAGRAM (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING
Vss	Power Supply Voltage	0.0 V ~ - 5.5 V
Vin	Applied Voltage at Signal Inputs (D_0, D_1)	+0.3 V ~ - 1.6 V
Vout	Applied Voltage at Signal Outputs (Q, $\overline{Q}$)	+0.2 V ~ - 1.75 V
Vref0, Vref1	Applied Voltage at Vref0 and Vref1 pins	+0.3 V ~ - 1.6 V
Tstor	Storage temperature	- 60 ℃ ~ +150 ℃
Tc (1)	Case temperature under Bias	- 60 ℃ ~ +125 ℃

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
Vss	Power Supply Voltage	- 4.75	- 4.5	- 4.25	V
Vref0, Vref1	Signal Input Reference Voltage	Adjust in the range from - 0.75 V to - 0.20 V			V
D_0, D_1	Signal Input Interface (D_0, D_1)	DC Coupling (See DC Characteristics)			–
OUT	Signal Output Interface (Q, $\overline{Q}$)	DC Coupling, Terminate to GND through 50Ω			–

DC CHARACTERISTICS

(Vss = - 4.75 V ~ - 4.25 V, GND = 0.0 V, Tc = 0 ~ 85 ℃ (1))

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	
V_{OH}	Output Voltage, High (Q, $\overline{Q}$)	- 0.1	0.0		V	
V_{OL}	Output Voltage, Low (Q, $\overline{Q}$)		- 0.9	- 0.85	V	
V_{IH}	Input Voltage, High (D_0, D_1)	- 0.2	0.0		V	
V_{IL}	Input Voltage, Low (D_0, D_1)		- 0.9	- 0.75	V	
Iss	Power Supply Current		510	715	mA	
Pd	Power Dissipation		2.3	3.4	W	(2)

Notes

(1) Tc : temperature at package base.

(2) Includes load current. Excludes current through input termination resistors, all of which have a value of 50 - ohm resistors.

AC CHARACTERISTICS

(Vss = - 4.5 V, GND = 0.0 V, Vref0 : Adjust in the range from -0.75 V to -0.2 V,
Vref1 : Adjust in the range from -0.75 V to -0.2 V)

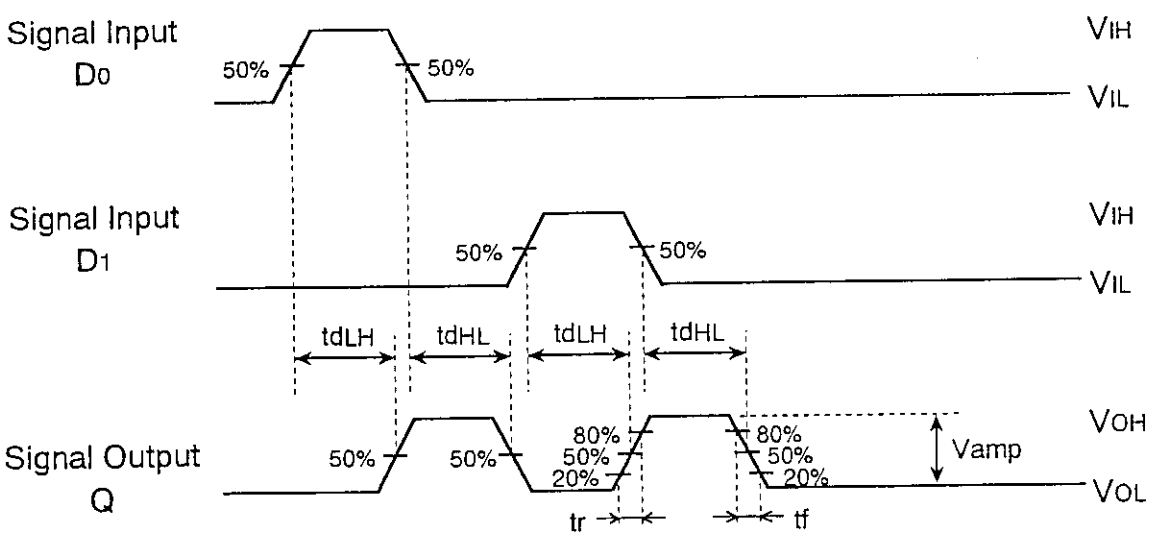
SYMBOL	PARAMETER	Tc=0 ℃			Tc=25 ℃			Tc=85 ℃			UNITS	
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
f_{MAX}	Maximum Data Operating Speed	20.0			20.0			20.0			Gb/s	(1)
Vamp	Output Voltage Amplitude	0.75	0.90		0.75	0.90		0.65	0.80		Vp-p	(2) (3)
tr	Output Rise Time (Q, $\overline{Q}$)		20	25		20	25		25	30	ps	(2) (3)
tf	Output Fall Time (Q, $\overline{Q}$)		20	25		20	25		25	30	ps	(2) (3)
tdLH	Output Rise Delay (Dn - Q, $\overline{Q}$)	210	270	330	215	275	335	220	280	340	ps	(3)
tdHL	Output Fall Delay (Dn - Q, $\overline{Q}$)	210	270	330	215	275	335	220	280	340	ps	(3)

Notes

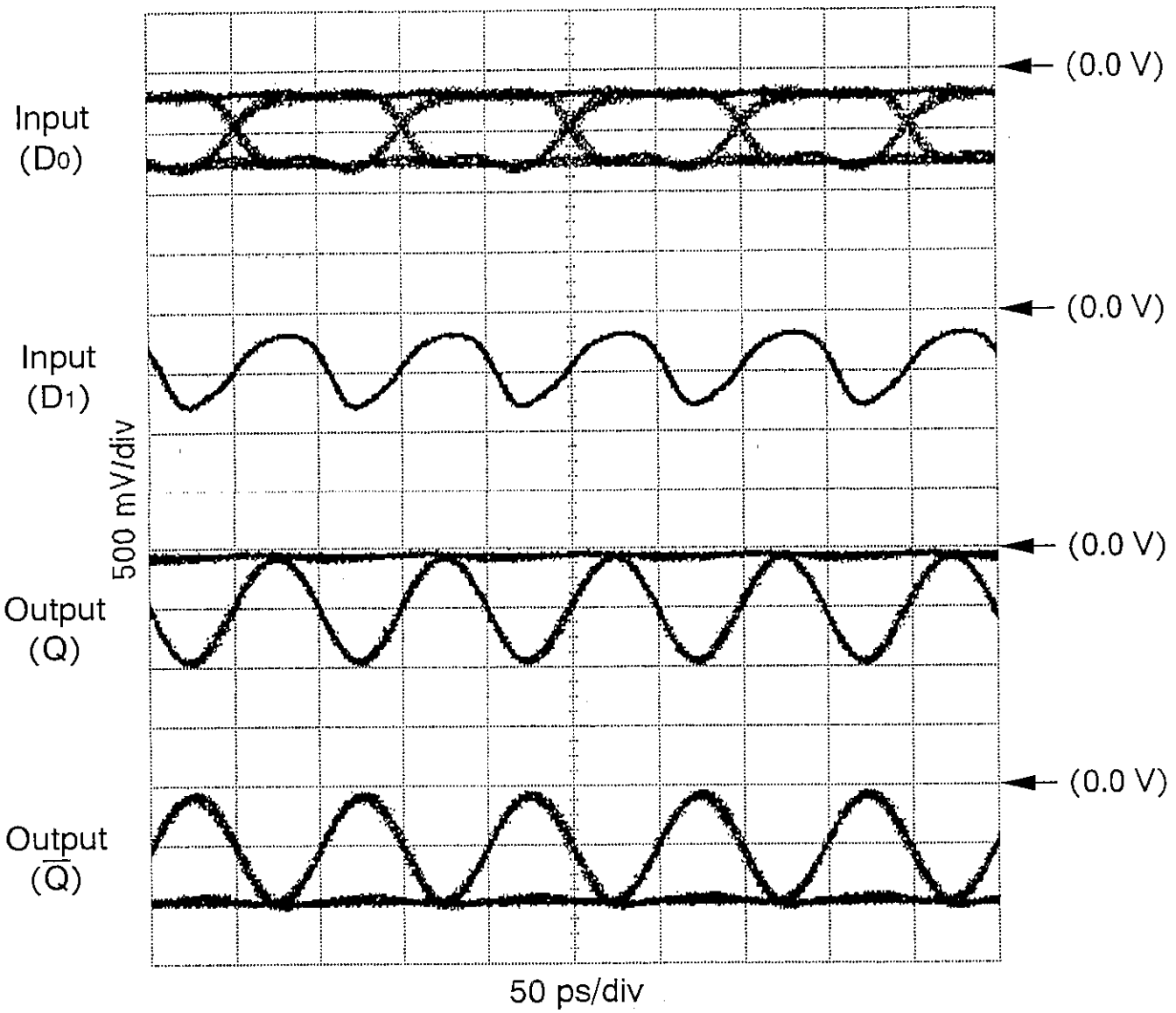
(1) Confirmed by error-free operation using a pseudo-random pattern having a word length of 2^{23}-1 bits.

(2) Measurement Condition : f = 20 Gb/s, Output pattern = 1, 0, 1, 0, ···

(3)



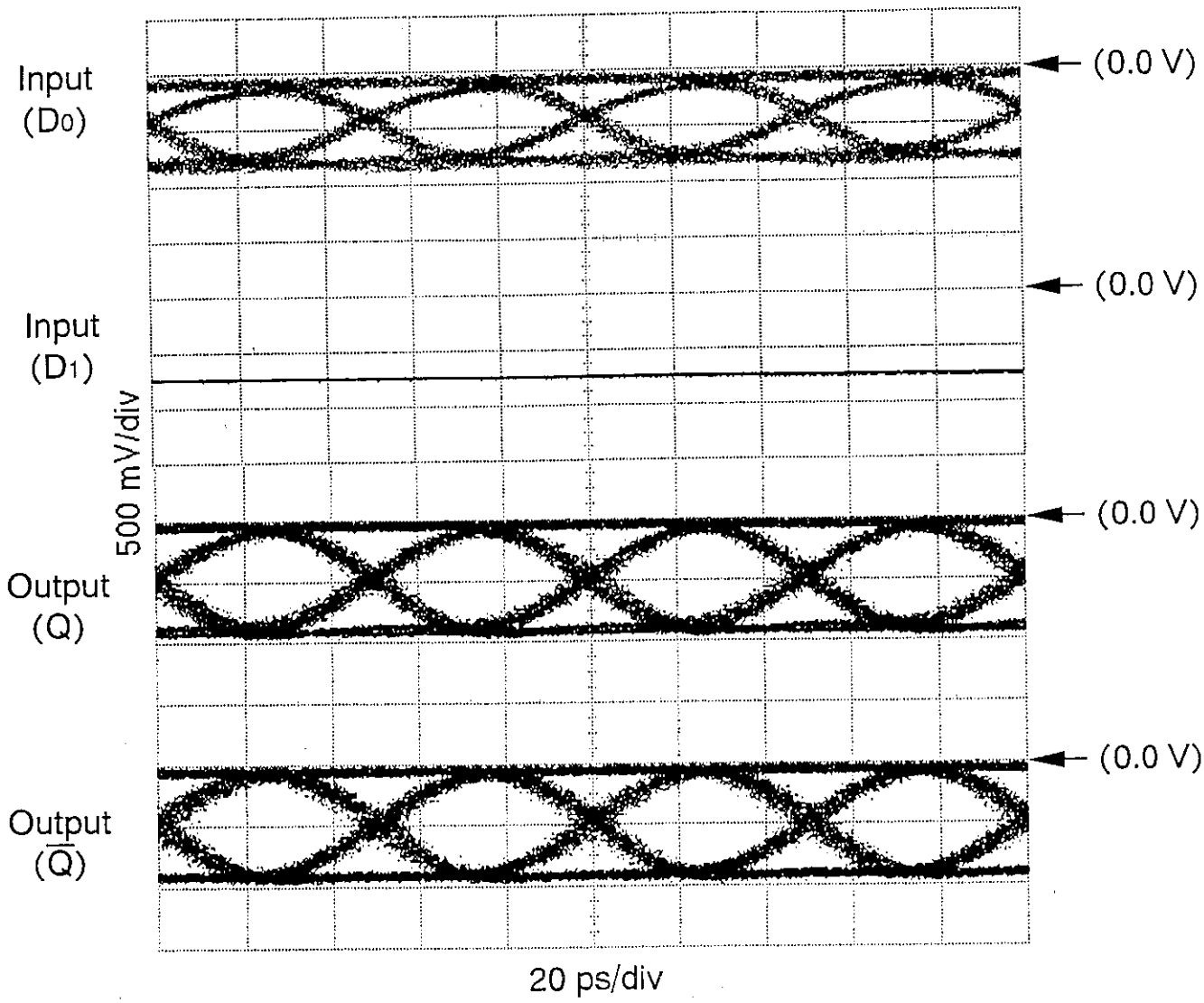
SAMPLE INPUT AND OUTPUT WAVEFORMS (20 Gb/s)



Measurement Conditions

Vss = - 4.5 V
Vref0 = - 0.5 V
Vref1 = - 0.5 V
Signal outputs connected to the 50-ohm impedance pins of a sampling oscilloscope.
Results given here were obtained using the NEL test fixture.

SAMPLE INPUT AND OUTPUT WAVEFORMS (20 Gb/s)



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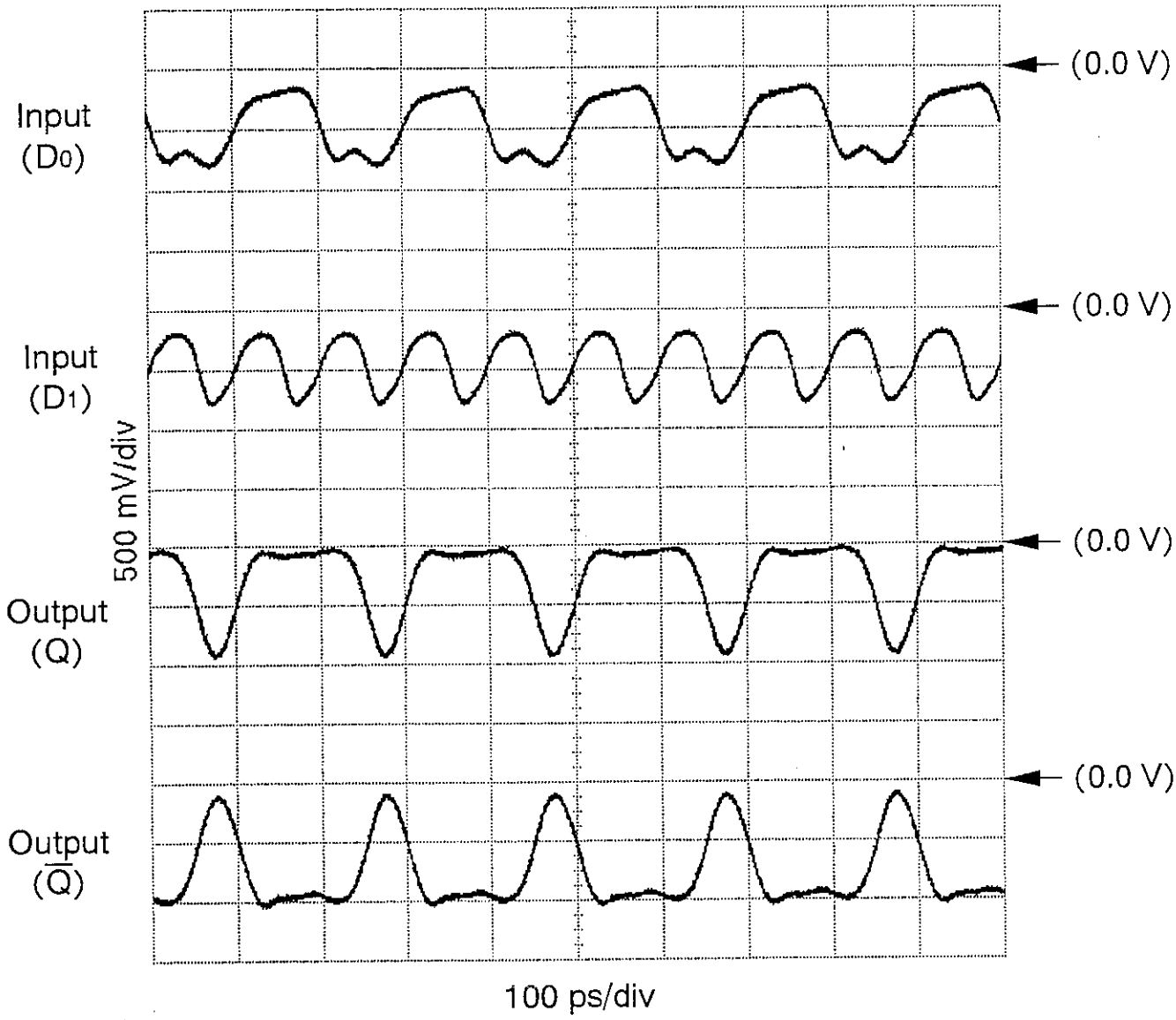
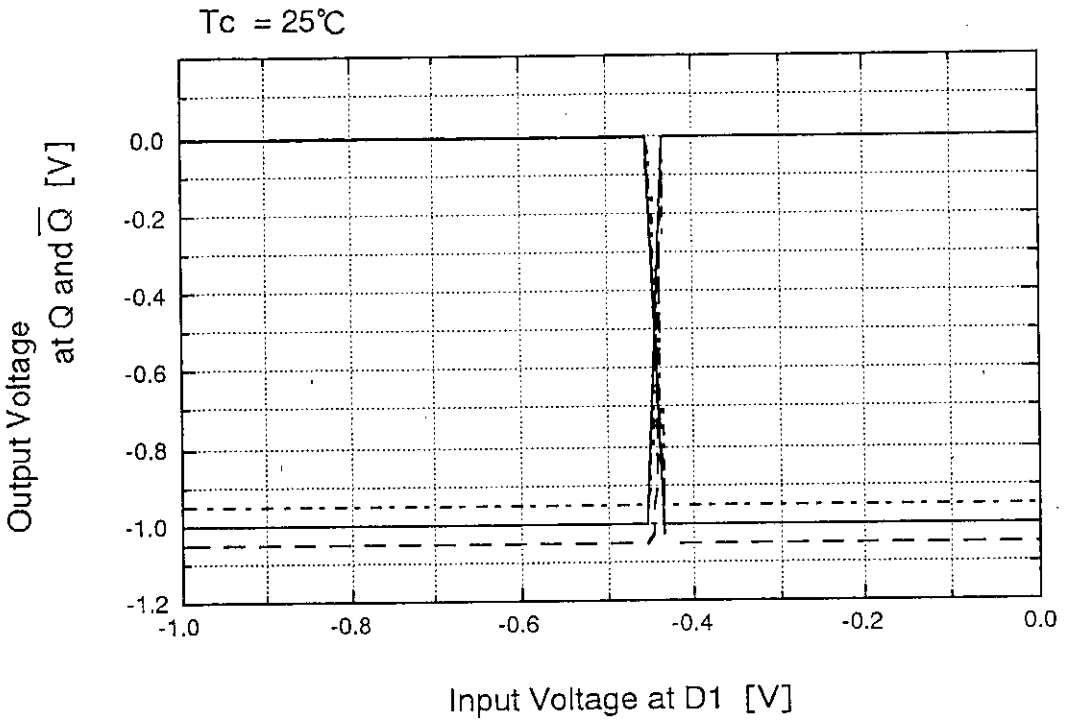


Measurement Conditions

Vss = - 4.5 V
Vref0 = - 0.5 V
Vref1 = - 0.5 V
Signal outputs connected to the 50-ohm impedance pins of a sampling oscilloscope.
Results given here were obtained using the NEL test fixture.

SAMPLE DC TRANSFER CHARACTERISTICS

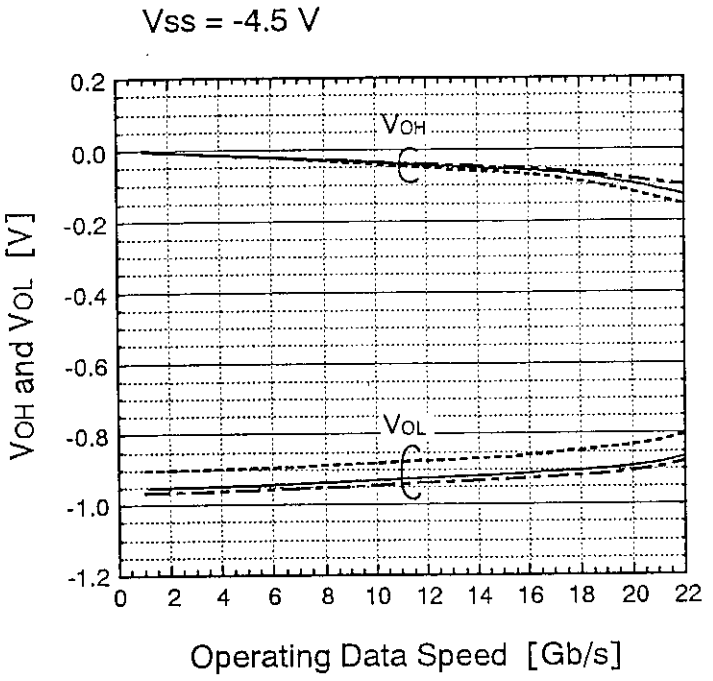


- - - - - - : Vss = - 4.25 V
——— : Vss = - 4.5 V
– – – – : Vss = - 4.75 V

Measurement Conditions

D_0 : - 0.75 V
Vref0 : Open
Vref1 = - 0.44 V
Results given here were obtained using the NEL test fixture.

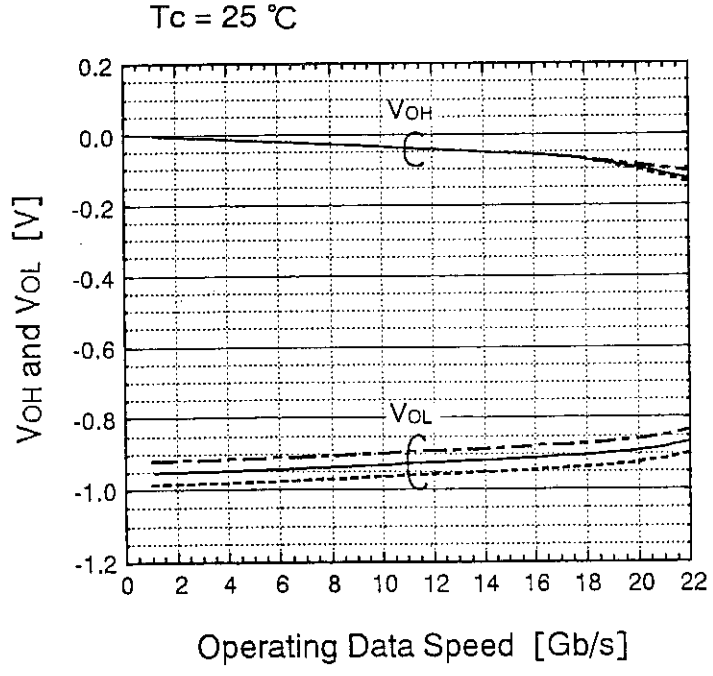
SAMPLE AC CHARACTERISTICS (Q, $\overline{Q}$)



—·—·— : Tc = 0 ℃
——— : Tc = 25 ℃
- - - - - - : Tc = 85 ℃

Measurement Conditions

D_0 : - 0.75 V
D_1 : V_{IH} = - 0.2 V, V_{IL} = - 0.75 V,
Input pattern = 1, 0, 1, 0, ···
Vref0 : Open
Vref1 = - 0.44 V
Results given here were obtained using the NEL test fixture.



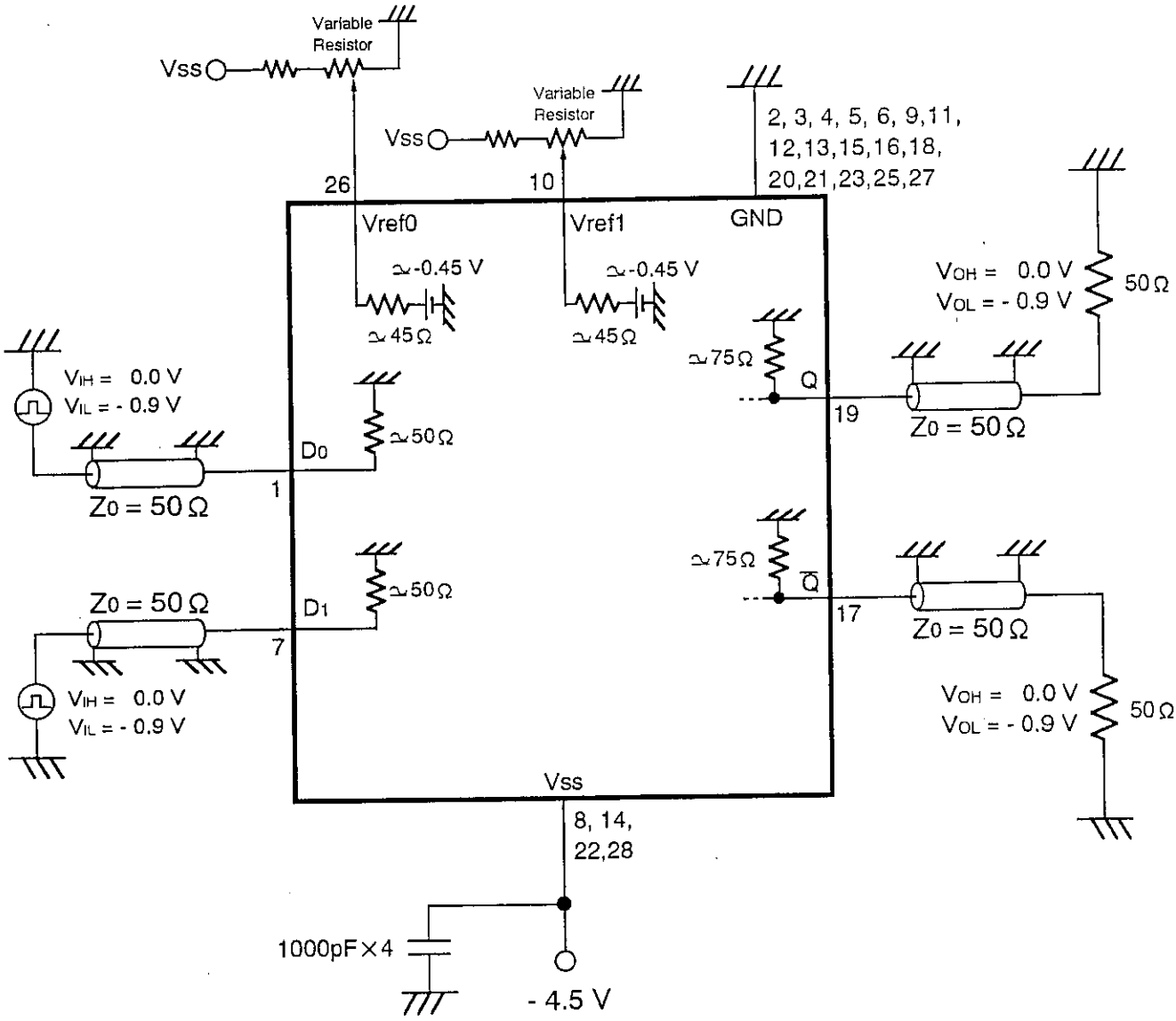
—·—·— : Vss = - 4.25 V
——— : Vss = - 4.5 V
- - - - - - : Vss = - 4.75 V

Measurement Conditions

D_0 : - 0.75 V
D_1 : V_{IH} = - 0.2 V, V_{IL} = - 0.75 V,
Input pattern = 1, 0, 1, 0, ···
Vref0 : Open
Vref1 = - 0.44 V
Results given here were obtained using the NEL test fixture.

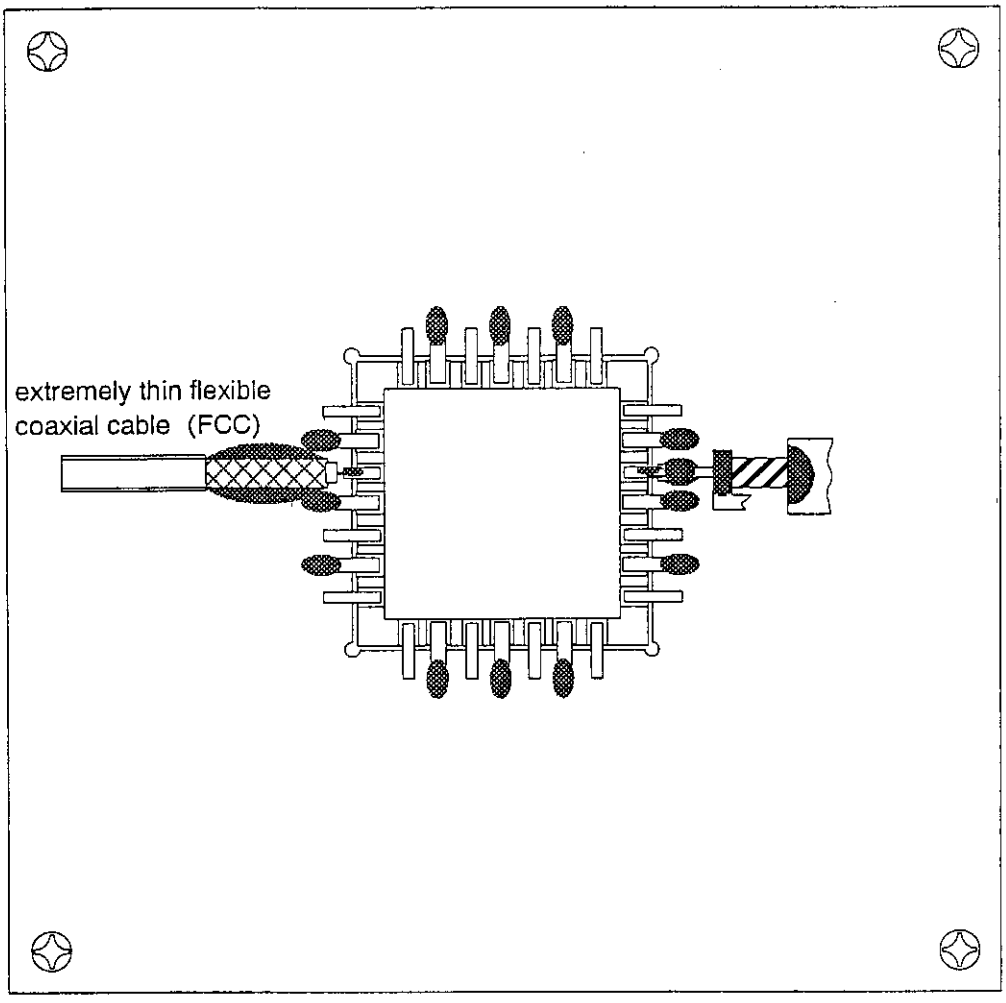
SAMPLE IMPLEMENTATION

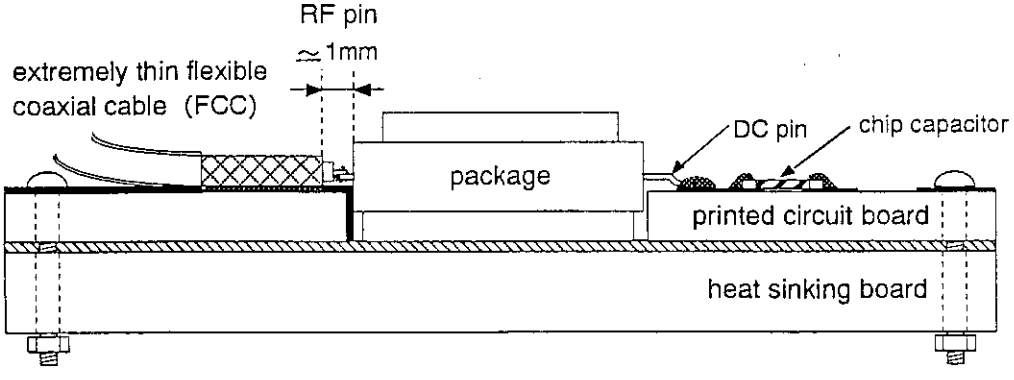
Note : Numbers represent pin numbers



Although not shown here, in place of the above variable resistors, the Vref0 and Vref1 pins can be connected directly to an external power supply.
In this case, apply approximately - 0.5 V .

SAMPLE MOUNTING





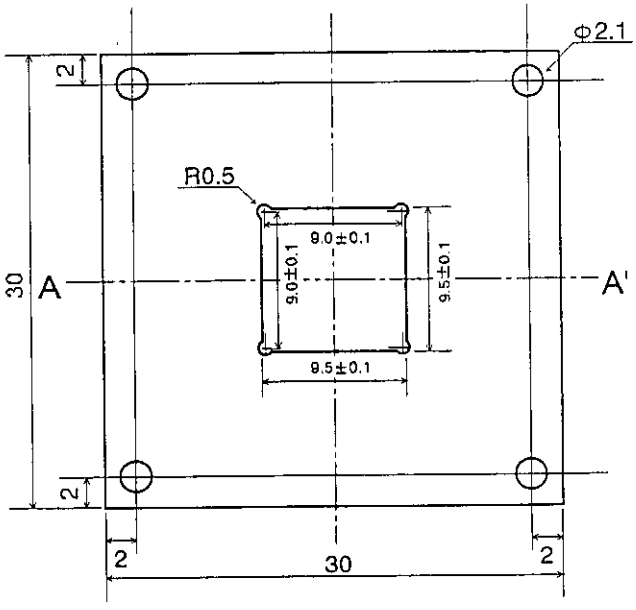
: conducting epoxy adhesive

: solder

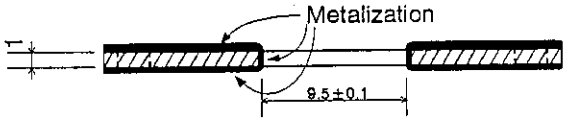
MOUNTING PARTS (unit : mm)

Printed Circuited Board

top view



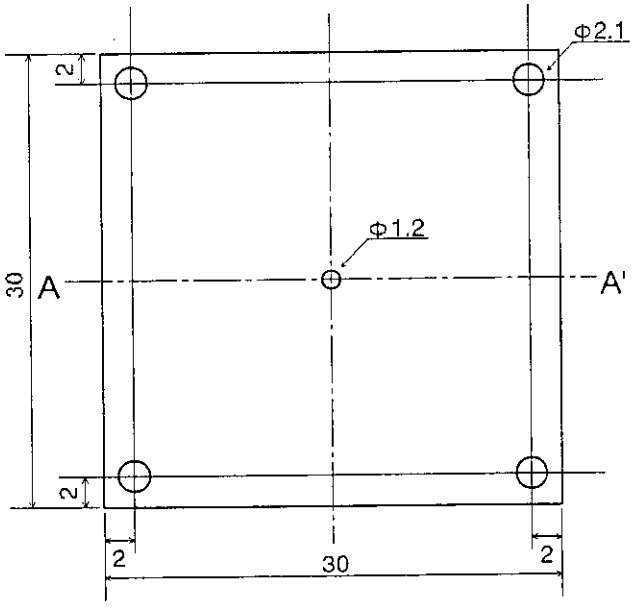
A-A' cross-sectional view



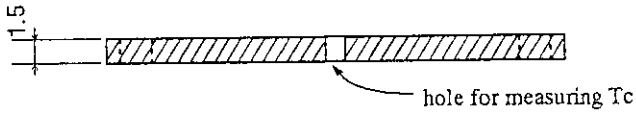
material : glass epoxy base coated
on both sides with a layer of metal and solder
(copper foil thickness : 18 μ m
solder thickness : 40～70 μ m)

Heat Sinking Board

top view



A-A' cross-sectional view



material : aluminum board

Solder

Sn : 60%, Φ0.6mm
(melting point : 190℃)

Conducting epoxy adhesive

Sumitomo bakelite CRM-1061

Screws for attaching the printed circuit board to the heat sinking board

4 M2×8, cross-type small screws

Nuts

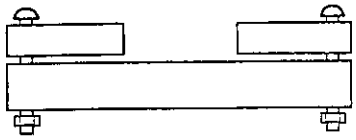
4 M2 hex nuts

Spring washers

4 M2 spring washers

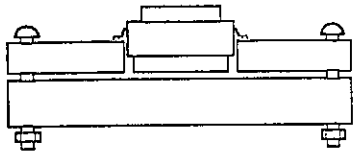
MOUNTING PROCEDURE

①



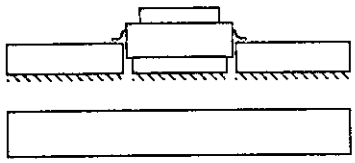
Temporarily fasten the printed circuit board to the heat sinking board with the screws.

②



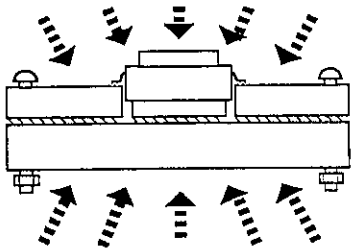
Insert the IC package into the center part of the printed circuit board. Solder the GND pins to the printed circuit board.

③



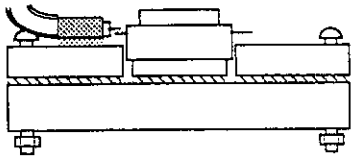
Unfasten the printed circuit board from the heat sinking board. Thinly paint the entire bottom surfaces of the printed circuit board and the IC with the conducting epoxy adhesive. Make sure that silver paste is not applied to the region between the printed circuited board and the IC.

④



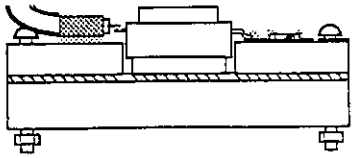
Again fasten the printed circuit board to the heat sinking board with the screws. Bake the fixture in an oven for 60 minutes at 150℃ (120℃～170℃).

⑤



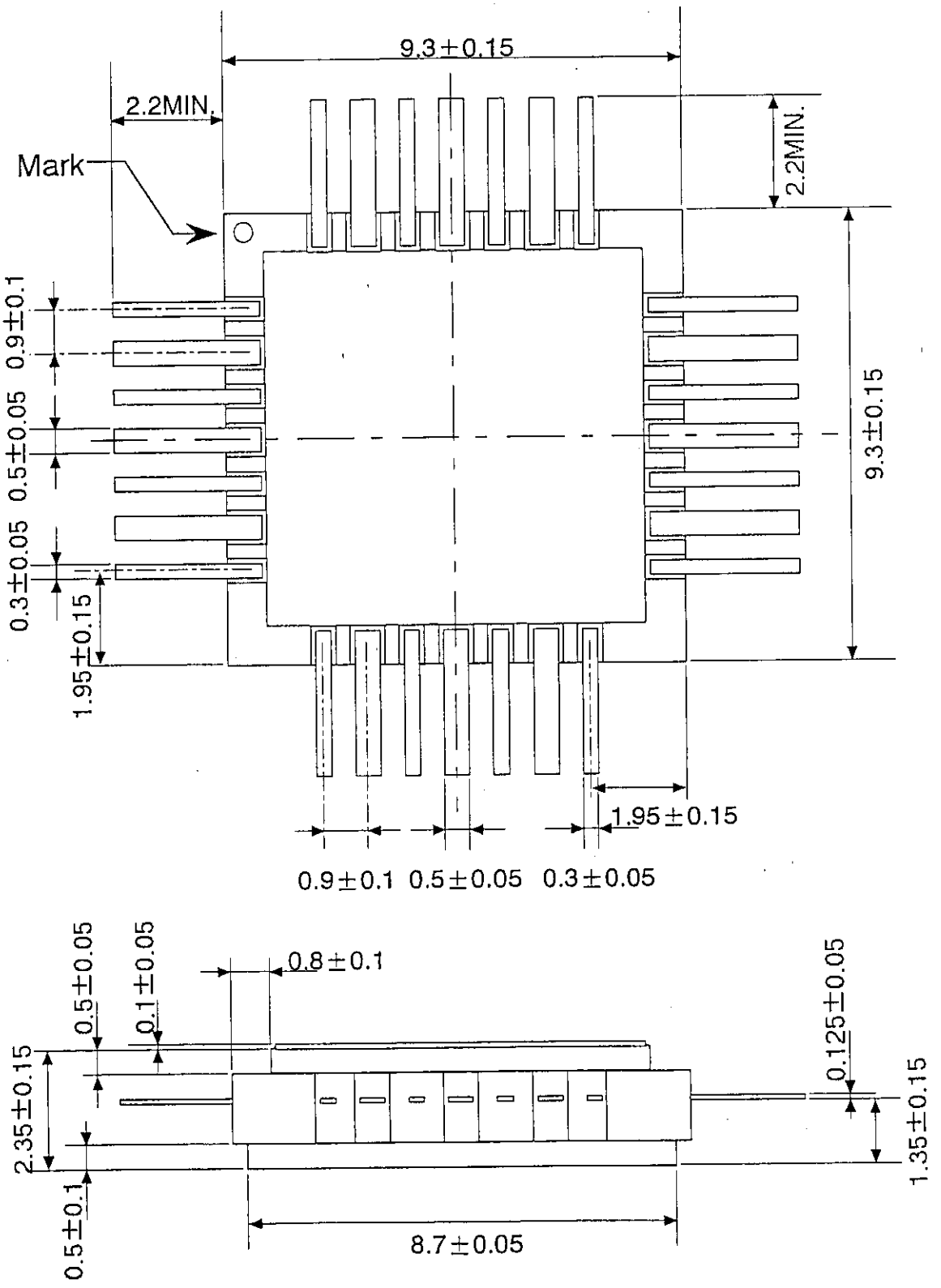
Take the fixture out of the oven. After the IC has cooled, solder the FCC to the input/output pins.

⑥



As the final step, solder the chip capacitors, chip resistors, etc., to the DC pins.

TB 28 - PIN PACKAGE DIMENSION (mm)



HANDLING INSTRUCTIONS

Since the NLG4001 is fabricated with GaAs MESFET's (Metal Semiconductor Field Effect Transistors), users are recommended to follow the instructions below to prevent damage to the chip from electro-static discharge.

1) Use a conductive working desk connected to the ground (or, a conductive table top connected to the ground).
2) Require all handling personnel to wear a conductive bracelet or wrist-strap connected to the ground through a 1 M-ohm resistors.
3) Ground all test equipment.
4) Ground all soldering iron tops.
5) Store IC's and other devices such as chip capacitors in their conductive carriers until they are soldered.

NEL

Caution

1. In order to improve products and technology, specifications are subject to change without notice.

2. When using the products, be sure the latest information and specifications are used.

3. Circuit drawings etc. shall be provided for the purpose of information only on application examples not for actual installation of equipment. NTT Electronics Corp. shall not assume any liability for damage that may result from the use of these circuit drawings etc. NTT Electronics Corp. shall not assent to or guarantee any rights of execution for patent rights of the third parties and other rights that may be raised for use of these circuit drawings.

4. To make a design, the products shall be used within the assured ranges with respect to maximum ratings, voltage, and radiation. NTT Electronics Corp. shall not take any responsibility for damage caused by neglecting the assured values or improper usage.

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