NIF62514

Product Preview

HDPlus N-Channel Self-protected Field Effect Transistors w/ Temperature and Current Limit

HDPlus devices are an advanced series of power MOSFETs which utilize ON's latest MOSFET technology process to achieve the lowest possible on–resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain–to–Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate–to–Source Clamp.

Features

- Current Limitation
- Thermal Shutdown with Automatic Restart
- Short Circuit Protection
- Low $R_{DS(on)}$
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection

ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	40	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	40	Vdc
Gate–to–Source Voltage	V_{GS}	±16	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Pulsed ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.8 1.8 8*	Adc Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2)	P_D P_D	1.1 1.73	W
Thermal Resistance Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$	 114 72.3	°C/W
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, V_{DS} = 40 Vdc, I_L = 2.8 Apk, L = 80 mH, R_G = 25 Ω)	E_{AS}	300	mJ

1. Mounted onto min pad board.
2. Mounted onto 1″ pad board.

* Limited by the current limit circuit.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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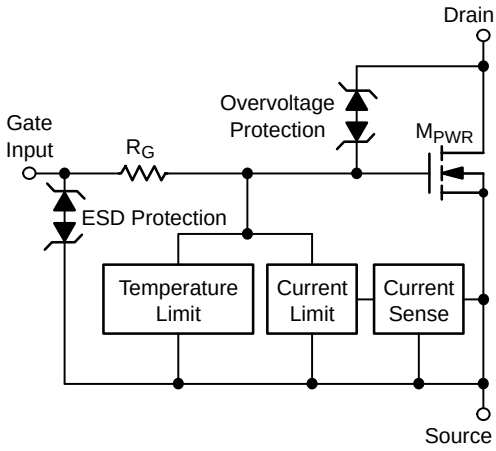
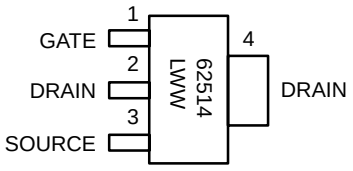
2.8 AMPERES
40 VOLTS CLAMPED
$R_{DS(on)}$ = 125 mΩ



SOT–223
CASE 318E
STYLE 3

MARKING DIAGRAM



(Top View)

62514 = Specific Device Code
L = Location Code
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NIF62514	SOT–223	4000/Tape & Reel

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = 150°C)	$V_{(BR)DSS}$	 40 40	 45 –	 50 50	 Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	 – –	 4.1 –	 10 100	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc) (V_{GS} = –5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	 – –	 50 450	 100 1000	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 150 μAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 1.0 –	 1.55 3.8	 2.0 4.6	 Vdc mV/°C
Static Drain–to–Source On–Resistance (Note 3) (V_{GS} = 10 Vdc, I_D = 1.4 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 1.4 Adc, T_J @ 150°C)	$R_{DS(on)}$	 – –	 105 190	 125 215	mΩ
Static Drain–to–Source On–Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 1.4 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 1.4 Adc, T_J @ 150°C)	$R_{DS(on)}$	 – –	 130 215	 150 240	mΩ

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Current Limit	(V_{GS} = 5.0 Vdc) (V_{GS} = 5.0 Vdc, T_J = 150°C)	I_{LIM}	– –	7.5 4.5	– –	Adc
Current Limit	(V_{GS} = 10 Vdc) (V_{GS} = 10 Vdc, T_J = 150°C)	I_{LIM}	– –	8.5 5.5	– –	Adc
Temperature Limit (Turn–off)	V_{GS} = 5.0 Vdc	$T_{LIM(off)}$	150	175	–	°C
Temperature Limit (Circuit Reset)	V_{GS} = 5.0 Vdc	$T_{LIM(on)}$	135	160	–	°C
Temperature Limit (Turn–off)	V_{GS} = 10 Vdc	$T_{LIM(off)}$	150	160	–	°C
Temperature Limit (Circuit Reset)	V_{GS} = 10 Vdc	$T_{LIM(on)}$	135	145	–	°C

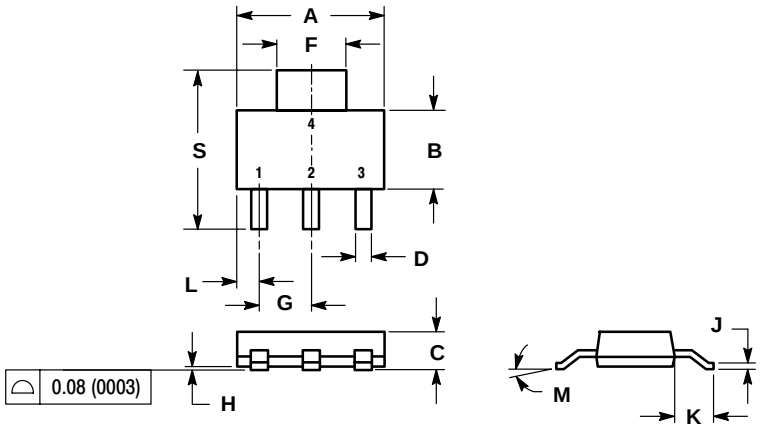
ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro–Static Discharge (ESD) Capability		_	1800	–	–	V
Charge Device Model (CDM) Capability		_	2000	–	–	V

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

PACKAGE DIMENSIONS

SOT−223
CASE 318E−04
ISSUE K



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
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