

DATA SHEET

NE57605

Lithium-ion battery protector
for 3 or 4 cell battery packs

Product data

2001 Oct 03

Lithium-ion battery protector for 3 or 4 cell battery packs

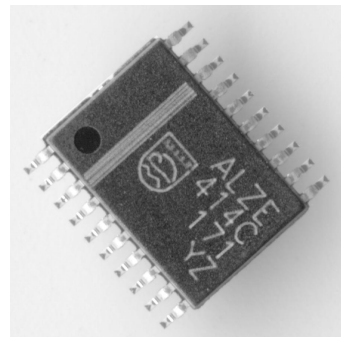
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GENERAL DESCRIPTION

The NE57605 is a 3-4-cell Li-ion protection IC. Its over- and under-voltage accuracy is trimmed to within ± 25 mV (5%), and is available to match the requirements of all lithium-ion cells manufactured in the market today.

FEATURES

- Trimmed overvoltage trip point to within ± 25 mV
- Programmable overvoltage trip time delay
- Trimmed undervoltage trip point to within ± 25 mV
- Very low undervoltage sleep quiescent current 2 mA.
- Discharge overcurrent cutoff.
- Low operating current (10 mA).
- Very small package (TSOP-20A).



APPLICATIONS

- Laptop Computers
- Other battery-powered devices

SIMPLIFIED SYSTEM DIAGRAM

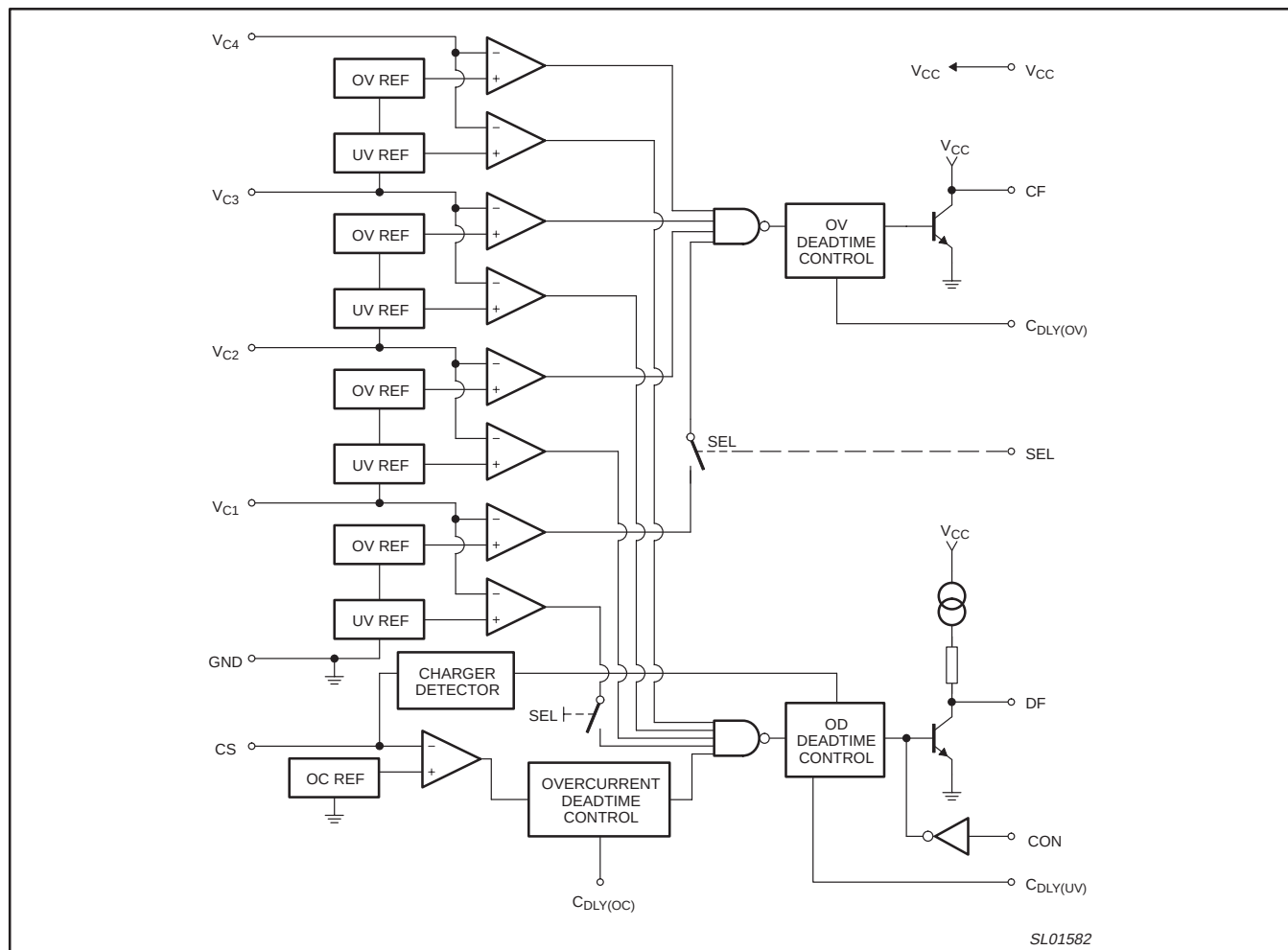


Figure 1. Simplified system diagram.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		TEMPERATURE RANGE
	NAME	DESCRIPTION	
NE57605CD	TSOP-20A	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	–20 to +70 °C

Part number marking

Each device is marked with a four letter code. The first three letters in the top line of markings designate the product. The fourth letter, represented by "x", is a date code. The remaining markings are manufacturing codes.

Part Number	Marking
NE57605CD	ALZx

PIN CONFIGURATION

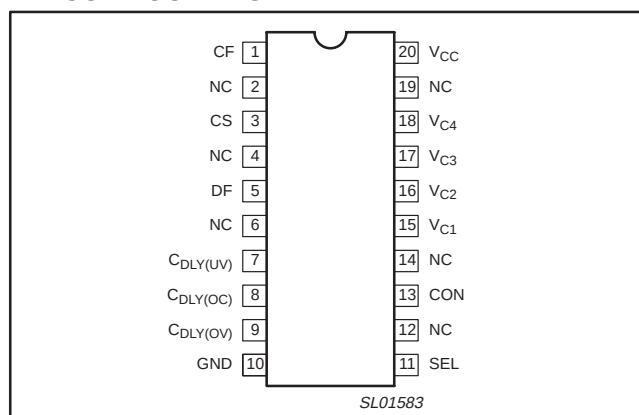


Figure 2. Pin configuration.

PIN DESCRIPTION

PIN	SYMBOL	I/O	DESCRIPTION
1	CF	Output	Overcharge detection output pin. NPNT _r open collector output. Normal: high impedance. Overcharge: LOW.
2, 4, 6, 12, 14, 19	NC	–	Not Connected.
3	CS	Input	Overcurrent detection pin. Monitors load current equivalently by the voltage drop between discharge control FET source and drain, and makes DF pin HIGH when the voltage goes below overcurrent detection voltage, turning off discharge control FET. After overcurrent detection, current flows from this pin and when there is a light load, overcurrent mode is released. This function does not operate in overdischarge mode.
5	DF	Output	Discharge control FET (P-ch) drive pin. Normal: LOW. Overdischarge: HIGH.
7	C _{DLY(UV)}	Input	Overdischarge detection dead time setting pin. Dead time can be set by connecting a capacitor between C _{DLY(UV)} pin and ground.
8	C _{DLY(OC)}	Input	Overcurrent detection dead time setting pin. Dead time can be set by connecting a capacitor between C _{DLY(OC)} pin and ground.
9	C _{DLY(OV)}	Input	Overcharge detection dead time setting pin. Dead time can be set by connecting a capacitor between C _{DLY(OV)} pin and ground.
10	GND	–	Ground pin.
11	SEL	Input	3/4 cell selection pin. SEL pin = GND: 3 cell (Connect V _{C1} to GND). SEL pin = V _{CC} : 4 cell.
13	CON	Input	Discharge FET ON/OFF pin. CON pin LOW; DF pin LOW (Normal mode). CON pin HIGH; DF pin HIGH (Discharging prohibited).
15	V _{C1}	Input	V1 cell high side voltage input pin.
16	V _{C2}	Input	V2 cell high side voltage and V3 cell low side voltage input pin.
17	V _{C3}	Input	V3 cell high side voltage and V4 cell low side voltage input pin.
18	V _{C4}	Input	V4 cell high side voltage input pin.
20	V _{CC}	–	Power supply input pin.

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MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{CC(max)}$	Power supply voltage	-0.3	+24	V
$V_{CF(max)}$	CF pin impressed voltage	-0.3	+24	V
$V_{SEL(max)}$	SEL pin impressed voltage	-0.3	+24	V
$V_{CON(max)}$	CON pin impressed voltage	-0.3	+24	V
T_{opr}	Operating ambient temperature range	-20	+70	°C
T_{stg}	Storage temperature	-40	+125	°C
P_D	Power dissipation	—	300	mW

ELECTRICAL CHARACTERISTICS

$T_{amb} = 25\text{ °C}$; $V_{IN} = V_{CE}$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	UNIT
I_{CC1}	Current consumption 1 (V_{CC} pin)	$V_{CELL} = 4.4\text{ V}$; $CON = 0\text{ V}$	—	55	110	μA
I_{CC2}	Current consumption 2 (V_{CC} pin)	$V_{CELL} = 3.5\text{ V}$; $CON = 0\text{ V}$	—	27	50	μA
I_{CC3}	Current consumption 3 (V_{CC} pin)	$V_{CELL} = 1.8\text{ V}$; $CON = 0\text{ V}$	—	2	4	μA
I_{CC4}	Current consumption 4 (V_{CC} pin)	$V_{CELL} = 3.5\text{ V}$; $CON = V_{CC}$	—	12	20	μA
I_{CC5}	Current consumption 5 (V_{CC} pin)	$V_{CELL} = 1.8\text{ V}$; $CON = V_{CC}$	—	1	2	μA
I_{1V4}	Consumption current (V4 pin) 1	$V_{CELL} = 4.4\text{ V}$	—	10	20	μA
I_{2V4}	Consumption current (V4 pin) 2	$V_{CELL} = 3.5\text{ V}$	—	8	15	μA
I_{3V4}	Consumption current (V4 pin) 3	$V_{CELL} = 1.8\text{ V}$	—	2.5	5.0	μA
I_{V3}	V3 pin input current	$V_{CELL} = 3.5\text{ V}$	-300	0	+300	nA
I_{V2}	V2 pin input current	$V_{CELL} = 3.5\text{ V}$	-300	0	+300	nA
I_{V1}	V1 pin input current	$V_{CELL} = 3.5\text{ V}$	-300	0	+300	nA
V_{CELLU}	Overcharge detection voltage	$V_{CELL}: 4.2\text{ V} \rightarrow 4.4\text{ V}$; $T_{amb} = 0 \sim 50\text{ °C}$	4.10	4.35	4.60	V
ΔV_U	Overcharge hysteresis voltage	$V_{CELL}: 4.2\text{ V} \rightarrow 4.4\text{ V} \rightarrow 3.9\text{ V}$	—	200	260	mV
t_{OV}	Overcharge sensing dead time	$C_{OV} = 0.1\text{ }\mu\text{F}$	0.5	1.0	1.5	s
V_{CELLS}	Overdischarge detection voltage	$V_{CELL}: 3.5\text{ V} \rightarrow 1.8\text{ V}$	2.20	2.30	2.40	V
V_{CELLD}	Discharge resume voltage	$V_{CELL}: 1.8\text{ V} \rightarrow 3.5\text{ V}$	2.85	3.00	3.15	V
ΔV_{DS}	Overdischarge hysteresis voltage	$V_{CELLD} - V_{CELLS}$	0.45	0.70	0.95	V
t_{CDC}	Overdischarge sensing dead time	$C_{DC} = 0.1\text{ }\mu\text{F}$	0.5	1.0	1.5	s
V_{OC}	Overcurrent detection voltage	$V_{CC} - V_{CS}$; DF	135	150	165	mV
ΔV_{OC}	Overcurrent hysteresis voltage		—	20	40	mV
t_{COL1}	Overcurrent sensing dead time 1	$C_{OL} = 0.001\text{ }\mu\text{F}$	5	10	15	ms
t_{COL2}	Overcurrent sensing dead time 2	$C_{OL} = 0.001\text{ }\mu\text{F}$; $V_{CC} - CS > 1.0\text{ V}$	—	1.5	3.0	ms
t_{COL3}	Overcurrent sensing dead time 3	$C_{OL} = 0.001\text{ }\mu\text{F}$	5	10	15	ms
Overcurrent reset conditions		Load release conditions 500 kΩ				
$I_{SO}D_{CH}$	DF pin source current	$V_{CELL} = 1.8\text{ V}$; SW1: A $V_{DF} = V_{CC} - 0.8\text{ V}$	20	—	—	μA
$I_{SI}D_{CH}$	DF pin sink current	$V_{CELL} = 3.5\text{ V}$; SW1: A $V_{DF} = 0.8\text{ V}$	20	—	—	μA
$V_{TH}D_{CH}$	DF pin output voltage HIGH	$V_{CC} - V_{DF}$; $I_{SO} = 20\text{ }\mu\text{A}$; SW1: B	—	—	0.8	V
$V_{TH}D_{CL}$	DF pin output voltage LOW	$V_{DF} - GND$; $I_{SI} = -20\text{ }\mu\text{A}$; SW1: B	—	—	0.8	V
$I_{SI}OV$	OV pin sink current	$V_{OV} = 0.4\text{ V}$; $T_{amb} = -20\text{ °C to } +70\text{ °C}$	100	—	—	μA
$I_{LK}OV$	OV pin leak current	$V_{OV} = 24\text{ V}$	—	—	0.1	μA
	CON pin LOW voltage	DF = HIGH	—	—	0.4	V
	CON pin HIGH voltage	DF = LOW	$V_{CC} - 0.4$	—	—	V
	CON pin current	$V_{CELL} = 3.5\text{ V}$; $CON = 0.4\text{ V}$	—	1	2	μA
	SEL pin LOW voltage	for 3 cell	—	—	0.4	V
	SEL pin HIGH voltage	for 4 cell	$V_{CC} - 0.4$	—	—	V
	SEL pin current	$V_{CELL} = 3.5\text{ V}$; $SEL = 0.4\text{ V}$	—	1	2	μA

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TECHNICAL DISCUSSION

Lithium cell safety

Lithium-ion and lithium-polymer cells have a higher energy density than that of nickel-cadmium or nickel metal hydride cells and have a much lighter weight. This makes the lithium cells attractive for use in portable products. However, lithium cells require a protection circuit within the battery pack because certain operating conditions can be hazardous to the battery or the operator, if allowed to continue.

Lithium cells have a porous carbon or graphite anode where lithium ions can lodge themselves in the pores. The lithium ions are separated, which avoids the hazards of metallic lithium.

If the lithium cell is allowed to become overcharged, metallic lithium plates out onto the surface of the anode and volatile gas is generated within the cell. This creates a **rapid-disassembly hazard** (the battery ruptures). If the cell is allowed to over-discharge (V_{cell} less than approximately 2.3 V), then the copper metal from the cathode goes into the electrolyte solution. This shortens the cycle life of the cell, but presents no safety hazard. If the cell experiences excessive charge or discharge currents, as happens if the wrong charger is used, or if the terminals short circuit, the internal series resistance of the cell creates heating and generates the volatile gas which could rupture the battery.

The protection circuit continuously monitors the cell voltage for an **overcharged condition** or an **overdischarged condition**. It also continuously monitors the output for an **overcurrent condition**. If any of these conditions are encountered, the protection circuit opens a series MOSFET switch to terminate the abnormal condition. The lithium cell protection circuit is placed within the battery pack very close to the cell.

Charging control versus battery protection

The battery pack industry does not recommend using the pack's internal protection circuit to end the charging process. The external battery charger should have a charge termination circuit in it, such as that provided by the SA57611. This provides two levels of overcharge protection, with the primary protection of the external charge control circuit and the backup protection from the battery pack's protection circuit. The charge termination circuit will be set to stop charging at a level around 50 mV less than the overvoltage threshold voltage of the battery pack's own protection circuit.

Lithium cell operating characteristics

The internal resistance of lithium cells is in the 100 mΩ range, compared to the 5–20 mΩ of the nickel-based batteries. This makes the Lithium-ion and polymer cells better for lower battery current applications (less than 1 ampere) as found in cellular and wireless telephones, palmtop and laptop computers, etc.

The average operating voltage of a lithium-ion or polymer cell is 3.6 V as compared to the 1.2 V of NiCd and NiMH cells. The typical discharge curve for Lithium cell is shown in Figure 3.

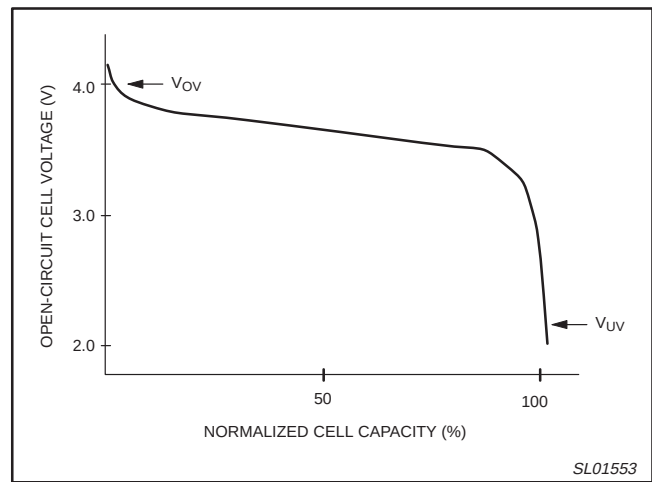


Figure 3. Lithium discharge curve.

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Charging Lithium cells

The lithium cells must be charged with a dedicated charging IC such as the NE57610. These dedicated charging ICs perform a current-limited, constant-voltage charge, as shown in Figure 4.

The charger IC begins charging with a current that is typically the rating of the cell (1C) or the milliampere rating of the cell. As the cell approaches its full-charge voltage rating (V_{OV}), the current entering the cell decreases, and the charger IC provides a constant voltage. When the charge current falls below a preset amount, 5 mA for example, the charge is discontinued.

If charging is begun below the overdischarged voltage rating of the cell, it is important to slowly raise the cell voltage up to this overdischarged voltage level. This is done by a **reconditioning charge**. A small amount of current is provided to the cell (50 mA for example), and the cell voltage is allowed a period of time to rise to the overdischarged voltage. If the cell voltage recovers, then a normal charging sequence can begin. If the cell does not reach the overdischarged voltage level, then the cell is too damaged to charge and the charge is discontinued.

To take advantage of the larger energy density of lithium cells it is important to allow enough time to completely charge the cell. When the charger switches from constant current to constant voltage charge (Point B, Figure 4) the cell only contains about 80 percent of its full capacity. When the cell is 100 mV less than its full rated charge voltage the capacity contained within the cell is 95 percent. Hence, allowing the cell to slowly complete its charge takes advantage of the larger capacity of the lithium cells.

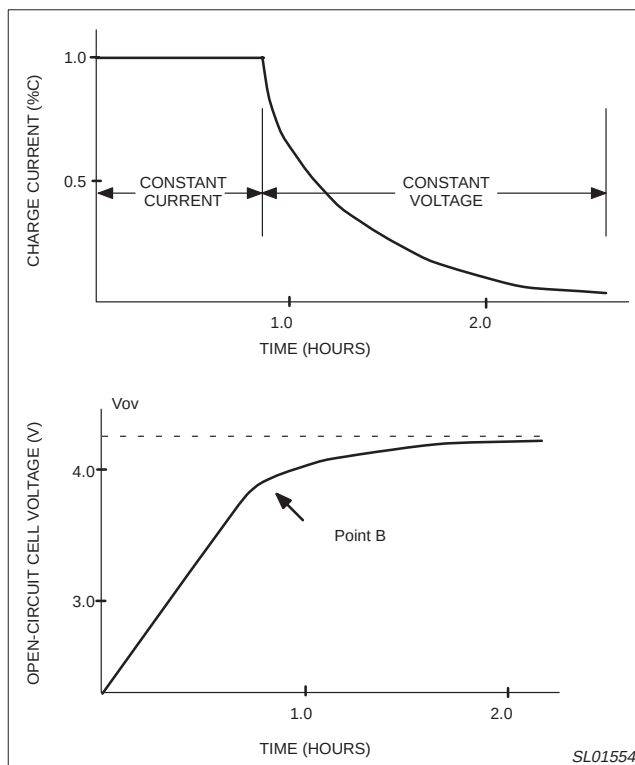


Figure 4. Lithium Cell charging Curves

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APPLICATION INFORMATION

The typical 4-cell lithium-ion or polymer protection circuit based upon the NE57605 is seen in Figure 5.

With a minor redesign, the NE57605 3-cell system is shown in Figure 6. Pin 11 (SEL) is connected to ground.

The NE57605 drives the series P-Channel MOSFETs to states determined by each of the cell's voltage and the battery pack load current. During normal periods of operation, both the discharge and charge MOSFETs are in the ON state, thus allowing bi-directional current flow.

If the battery pack is being charged, and any of the cell's voltage exceeds the overvoltage threshold, then the charge MOSFET is turned OFF (the charge FET is the FET closest to the pack's external terminal). The cell's voltage must fall lower than the overvoltage hysteresis voltage ($V_{OV(hyst)}$) before the charge MOSFET is again turned ON.

If the battery pack is being discharged and the undervoltage threshold ($V_{UV(th)}$) is exceeded by any of the cells, then the discharge MOSFET is turned OFF. It will not run back ON until a charger is applied to the pack's external terminals **and** the cell's voltage rises above the undervoltage hysteresis voltage ($V_{UV(hyst)}$).

When the battery pack is being discharged, the load current causes the voltage across the discharge MOSFET to increase past the overcurrent threshold voltage ($V_{OC(th)}$), then the discharge MOSFET is turned OFF after a fixed 7–18 ms delay. If short-circuit is placed across the pack's terminals, then the discharge MOSFET is turned OFF after a 100–300 μ s time delay to avoid damaging the MOSFETs.

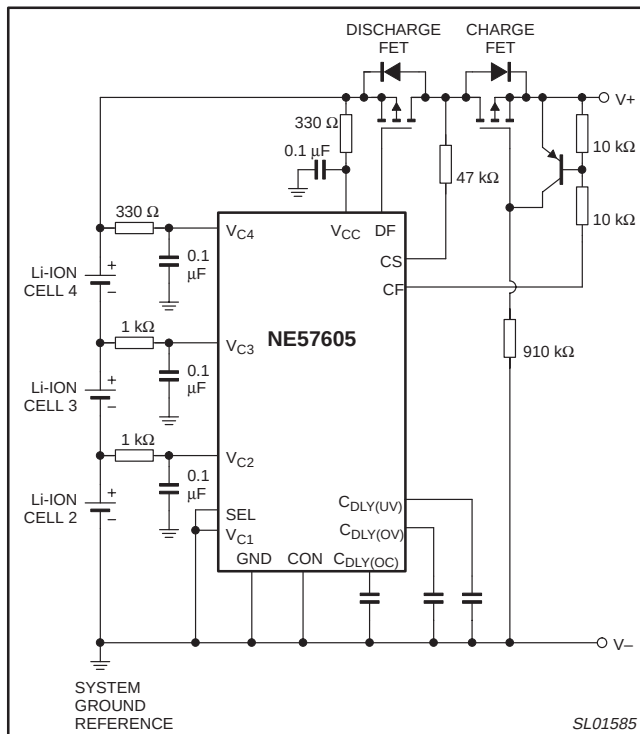


Figure 6. 3-cell protection circuit

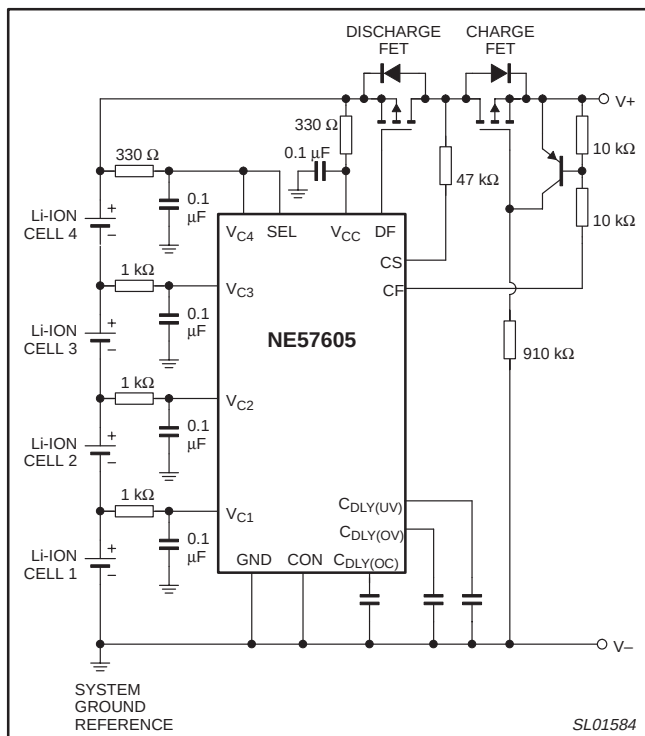


Figure 5. 4-cell protection circuit

FET STATUS FOR NORMAL AND ABNORMAL CONDITIONS

Operating Mode and Charging Condition	Charge FET (CF)	Discharge FET (DF)
Normal (charging or discharging)	ON	ON
Overcharge (charging)	OFF	ON
Overcharge (discharging)	ON	ON
Overdischarge (discharging)	OFF	OFF
Overdischarge (charging)	ON	ON
Overcurrent (charging or discharging)	OFF	OFF

Normal mode:

Overdischarge detection voltage < battery voltage
< overcharge detection voltage
Discharge current < overcurrent detection level

Overcharge mode:

Battery voltage > overcharge detection voltage

Overdischarge mode:

Overdischarge detection voltage > battery voltage

Overcurrent mode:

Discharge current > overcurrent detection level
voltage between V_M and GND = discharge current $\times$ FET ON resistance (discharge or charge FET)

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The R-C filters around the NE57605

One needs to place R-C filters on the positive input pins of the NE57605. These are primarily to shield the IC from electrostatic occurrences and spikes on the terminals of the battery pack. A secondary need is during the occurrence of a short-circuit across the battery pack terminals. Here, the Li-ion cell voltage could collapse and cause the IC to enter an unpowered state. The R-Cs then provide power during the first instance of the short circuit and allow the IC to turn OFF the discharge MOSFET. The IC can then enter an unpowered state. Lastly, the R-C filter on the node between the cells filters any noise voltage caused by noisy load current.

The value of 330 Ω and 0.1 μF are good for the V_{CC} and V_{C4} pins. Values of 1 k Ω and 0.1 μF are good for the V_{C1} , V_{C2} and V_{C3} pins.

Selecting the optimum MOSFETs

For a 3- or 4-cell battery pack, a standard MOSFET should be used. These MOSFETs have turn-on thresholds of 2.5 V and are considered full-on at 10 V V_{GS} . The total 4-cell pack voltage will be a maximum of 17.2 V, which is within safe operating range of the gate voltage which is typically around 20 volts.

The MOSFETs should have a voltage rating greater than 30 V and should have a high avalanche rating to survive any spikes generated across the battery pack terminals.

The current rating of the MOSFETs should be greater than four times the maximum "C-rating" of the cells. The current rating,

though, is more defined by the total series resistance of the battery pack. The total resistance of the battery pack is given by Equation 1.

$$R_{\text{bat}(\text{tot})} = 2(R_{DS(\text{on})}) + 4R_{\text{cell}} \quad (\text{Equation 1})$$

The total pack resistance is typically determined by the system requirements. The total pack resistance directly determines how much voltage droop will occur during pulses in load current.

Another consideration is the forward-biased safe operating area of the MOSFET. During a short-circuit, the discharge current can easily reach 10–15 times the "C-rating" of the cells. The MOSFET must survive this current prior to the discharge MOSFET can be turned OFF. So having an FBSOA envelope that exceeds 20 amperes for 5 ms would be safe.

The Charge MOSFET circuit

The NE57605 uses an isolated charge MOSFET drive arrangement. This is to help keep ESD charges from entering the IC. The charge MOSFET is normally ON until turned off by the IC. The CF pin uses a current source to drive an external NPN transistor to turn OFF the charge FET. If a charge has poor "compliance" or the no load voltage of the charge can rise significantly above the rating of the battery pack. This condition causes the source of the charge FET to go very negative compared to the cell GND voltage after the charge FET opens. This design allows the charge FET gate drive to "float" down to this very negative voltage without upsetting the operation of the IC.

PACKING METHOD

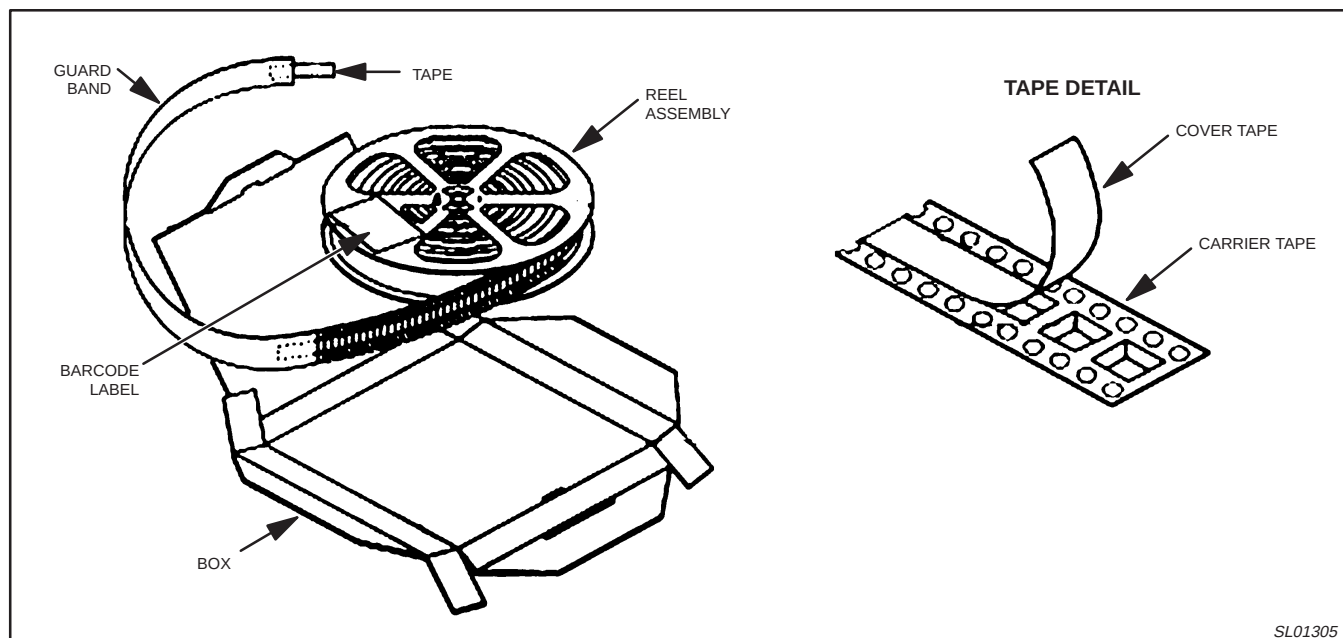
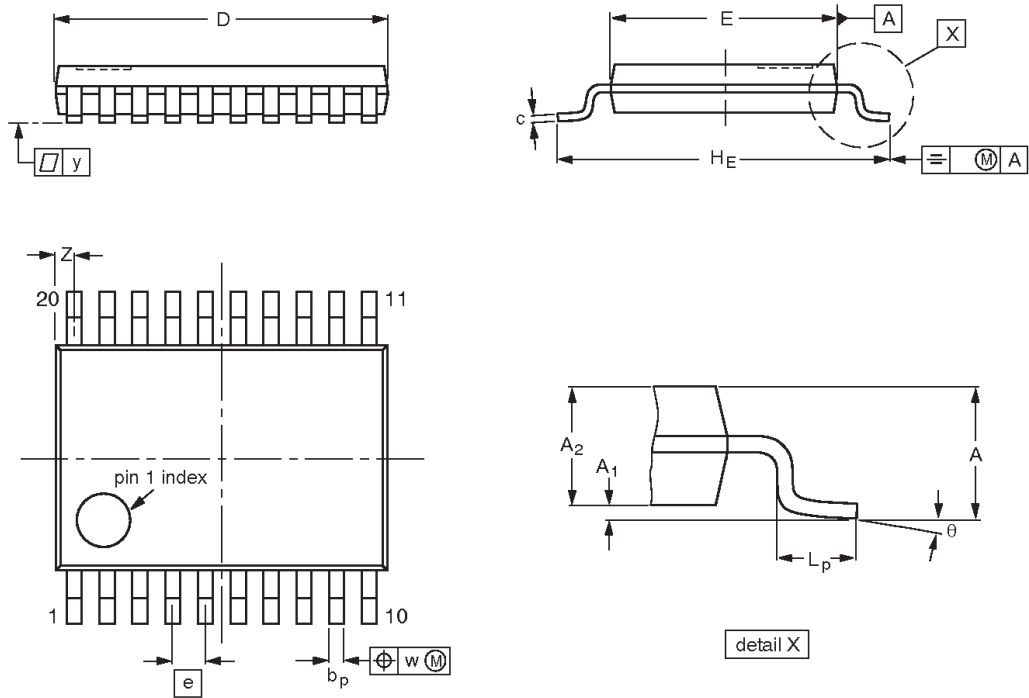


Figure 7. Tape and reel packing method.

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TSOP-20A: plastic thin shrink small outline package; 20 leads; body width 4.4 mm



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂		b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p			w	y	Z ⁽¹⁾	θ
mm	1.2	0.15 0.05	1.0		0.23 0.21	0.25 0.10	6.8 6.2	4.6 4.2	0.65	6.7 6.1	1.0	0.7 0.3			0.1	0.1	0.625 max.	10° 0°

- Notes
- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 - 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION
	IEC	JEDEC	EIAJ		
TSOP-20A					

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Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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For additional information please visit
<http://www.semiconductors.philips.com>. Fax: +31 40 27 24825

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sales.addresses@www.semiconductors.philips.com.

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