

January 2000 Revised May 2003

### NC7SB3257

# TinyLogic® UHS

# 2:1 Multiplexer/Demultiplexer Bus Switch

### **General Description**

The NC7SB3257 is a high performance, 2:1 NMOS passgate multiplexer/demultiplexer from Fairchild's Ultra High Speed Series of TinyLogic®. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance. The device is specified to operate over the 4.0 to 5.5V  $\rm V_{CC}$  operating range. The control input tolerates voltages up to 5.5V independent of the  $\rm V_{CC}$  operating range.

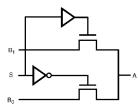
#### **Features**

- Space saving SC70 6-lead surface mount package
- Ultra small MicroPak™ leadless package
- Typical  $3\Omega$  switch resistance @ 5.0V V<sub>CC</sub>
- Minimal propagation delay through the switch
- Power down high impedance control input
- Zero bounce in flow through mode
- TTL compatible control input
- Overvoltage tolerance of control input to 7.0V
- Break before make enable circuitry

### **Ordering Code:**

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7SB3257P6X	MAA06A	B7B	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel
NC7SB3257L6X	MAC06A	B7	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel

### **Logic Symbol**



### **Pin Descriptions**

Pin Names	Description
A, B <sub>0</sub> , B <sub>1</sub>	Data Ports
S	Control Input

### **Function Table**

Input (S) Function					
L	B <sub>0</sub> Connected to A				
Н	B <sub>1</sub> Connected to A				

H = HIGH Logic Level L = LOW Logic Level

 $\label{eq:total_cond} \mbox{TinyLogio} \mbox{$\otimes$ is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{$\sim$}} \mbox{$is$ a trademark of Fairchild Semiconductor Corporation.} \\$ 

#### **Connection Diagrams**



#### Pin One Orientation Diagram



AAA = Product Code Top Mark - see ordering code

**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

#### Pad Assignments for MicroPak



(Top Thru View)

### **Absolute Maximum Ratings**(Note 1)

### **Recommended Operating** Conditions (Note 2)

Supply Voltage (V <sub>CC</sub> )	-0.5V to $+7.0V$
DC Switch Voltage (V <sub>S</sub> )	-0.5V to $+7.0V$
DC Output Voltage (V <sub>IN</sub> )	-0.5V to $+7.0V$
501 .51 1 0 .41	

DC Input Diode Current (I<sub>IK</sub>)  $@ (I_{IK}) V_{IN} < 0V$ 

DC Output Current (I<sub>OUT</sub>) 128 mA DC  $V_{CC}$  or Ground Current ( $I_{CC}/I_{GND}$ ) ±100 mA

Storage Temperature Range (T<sub>STG</sub>) -65°C to +150°C

Junction Lead Temperature under Bias (T<sub>J</sub>)

Lead Temperature (T<sub>L</sub>)

(Soldering, 10 seconds) +260°C 180 mW Power Dissipation (PD) @ +85°C

Supply Voltage Operating ( $V_{CC}$ ) 4.0V to 5.5V Control Input Voltage (VIN) 0V to V<sub>CC</sub> Switch Input Voltage (V<sub>IN</sub>) 0V to V<sub>CC</sub> Output Voltage (V<sub>OUT</sub>) 0V to  $V_{CC}$ -40°C to +85°C Operating Temperature (T<sub>A</sub>) Input Rise and Fall Time (t<sub>r</sub>, t<sub>f</sub>)

Control Input  $V_{CC} = 4.0V$  to 5.5V

0 ns/V to 5 ns/V +150°C Thermal Resistance ( $\theta_{JA}$ ) 350°C/W

> Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifi-

Note 2: Control input must be held HIGH or LOW, it must not float.

Note 3: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

### **DC Electrical Characteristics**

Symbol	Parameter	V <sub>CC</sub>	T <sub>A</sub> = -40°C to +85°C			Units	Conditions
Cymbol		(V)	Min	Тур	Max	Onics	Conditions
V <sub>IK</sub>	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18 \text{ mA}$
V <sub>IH</sub>	HIGH Level Input Voltage	4.5 – 5.5	2.0			V	
V <sub>IL</sub>	LOW Level Input Voltage	4.5 – 5.5			0.8		
I <sub>IN</sub>	Input Leakage Current	5.5			±1	μΑ	$0 \le V_{IN} \le 5.5V$
I <sub>OFF</sub>	OFF State Leakage Current	5.5			±1	μΑ	0 ≤ A, B ≤ V <sub>CC</sub>
R <sub>ON</sub>	Switch On Resistance (Note 4)	4.5		3	7	Ω	$V_{IN} = 0V$ , $I_{IN} = 64$ mA
		4.5		3	7	Ω	$V_{IN} = 0V$ , $I_{IN} = 30 \text{ mA}$
		4.5		6	15	Ω	$V_{IN} = 2.4V$ , $I_{IN} = 15 \text{ mA}$
		4.0		10	20	Ω	V <sub>IN</sub> = 2.4V, I <sub>IN</sub> = 15 mA
I <sub>CC</sub>	Quiescent Supply Current	5.5			10	μΑ	V <sub>IN</sub> = V <sub>CC</sub> or GND
							$I_{OUT} = 0$
$\Delta I_{CC}$	Increase in I <sub>CC</sub> Per Input (Note 5)	5.5		0.9	2.5	mA	$V_{IN} = 3.4V, I_{O} = 0$
							Control Input Only

-50 mA

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B Ports).

Note 5: Per TTL driven Input ( $V_{IN} = 3.4V$ , Control input only). A and B pins do not contribute to  $I_{CC}$ .

## **AC Electrical Characteristics**

Symbol	Parameter	v <sub>cc</sub>	$T_A = -40$ °C to $+85$ °C $C_L = 50$ pF, RU = RD $=500\Omega$			Units	Conditions	Figure
		(V)	Min	Тур	Max			Number
t <sub>PHL</sub>	Propagation Delay Bus to Bus (Note 6)	4.0 – 55			0.25	ns	V <sub>I</sub> = OPEN	Figures 1, 2
t <sub>PZL</sub>	Output Enable Time	4.5 – 5.5	1.8		6.5	ns	V <sub>I</sub> = 7V for t <sub>PZL</sub>	Figures
$t_{PZH}$		4.0	1.8		7.3	113	$V_I = 0V$ for $t_{PZH}$	1, 2
t <sub>PLZ</sub>	Output Disable Time	4.5 – 5.5	0.8		4.7		$V_I = 7V$ for $t_{PLZ}$	Figures
$t_{PHZ}$		4.0	0.8		5.3		V <sub>I</sub> = 0V for t <sub>PHZ</sub>	1, 2
t	Break Before Make Time	4.5 – 5.5	0.5			ns		Figure 3
t <sub>B-M</sub>	(Note 7)	4.0	0.5			115		1 igule 3

Note 6: This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

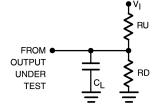
Note 7: Guaranteed by design.

## Capacitance (Note 8)

Symbol	Parameter	Тур	Max	Units	Conditions
C <sub>IN</sub>	Control Pin Input Capacitance	2.3		pF	V <sub>CC</sub> = 0V
C <sub>IO-B</sub>	B Port OFF Capacitance	5.7		pF	V <sub>CC</sub> = 5.0V
C <sub>IO-A</sub>	A Port ON Capacitance	16		pF	V <sub>CC</sub> = 5.0V

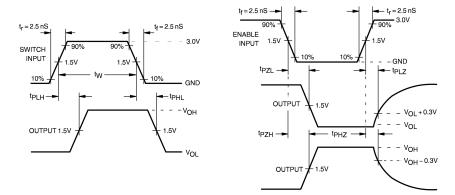
Note 8: Capacitance is characterized but not tested.

# AC Loading and Waveforms



Note: Input Driven by  $50\Omega$  source terminated in  $50\Omega$ Note:  $C_L$  includes load and stray capacitance Note: Input PRR = 1.0 MHz;  $t_W$  = 500 ns

FIGURE 1. AC Test Circuit



Input = AC Waveform; PRR = Variable; Duty Cycle = 50%

FIGURE 2. AC Waveforms

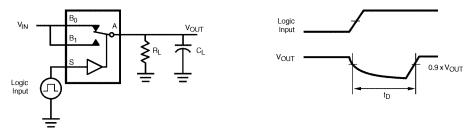


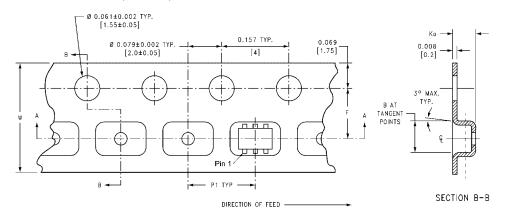
FIGURE 3. Break Before Make Interval Timing

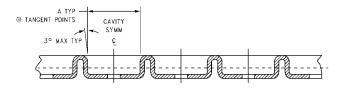
# **Tape and Reel Specification**

TAPE FORMAT for SC70

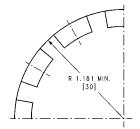
= . •				
Package	Tape	Number	Cavity	Cover Tape
Designator	Section	Cavities	Status	Status
	Leader (Start End)	125 (typ)	Empty	Sealed
P6X	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

#### TAPE DIMENSIONS inches (millimeters)





SECTION A-A



BEND RADIUS NOT TO SCALE

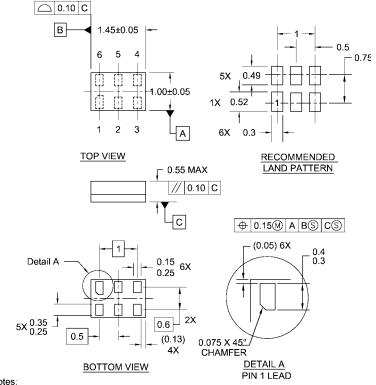
Package	Tape Size	DIM A	DIM B	DIM F	DIM K <sub>o</sub>	DIM P1	DIM W
SC70-6	8 mm	0.093	0.096	$0.138 \pm 0.004$	$0.053 \pm 0.004$	0.157	$0.315 \pm 0.004$
	0 111111	(2.35)	(2.45)	$(3.5 \pm 0.10)$	$(1.35 \pm 0.10)$	(4)	$(8 \pm 0.1)$

#### Tape and Reel Specification (Continued) TAPE FORMAT for MicroPak Package Tape Number Cavity Cover Tape Designator Section Cavities Status Status Leader (Start End) Sealed 125 (typ) Empty L6X Carrier 5000 Filled Sealed Trailer (Hub End) 75 (typ) Empty Sealed 4.00 1.75±0.10 В 5° MAX. 8.00 <sup>+0.30</sup> -0.10 3.50±0.05 1.15±0.05 В -ø 0.50 ±0.05 SECTION B-B SCALE:10X 0.254±0.020 C 0.70±0.05 SECTION A-A SCALE:10X **REEL DIMENSIONS** inches (millimeters) TAPE SLOT DETAIL X **DETAIL X** SCALE: 3X D N W1 W2 W3 Tape В С 7.0 0.059 0.512 0.795 2.165 0.331 + 0.059/-0.000 0.567 W1 + 0.078/-0.039 8 mm (1.50) (177.8)(13.00)(20.20)(55.00)(8.40 + 1.50 / -0.00)(14.40)(W1 + 2.00/-1.00)

# Physical Dimensions inches (millimeters) unless otherwise noted 0.65 1.9 B- 1.25±0.10 2.10±0.10 0.4 min 0.20 +0.10 LAND PATTERN RECOMMENDATION ◆ max 0.1 **②** SEE DETAIL A 0.9±.10 0.95±0.15 max 0.1 R0.14 GAGE PLANE R0.10 0.20 -- 0.425 NOMINAL DETAIL A NOTES: A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88. MAA06ARevC B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. C. DIMENSIONS ARE IN MILLIMETERS. 6-Lead SC70, EIAJ SC88, 1.25mm Wide

Package Number MAA06A

### Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



#### Notes:

- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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