SaRonix

Crystal Clock Oscillator

1.8V, LVCMOS, Tri-State

Technical Data

NTH Series

ACTUAL SIZE

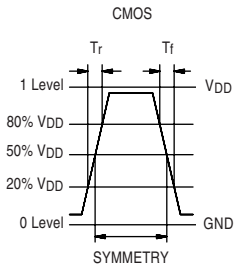
Description

A 1.8V LVDS, crystal controlled, low current, low jitter oscillator with precise rise and fall times demanded in networking applications, such as Gigabit Ethernet and Fibre Channel. The Tri-State function enables the output to go high impedance. Device is packaged in an 8-pin DIP compatible resistance welded, all metal grounded case, to reduce EMI.

Applications & Features

- Fibre Channel
- Gigabit Ethernet
- 32 Bit Microprocessors
- Tri-State output standard
- LVCMOS / HCMOS compatible
- Grounded, all metal half size case

Output Waveform



Frequency Range:	20 MHz to 70 MHz
Frequency Stability:	±50 or ±100 ppm over all conditions: calibration tolerance, operating temperature, input voltage change, load change, aging, shock and vibration.
Temperature Range:	
Operating:	0 to +70°C
Storage:	-55 to +125°C
Supply Voltage:	
Recommended Operating:	1.8V ±5%
Supply Current:	6mA max 20 to 50 MHz, output enabled 10mA max 50+ to 70MHz, output enabled 10µA max 20 to 70MHz, output disabled
Output Drive:	
Symmetry:	45/55% max @ 50% V_{DD}
Rise and Fall Times:	2.5ns max
Logic 0:	10% V_{DD} max
Logic 1:	90% V_{DD} min
Load:	15 pF max
Period Jitter RMS:	8ps max
Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-883, Method 2004, Conditions B2
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C
Environmental:	
Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

Tri-State

Logic Table:

Pin 1 Input	Pin 5 Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Control Characteristics:	
Output:	Oscillation @ V_{IN}, 2.2V min
Output:	High Impedance @ V_{IN}, 0.8V max
Internal Pullup Resistance:	50KΩ min
Control Input:	Disable Output Delay: 100ns max
Control Input:	Enable Output Delay: 10ms max

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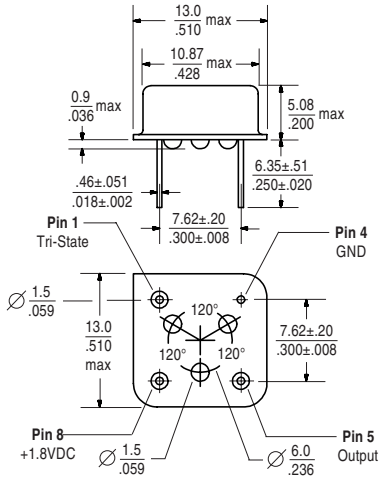
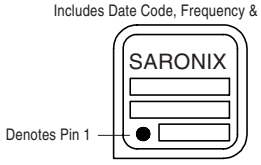
Package Details

HALF SIZE PACKAGE



Marking Format **

Includes Date Code, Frequency & Model



** Exact locations of items may vary

Scale: None (Dimensions in $\frac{mm}{inches}$)

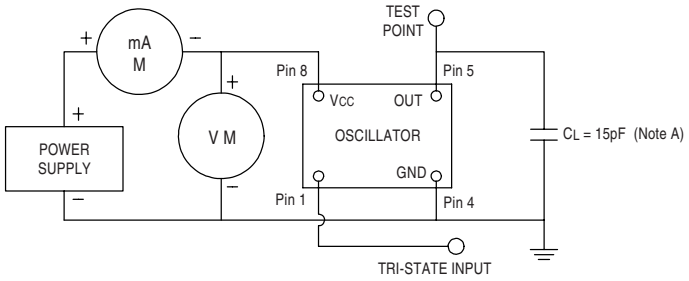
Part Numbering Guide

NTH A 3 9 B 2 – 50.0000

- **Frequency (MHz)**: 50.0000
- **Series**: NTH
- **Supply Voltage**: 2 = 1.8V
- **Symmetry / Temperature Range**: A = 45/55%, 0 to +70°C, HCMOS/LVCMOS
- **Stability Tolerance**: B = ±50 ppm, C = ±100 ppm
- **Frequency Range**: 3 = 20 to 50 MHz, 6 = 50+ to 70 MHz
- **Package**: 9 = Half Size, Thru-Hole

Example PN: NTHA39B2 - 60.0000

Test Circuits



NOTE A: C_L includes probe and fixture capacitance

HCMOS (Used at SaRonix)

All specifications are subject to change without notice.

DS-206 REV A