

NB100ELT23L

3.3V Dual Differential LVPECL to LVTTTL Translator

The NB100ELT23L is a dual differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used, only +3.3 V and ground are required. The small outline 8-lead package and the dual gate design of the ELT23L makes it ideal for applications which require the translation of a clock and a data signal.

The ELT23L is available in only the ECL 100K standard. Since there are no LVPECL outputs or an external V_{BB} reference, the ELT23L does not require both ECL standard versions. The LVPECL inputs are differential. Therefore, the NB100ELT23L can accept any standard differential LVPECL input referenced from a V_{CC} of +3.3 V.

- 2.1 ns Typical Propagation Delay
- Maximum Operating Frequency > 275 MHz
- 24 mA LVTTTL Outputs
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at GND



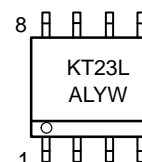
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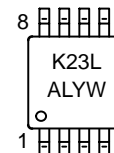
MARKING DIAGRAMS*



SO-8
D SUFFIX
CASE 751



TSSOP-8
DT SUFFIX
CASE 948R



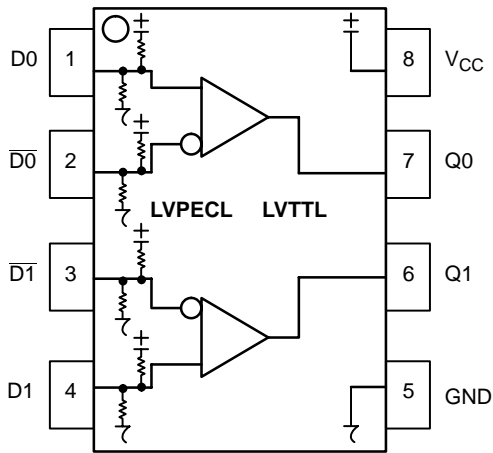
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note
AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NB100ELT23LD	SO-8	98 Units/Rail
NB100ELT23LDR2	SO-8	2500 Tape & Reel
NB100ELT23LDT	TSSOP-8	100 Units/Rail
NB100ELT23LDTR2	TSSOP-8	2500 Tape & Reel

NB100ELT23L



PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	LVTTTL Outputs
D0**, D1** D0**, D1**	Differential LVPECL Inputs
V _{CC}	Positive Supply
GND	Ground

** Pins will default to $V_{CC}/2$ when left open.

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k Ω
Internal Input Pullup Resistor	37.5 k Ω
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 1.2 kV > 150 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34 UL 94 V-0 @ 1.25 in
Transistor Count	91 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	Power Supply	GND = 0 V		3.8	V
V _I	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	3.8	V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44	°C/W
T _{sol}	Wave Solder	<2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

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PECL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CCH}	Power Supply Current (Outputs set to HIGH)	10	14	20	10	15	20	10	15	20	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)	15	19	25	15	19	25	15	20	25	mA
V_{IH}	Input HIGH Voltage	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage	1355		1675	1355		1675	1355		1675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current			0.5			0.5			0.5	μA

NOTE: Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

3. All values vary 1:1 with V_{CC} .

4. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TTL DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$, $GND = 0.0\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 5)	$I_{OH} = -3.0\text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage (Note 5)	$I_{OL} = 24\text{ mA}$			0.5	V
I_{OS}	Output Short Circuit Current		-180		-50	mA

NOTE: Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.

5. All loading with 500 Ω to GND.

AC CHARACTERISTICS $V_{CC} = 3.3\text{ V} \pm 5\%$, $GND = 0.0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency	160			160			160			MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 7) $C_L = 20\text{ pF}$	1.5	2.1	2.75	1.5	2.1	2.75	1.5	2.1	2.75	ns
$t_{SK+ +}$, $t_{SK- -}$, t_{SKPP}	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 8)			60 25 500			60 25 500			60 25 500	ps
t_{JITTER}	Cycle-to-Cycle Jitter		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times $C_L = 20\text{ pF}$ (1.0 V – 2.0 V) Q	500 300		1300 1000	500 300		1300 1000	500 300		1300 1000	ps

6. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 500 Ω to GND, $C_L = 20\text{ pF}$.

7. Reference ($V_{CC} = 3.3\text{ V} \pm 5\%$; $GND = 0\text{ V}$)

8. Skews are measured between outputs under identical conditions.

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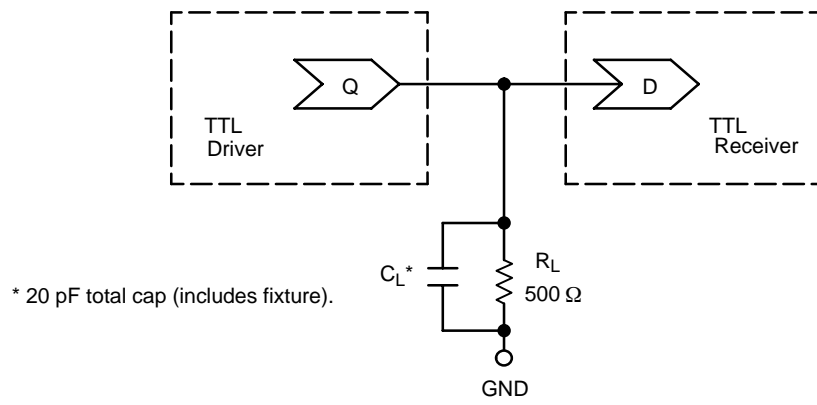


Figure 2. TTL Output Loading Used for Device Evaluation

Resource Reference of Application Notes

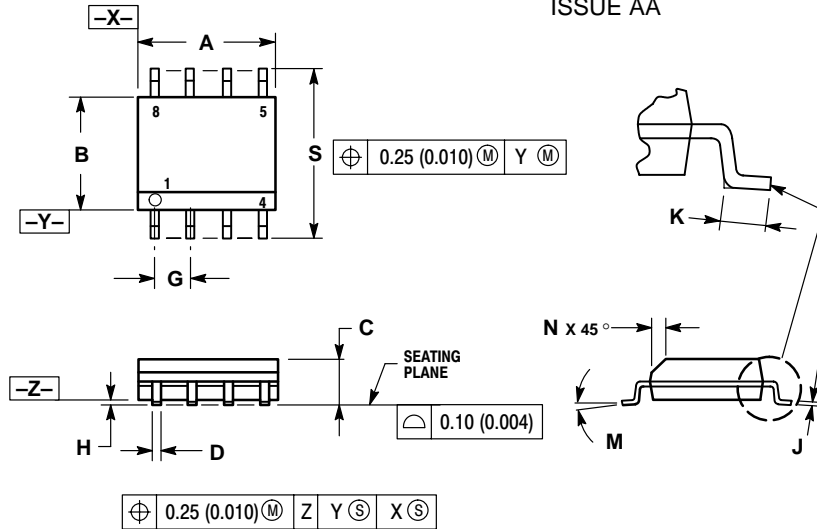
- AN1404** – ECLinPS Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

NB100ELT23L

PACKAGE DIMENSIONS

SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE AA



NOTES:

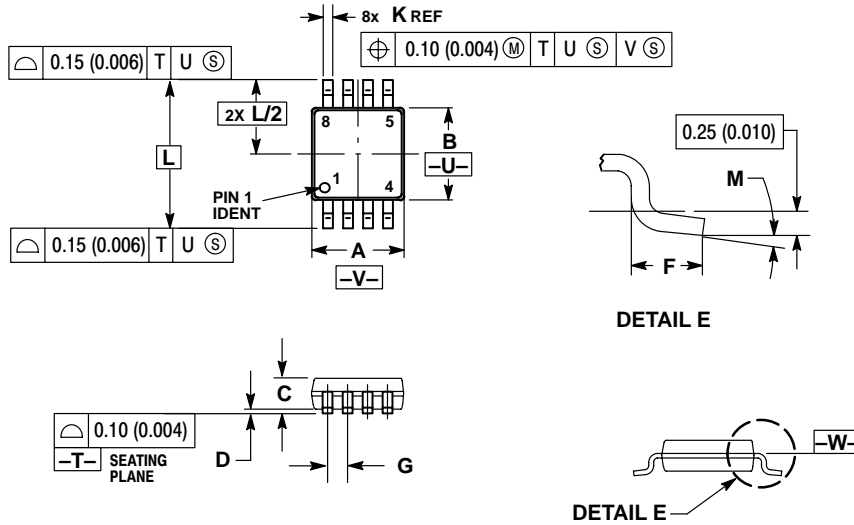
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

NB100ELT23L

PACKAGE DIMENSIONS

TSSOP-8
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948R-02
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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