NBSG16VS

2.5V/3.3V SiGe Differential Receiver/Driver with Variable Output Swing

The SG16VS is a Silicon Germanium differential receiver/driver. The device is functionally equivalent to the EP16VS device with much higher bandwidth and lower EMI capabilities. This device may be used for applications driving VCSEL lasers.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), TTL, CMOS, CML, or LVDS. The output amplitude is varied by applying a voltage to the V_{CTRL} input pin. Outputs are variable swing ECL from 100 mV to 750 mV amplitude, optimized for operation from $V_{CC} – V_{EE}$ = 3.0 V to 3.465 V.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used for single–ended NECL or PECL inputs and the V_{MM} pin is used for CMOS inputs. For single–ended input operation, the unused differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

- Maximum Input Clock Frequency up to 12 GHz (See Figure 7)
- 40 ps Typical Rise and Fall Times ($V_{CTRL} = V_{CC} – 1$ V)
- 120 ps Typical Propagation Delay ($V_{CTRL} = V_{CC} – 1$ V)
- Variable Swing PECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- Variable Swing NECL Output with NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.465 V
- Output Level (100 mV to 750 mV Peak–to–Peak Output; $V_{CC} – V_{EE}$ = 3.0 V to 3.465 V), Differential Output Only
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V EP Devices
- V_{BB} and V_{MM} Reference Voltage Output

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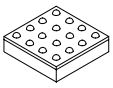
MARKING DIAGRAM*



FCBGA–16
BA SUFFIX
CASE 489

L = Wafer Lot
Y = Year
W = Work Week

*For additional information, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG16VSBA	4x4 mm FCBGA–16	100 Units/Tray
NBSG16VSBAR2	4x4 mm FCBGA–16	500/Tape & Reel

Board	Description
SG16VSEVB	NBSG16VSBA Evaluation Board

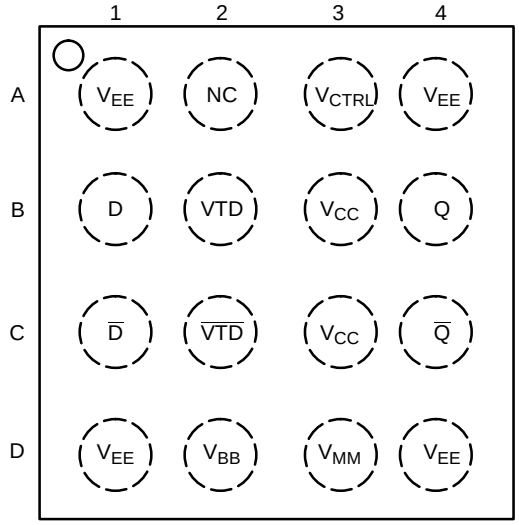


Figure 1. Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
D*, $\overline{D}$**	ECL, TTL, CMOS, CML, LVDS Compatible Inputs
Q, $\overline{Q}$	RSECL Data Outputs
VTD, $\overline{VTD}$	50 Ω Internal Input Termination Resistor
V_{MM}	CMOS Reference Voltage Output, $\frac{V_{CC} - V_{EE}}{2}$
V_{CTRL}***	Output Amplitude Swing Control
V_{BB}	ECL Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
NC	No Connect

* Pin will default low when left open.
** Pin will default to a slightly higher potential than D when both are left open.
*** Bypass pin to V_{CC} (0.1 μF capacitor).

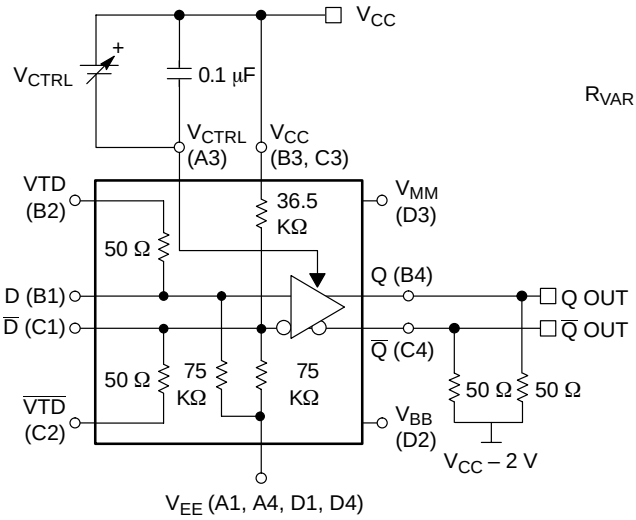


Figure 2. Logic Diagram/ Voltage Source Implementation

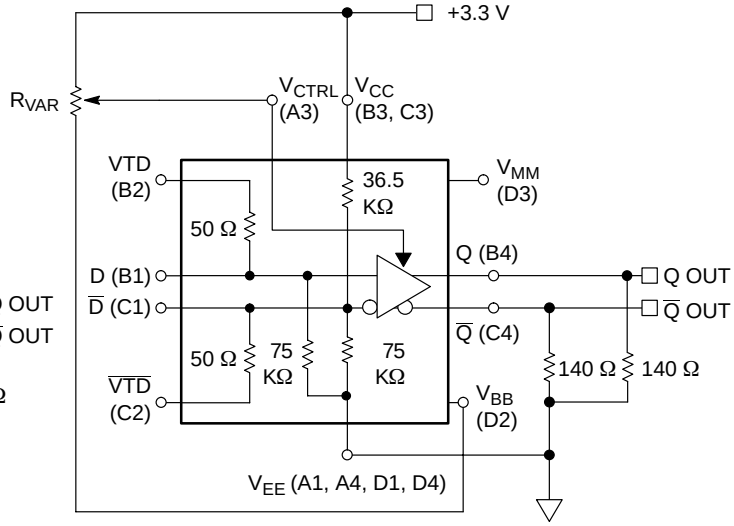


Figure 3. Alternative Voltage Source Implementation

INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and $\overline{VTD}$ to V_{CC}
LVDS	Connect VTD and $\overline{VTD}$ Together
AC–COUPLED	Bias VTD and $\overline{VTD}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	See Text on Page 1. Unused Differential Input Switching Voltage Reference Range is from V_{EE} + 1125 mV to V_{CC} – 75 mV

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (D, $\overline{D}$)	75 kΩ
Internal Input Pullup Resistor ($\overline{D}$)	36.5 kΩ
ESD Protection Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	Level 3
Flammability Rating	UL 94 V–0 @ 0.125 in
Oxygen Index	28 to 34
Transistor Count	192
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		–3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 –3.6	V V
V_{INPP} (IN–IN)	Differential Input Voltage (ID – $\overline{D}$I)	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\lvert V_{CC} - V_{EE} \rvert$	V V
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) (Note 3)	0 LFPM 500 LFPM	16 FCBGA 16 FCBGA	108 86	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	2S2P (Note 3)	16 FCBGA	5	°C/W
T_{sol}	Wave Solder	< 15 sec.		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard 51–6 multilayer board – 2S2P (2 signal, 2 power).

DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 4)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	18	25	32	18	25	32	18	25	32	mA
V_{OH}	Output HIGH Voltage (Note 5)	1315	1440	1565	1305	1430	1555	1305	1430	1555	mV
V_{OL}	Output LOW Voltage (Note 5) (Max Swing) (V_{CTRL} = V_{CC} – 600 mV)	645 1090	765 1210	885 1330	605 1035	725 1155	845 1275	600 1010	720 1130	840 1250	mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 7 and 8)	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 7 and 9)	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	mV
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{MM}	CMOS Output Voltage Reference (V_{CC} – V_{EE})/2	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

DC CHARACTERISTICS, INPUT WITH VARIABLE PECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 10)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	20	27	34	20	27	34	20	27	34	mA
V_{OH}	Output HIGH Voltage (Note 5)	2095	2220	2345	2085	2210	2335	2075	2200	2325	mV
V_{OL}	Output LOW Voltage (Note 5) (Max Swing) (V_{CTRL} = V_{CC} – 600 mV)	1275 1750	1395 1870	1515 1990	1285 1730	1405 1850	1525 1970	1295 1715	1415 1835	1535 1955	mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 7 and 8)	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 7 and 9)	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	mV
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		3.3	1.2		3.3	1.2		3.3	V
V_{MM}	CMOS Output Voltage Reference (V_{CC} – V_{EE})/2	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to –0.965 V.
5. All loading with 50 Ω to V_{CC}–2.0 volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
7. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}. $V_{THR(MIN)}$ = V_{IHCMR} + 75 mV. $V_{THR(MAX)}$ = V_{IHCMR} – 75 mV.
8. V_{IH} cannot exceed V_{CC}.
9. V_{IL} always ≥ V_{EE}.
10. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.165 V.

*Typicals used for testing purposes.

DC CHARACTERISTICS, NECL INPUT WITH VARIABLE NECL OUTPUT V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V (Note 11)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	20	27	34	20	27	34	20	27	34	mA
V_{OH}	Output HIGH Voltage (Note 12) –3.465 V ≤ V_{EE} ≤ –3.0 V –3.0 V < V_{EE} ≤ –2.375 V	 –1205 –1185	 –1080 –1060	 –955 –935	 –1215 –1195	 –1090 –1070	 –965 –945	 –1225 –1195	 –1100 –1070	 –975 –945	mV
V_{OL}	Output LOW Voltage (Note 12) –3.465 V ≤ V_{EE} ≤ –3.0 V (Max Swing) (V_{CTRL} = V_{CC} – 600 mV) –3.0 V < V_{EE} ≤ –2.375 V (Max Swing) (V_{CTRL} = V_{CC} – 600 mV)	 –2000 –1560 –1855 –1410	 –1910 –1440 –1620 –1215	 –1820 –1320 –1290 –1000	 –1990 –1580 –1895 –1460	 –1900 –1460 –1705 –1290	 –1810 –1340 –1425 –1100	 –1980 –1595 –1900 –1490	 –1890 –1475 –1730 –1330	 –1800 –1355 –1470 –1150	mV mV mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 14 and 15)	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 14 and 16)	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	mV
V_{BB}	NECL Output Voltage Reference	–1420	–1360	–1300	–1420	–1360	–1300	–1420	–1360	–1300	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
V_{MM}	CMOS Output Voltage Reference (Note 17)	V_{MMT} – 150	V_{MMT}	V_{MMT} + 150	V_{MMT} – 150	V_{MMT}	V_{MMT} + 150	V_{MMT} – 150	V_{MMT}	V_{MMT} + 150	mV
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	50		25	50		25	50	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}.
12. All loading with 50 Ω to V_{CC} –2.0 volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL}.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
14. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}. $V_{THR(MIN)}$ = V_{IHCMR} + 75 mV. $V_{THR(MAX)}$ = V_{IHCMR} – 75 mV.
15. V_{IH} cannot exceed V_{CC}.
16. V_{IL} always ≥ V_{EE}.
17. V_{MM} typical = $|V_{CC}–V_{EE}| / 2 + V_{EE} = V_{MMT}$.

*Typicals used for testing purposes.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.465 V to –3.0 V or V_{CC} = 3.0 V to 3.465 V; V_{EE} = 0 V

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 7) (Note 18)	10.7 (Note 21)	12		10.7 (Note 21)	12		10.7 (Note 21)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	(V_{CTRL} = V_{CC} – 2 V) D → Q, $\overline{Q}$	100	125	145	100	125	145	100	125	145	
	(V_{CTRL} = V_{CC} – 1 V) D → Q, $\overline{Q}$	100	120	140	100	120	140	100	120	140	
t_{SKEW}	Duty Cycle Skew (Note 19)		3	10		3	10		3	10	ps
t_{JITTER}	Cycle–to–Cycle Jitter (RMS) (See Figure 7) (Note 18)		0.8	< 2		0.8	< 2		0.8	< 2	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 20)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% – 80%)										ps
	(V_{CTRL} = V_{CC} – 2 V) Q, $\overline{Q}$	30	45	55	30	45	55	30	45	55	
	(V_{CTRL} = V_{CC} – 1 V) Q, $\overline{Q}$	30	40	50	30	40	50	30	40	50	

18. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}–2.0 V.
19. t_{SKEW} = $|t_{PLH} – t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 9.
20. $V_{INPP(MAX)}$ cannot exceed V_{CC} – V_{EE} (applicable only when V_{CC} – V_{EE} < 2600 mV).
21. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} – 2 V. Minimum output amplitude guarantee of 100 mV (see Output P–P Spec in Figure 7).

AC CHARACTERISTICS V_{CC} = 0 V; –3.0 V < V_{EE} ≤ –2.375 V or 2.375 V ≤ V_{CC} < 3.0 V; V_{EE} = 0 V

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 8) (Note 22)	10.7 (Note 25)	12		10.7 (Note 25)	12		10.7 (Note 25)	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential										ps
	(V_{CTRL} = V_{CC} – 2 V) D → Q, $\overline{Q}$	100	125	145	100	125	145	100	125	145	
	(V_{CTRL} = V_{CC} – 1 V) D → Q, $\overline{Q}$	100	120	140	100	120	140	100	120	140	
t_{SKEW}	Duty Cycle Skew (Note 23)		3	10		3	10		3	10	ps
t_{JITTER}	Cycle–to–Cycle Jitter (RMS) (See Figure 8) (Note 22)		0.9	< 3		0.9	< 3		0.9	< 3	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 24)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% – 80%)										ps
	(V_{CTRL} = V_{CC} – 2 V) Q, $\overline{Q}$	25	50	70	25	50	70	25	50	70	
	(V_{CTRL} = V_{CC} – 1 V) Q, $\overline{Q}$	22	45	60	22	45	60	22	45	60	

22. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}–2.0 V.
23. t_{SKEW} = $|t_{PLH} – t_{PHL}|$ for a nominal 50% differential clock input waveform. See Figure 9.
24. $V_{INPP(MAX)}$ cannot exceed V_{CC} – V_{EE} (applicable only when V_{CC} – V_{EE} < 2600 mV).
25. Conditions include input amplitude of 500 mV and V_{CTRL} = V_{CC} – 2 V. Minimum output amplitude guarantee of 100 mV (see Output P–P Spec in Figure 8).

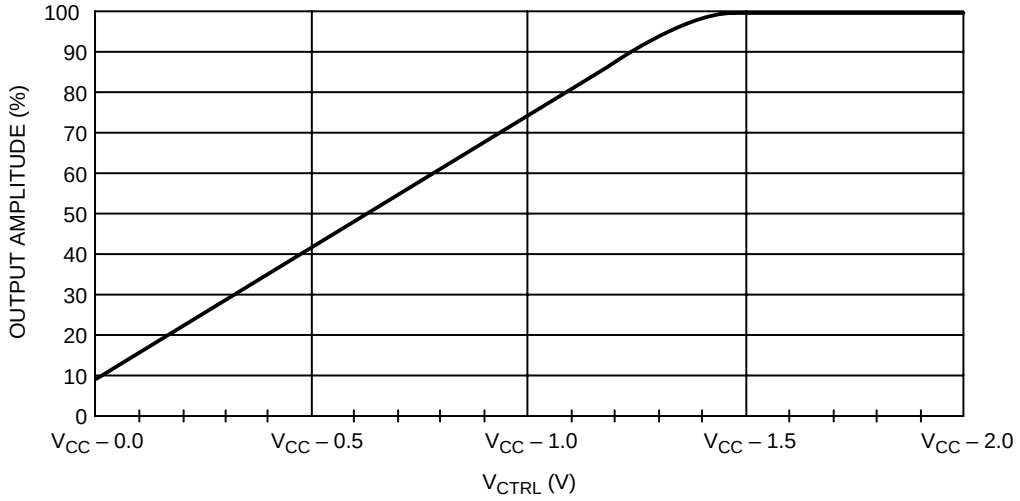


Figure 4. Output Amplitude % vs. V_{CTRL} (pin #A3)

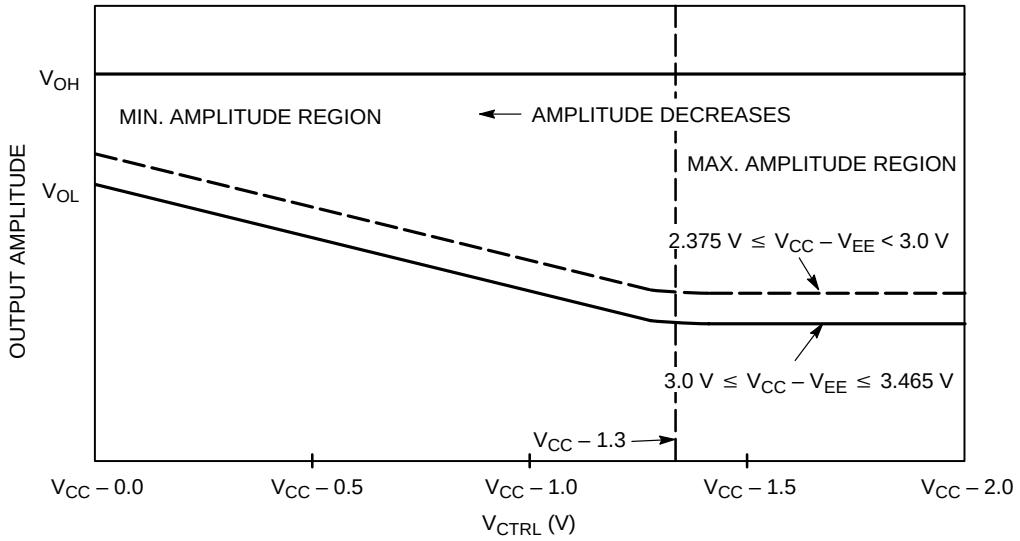


Figure 5. Output Amplitude vs. V_{CTRL} (pin #A3)

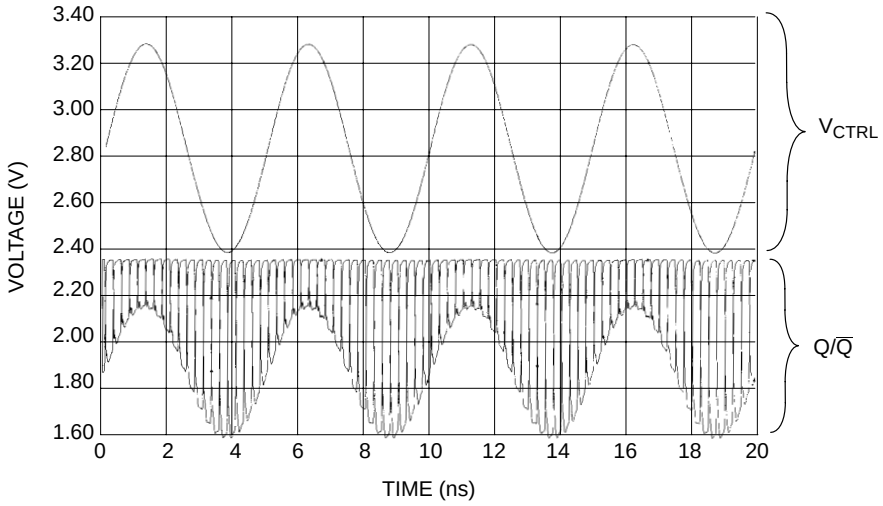


Figure 6. Output Response Under Amplitude Modulation of V_{CTRL} (Conditions Include $V_{CC} - V_{EE}$ = 3.3 V at 25°C, f_{IN} (V_{CTRL}) = 200 MHz, and f_{IN} (D, $\overline{D}$) = 2 GHz)

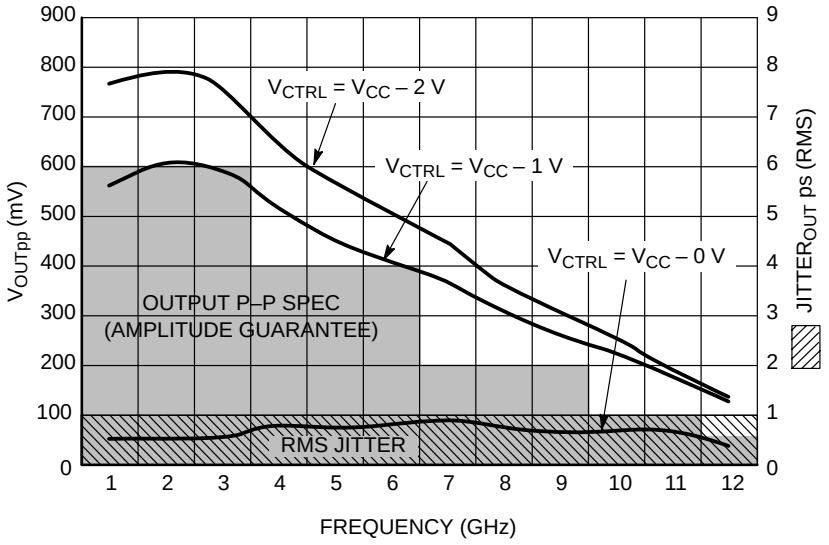


Figure 7. V_{OUT}/Jitter vs. Frequency (V_{CC} − V_{EE} = 3.3 V @ 25°C)

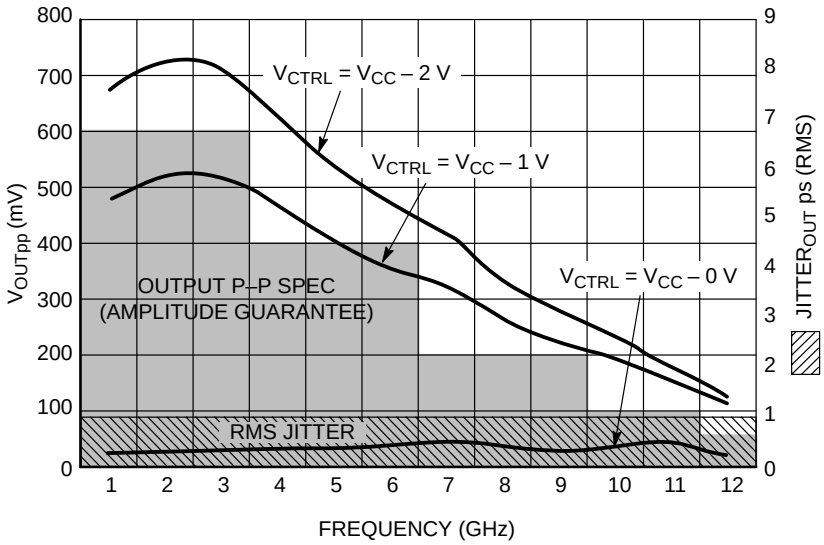


Figure 8. V_{OUT}/Jitter vs. Frequency (V_{CC} − V_{EE} = 2.5 V @ 25°C)

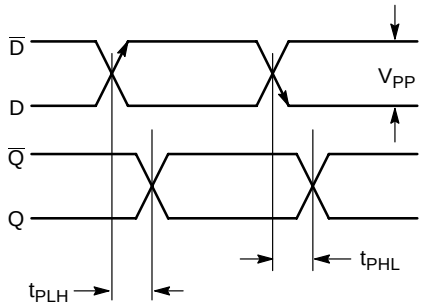


Figure 9. AC Reference Measurement

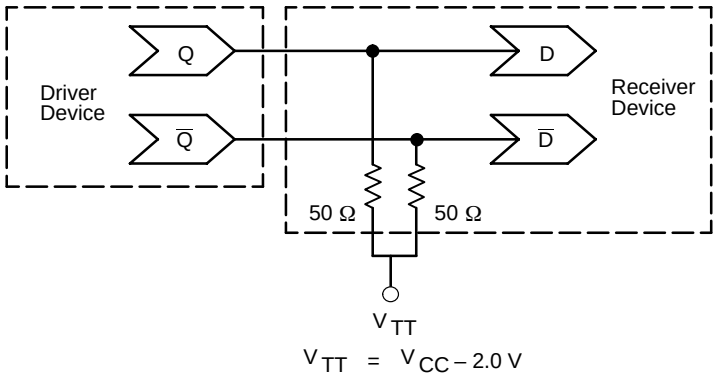
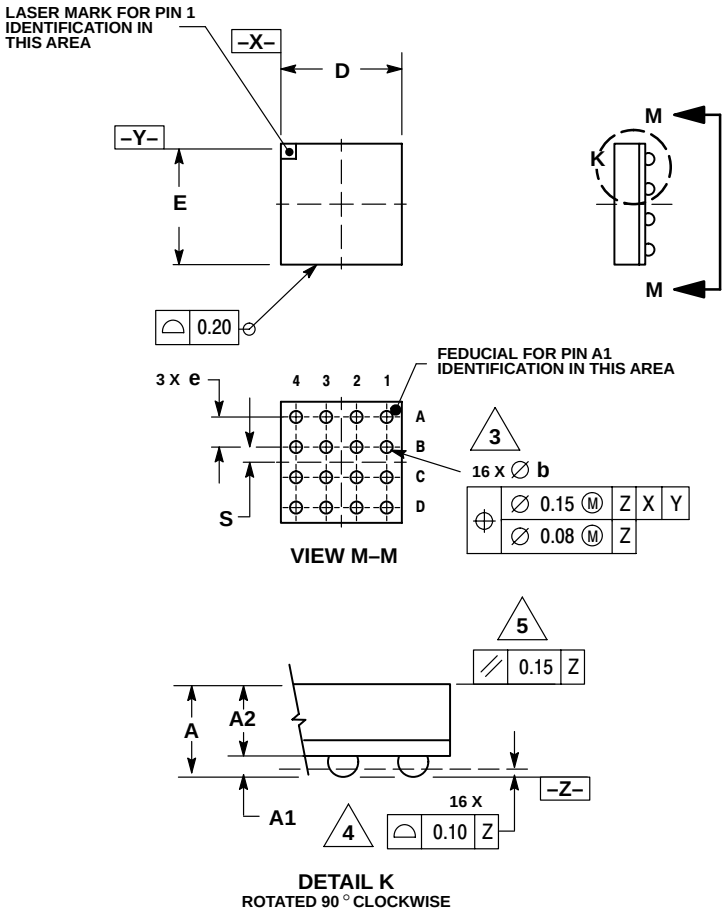


Figure 10. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA–16
BA SUFFIX
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489–01
ISSUE O



NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Notes

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