DATA SHEET

MOS FIELD EFFECT TRANSISTOR

NP80N03CLE, NP80N03DLE, NP80N03ELE

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

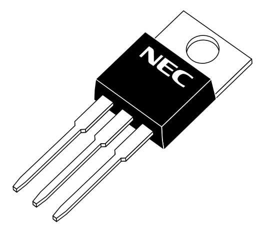
FEATURES

- Channel Temperature 175 degree rated
- Super Low On-state Resistance
  $R_{DS(on)1}$ = 7.0 mΩ MAX. (V_{GS} = 10 V, I_D = 40 A)
  $R_{DS(on)2}$ = 9.0 mΩ MAX. (V_{GS} = 5 V, I_D = 40 A)
- Low C_{iss} : C_{iss} = 2600 pF TYP.
- Built-in Gate Protection Diode

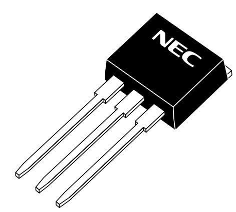
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP80N03CLE	TO-220AB
NP80N03DLE	TO-262
NP80N03ELE	TO-263

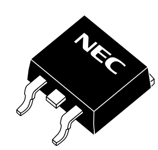
(TO-220AB)



(TO-262)



(TO-263)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	30	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC) Note1	$I_{D(DC)}$	±80	A
Drain Current (Pulse) Note2	$I_{D(pulse)}$	±320	A
Total Power Dissipation (T_A = 25°C)	P_T	1.8	W
Total Power Dissipation (T_C = 25°C)	P_T	120	W
Single Avalanche Current Note3	I_{AS}	50 / 40 / 9	A
Single Avalanche Energy Note3	E_{AS}	2.5 / 160 / 400	mJ
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C

Notes 1. Calculated constant current according to MAX. allowable channel temperature.

2. PW ≤ 10 μs, Duty cycle ≤ 1 %

3. Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V→0 V (see Figure 4.)

THERMAL RESISTANCE

Channel to Case	$R_{th(ch-C)}$	1.25	°C/W
Channel to Ambient	$R_{th(ch-A)}$	83.3	°C/W

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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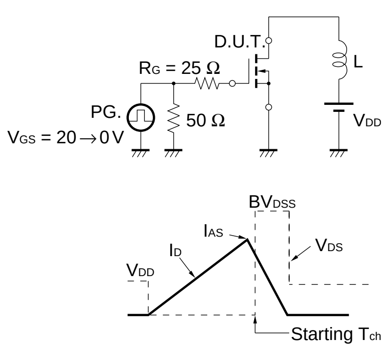
The mark ★ shows major revised points.

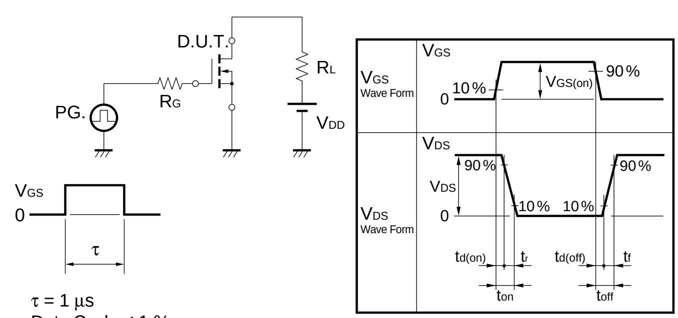
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 40 A		5.3	7.0	mΩ
	$R_{DS(on)2}$	V_{GS} = 5 V, I_D = 40 A		6.8	9.0	mΩ
	$R_{DS(on)3}$	V_{GS} = 4.5 V, I_D = 40 A		7.5	11	mΩ
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 40 A	20	41		S
Drain Leakage Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±10	μA
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		2600	3900	pF
Output Capacitance	C_{oss}			590	890	pF
Reverse Transfer Capacitance	C_{rss}			270	490	pF
Turn-on Delay Time	$t_{d(on)}$	I_D = 40 A, $V_{GS(on)}$ = 10 V, V_{DD} = 15 V,		20	44	ns
Rise Time	t_r	R_G = 1 Ω		12	31	ns
Turn-off Delay Time	$t_{d(off)}$			60	120	ns
Fall Time	t_f			14	35	ns
Total Gate Charge 1	Q_{G1}	I_D = 80 A, V_{DD} = 24 V, V_{GS} = 10 V		48	72	nC
Total Gate Charge 2	Q_{G2}	I_D = 80 A, V_{DD} = 24 V, V_{GS} = 5 V		28	42	nC
Gate to Source Charge	Q_{GS}			10		nC
Gate to Drain Charge	Q_{GD}			14		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 80 A, V_{GS} = 0 V		1.0		V
Reverse Recovery Time	t_{rr}	I_F = 80 A, V_{GS} = 0 V, di/dt = 100A/μs		34		ns
Reverse Recovery Charge	Q_{rr}			22		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

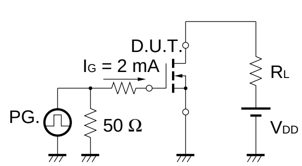


TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1 %

TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

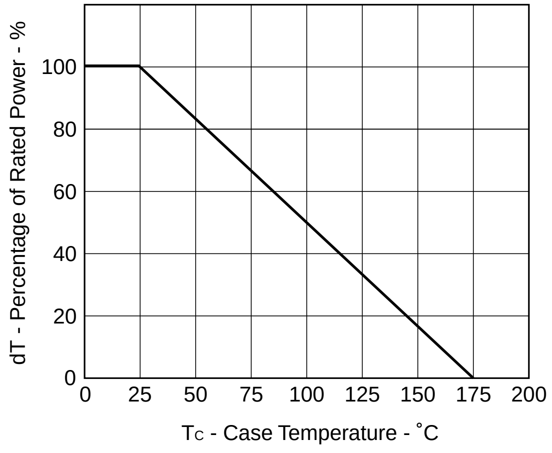
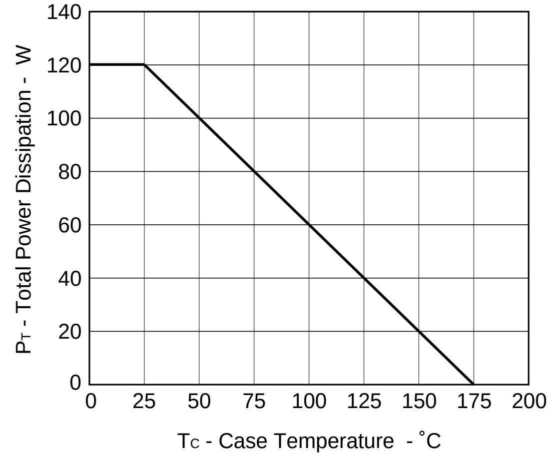


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



★ Figure3. FORWARD BIAS SAFE OPERATING AREA

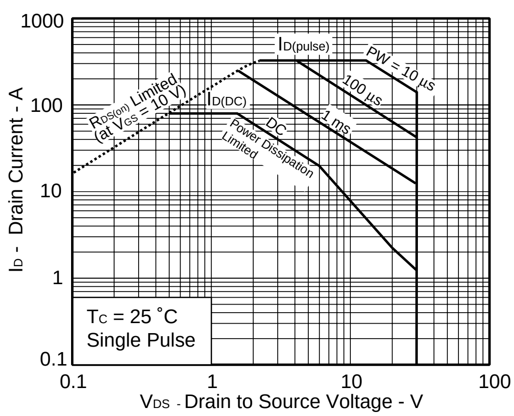


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

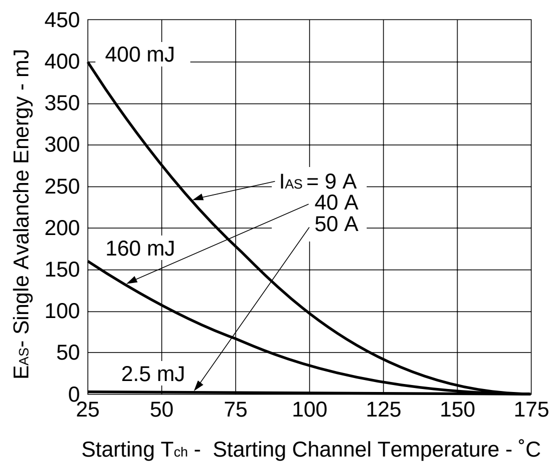


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

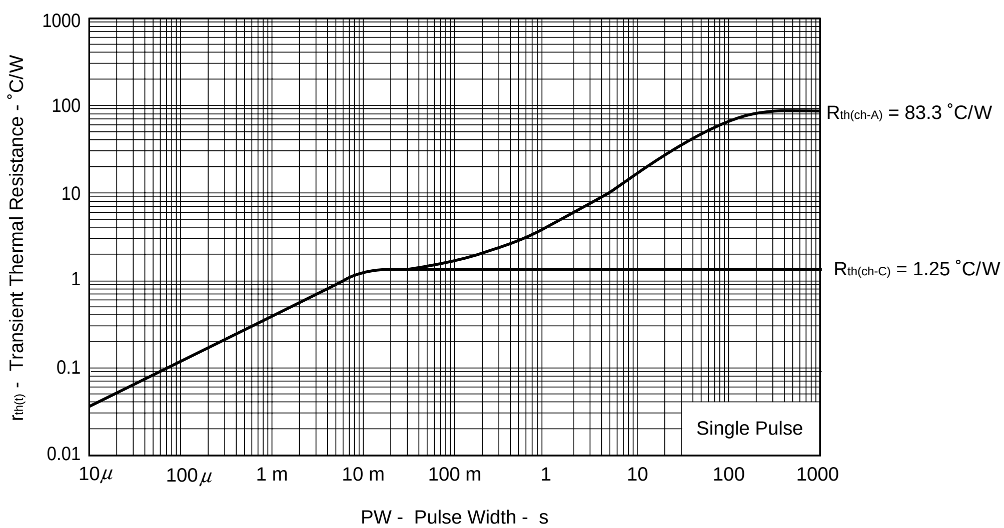


Figure6. FORWARD TRANSFER CHARACTERISTICS

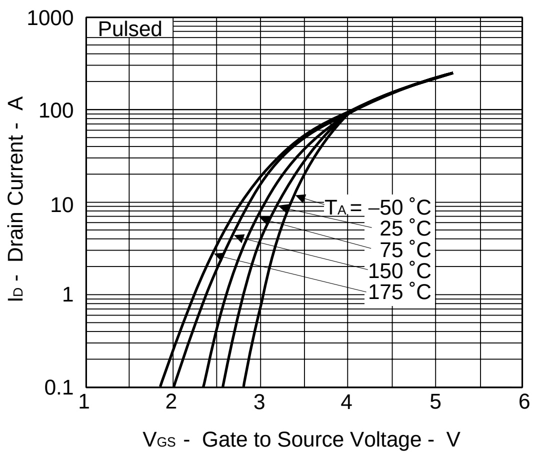


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

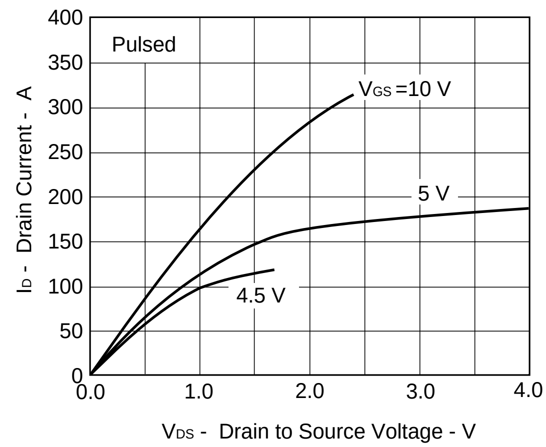


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

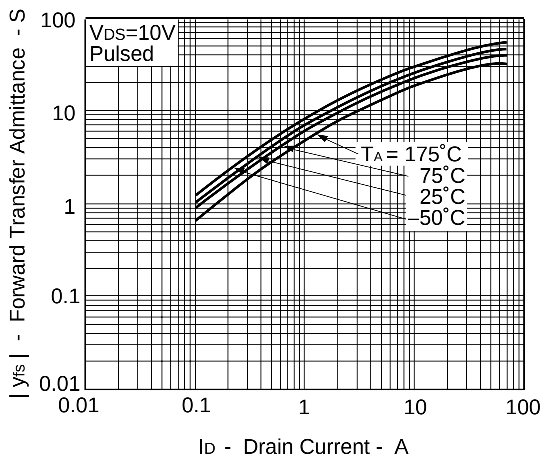


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

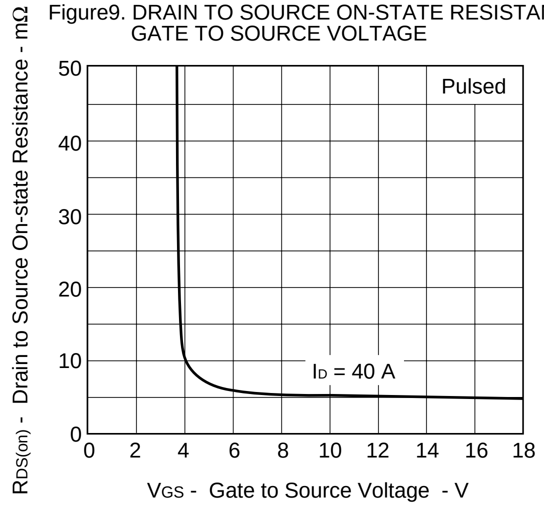


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

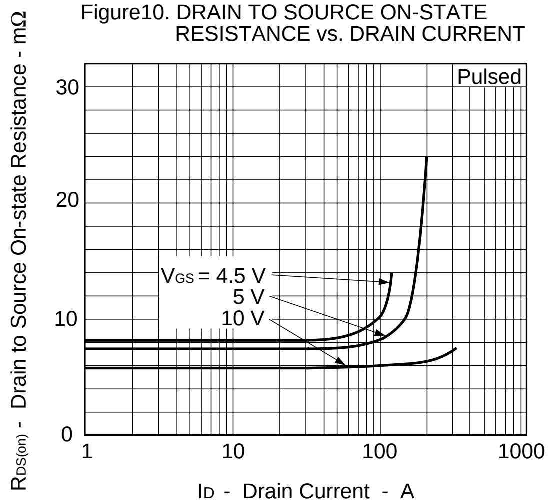


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

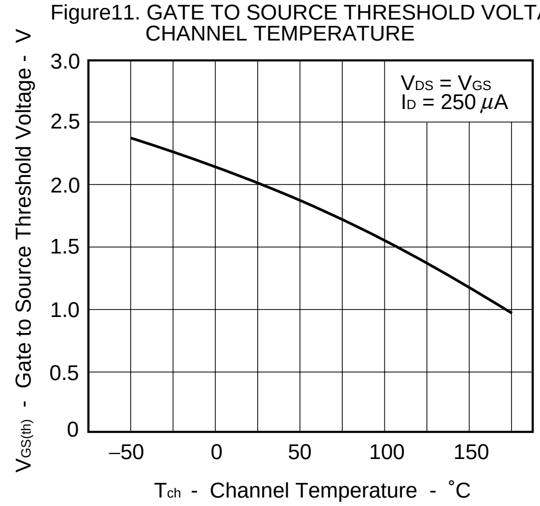


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

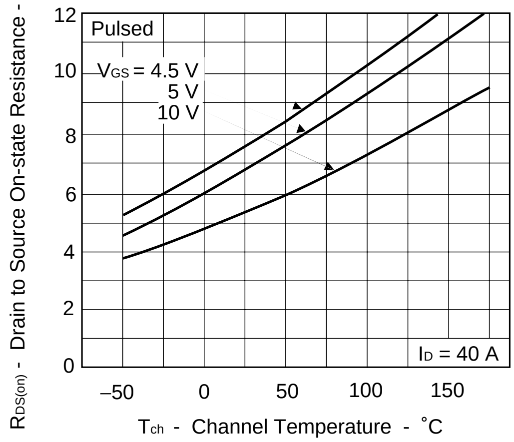


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

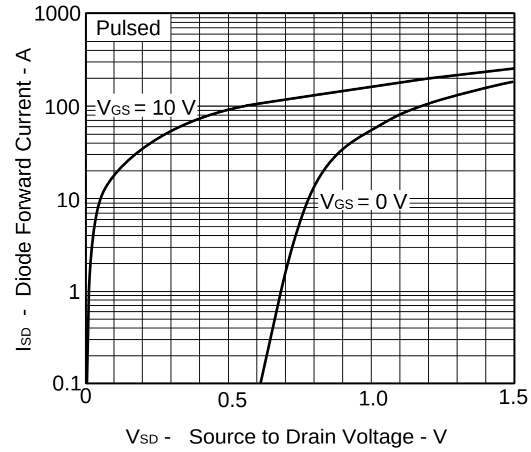


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

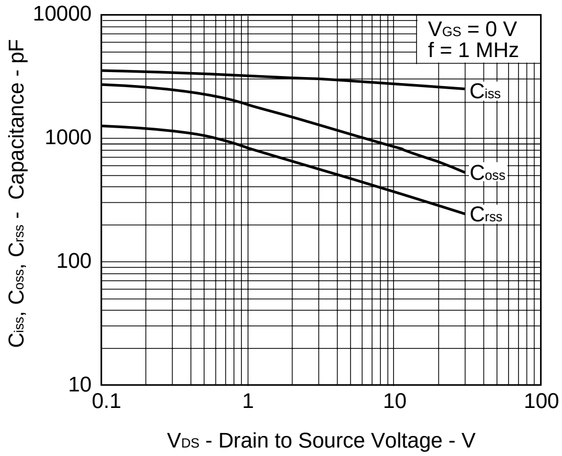


Figure15. SWITCHING CHARACTERISTICS

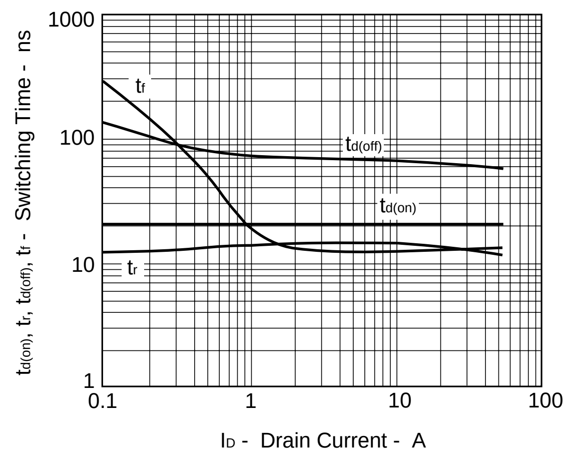


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

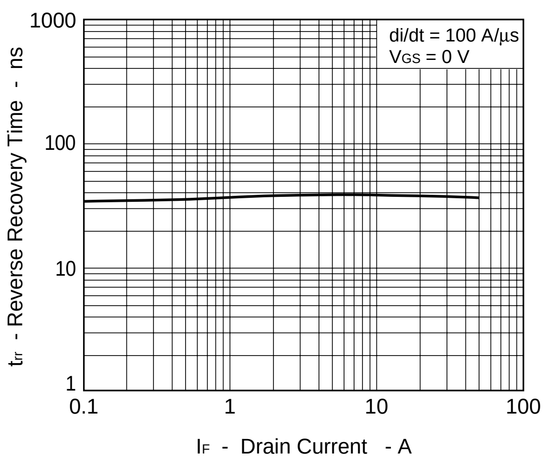
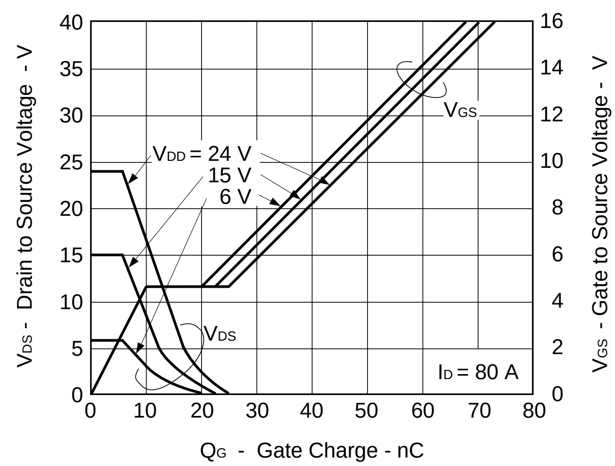
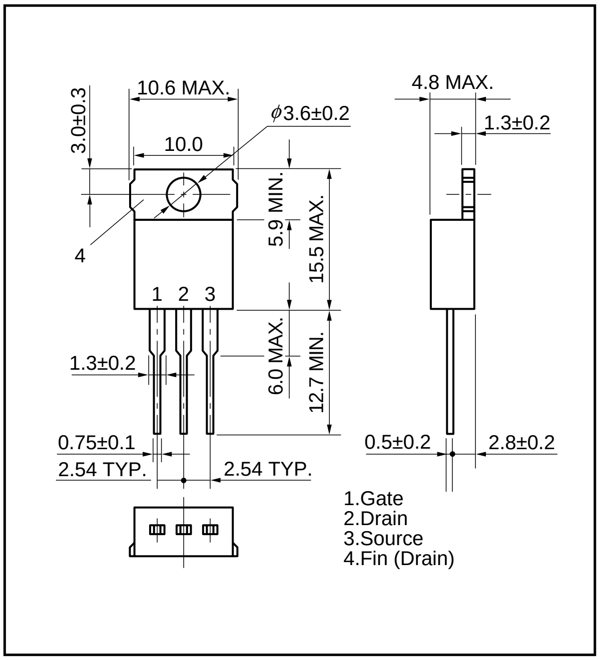


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

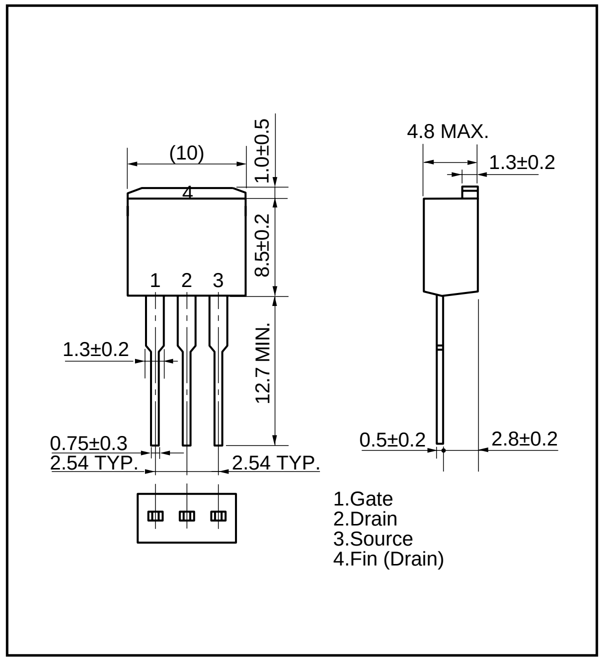


PACKAGE DRAWINGS (Unit: mm)

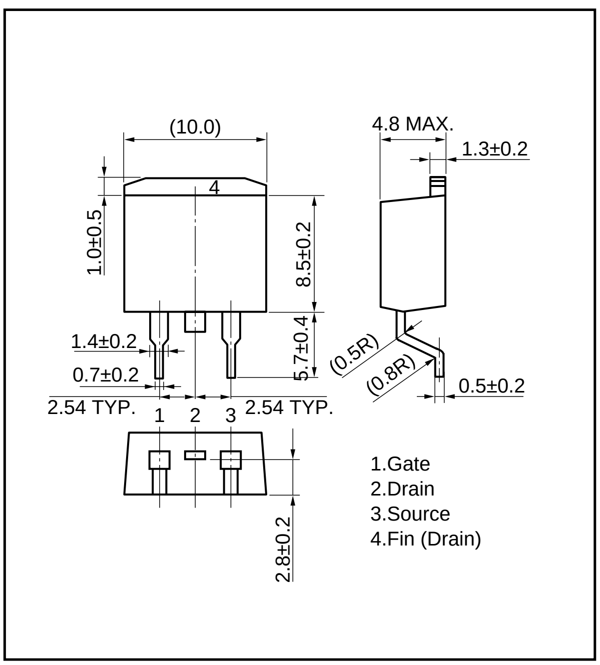
1) TO-220AB (MP-25)



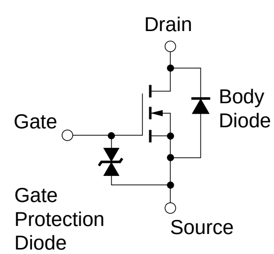
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]