NBSG111

Product Preview

2.5V/3.3V SiGe Differential 1:10 Clock/Data Driver with RSECL* Outputs

*Reduced Swing ECL

The SG111 is a Silicon Germanium 1–to–10 differential clock/data driver. The device is functionally equivalent to the LVEP111 device with much higher bandwidth and lower EMI capabilities.

Inputs incorporate internal 50 Ω termination resistors (input to VT pad) and accept NECL (Negative ECL), PECL (Positive ECL), TTL, CMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

The Q0:9/$\overline{Q0:9}$ outputs have a differential synchronous enable (EN/$\overline{EN}$) pin. The synchronous enable pin is used to avoid a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of selected clock (CLK0/$\overline{CLK0}$ or CLK1/$\overline{CLK1}$), therefore all associated specification limits are referenced to the negative edge of the selected clock input.

The V_{BB} and V_{MM} pins are internally generated voltage supplies available to this device only. The V_{BB} is used for single–ended NECL or PECL inputs and the V_{MM} pin is used for CMOS inputs. For single–ended input operation, the unused differential input is connected to V_{BB} or V_{MM} as a switching reference voltage. V_{BB} or V_{MM} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{MM} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} and V_{MM} outputs should be left open.

- Maximum Input Clock Frequency > 6 GHz Typical
- 260 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.465 V
- RSECL Output Level (400 mV Peak–to–Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP and EP Devices
- V_{BB} and V_{MM} Reference Voltage Output

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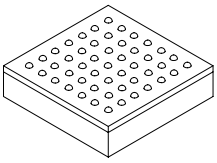
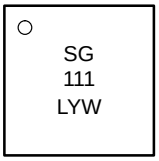
MARKING DIAGRAM*





FCBGA–49
BA SUFFIX
CASE 489A

SG111 = Device Code
L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG111BA	8x8 mm FCBGA–49	100 Units/Tray
NBSG111BAR2	8x8 mm FCBGA–49	500/Tape & Reel

Board	Description
SG111EVB	NBSG111BA Evaluation Board

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

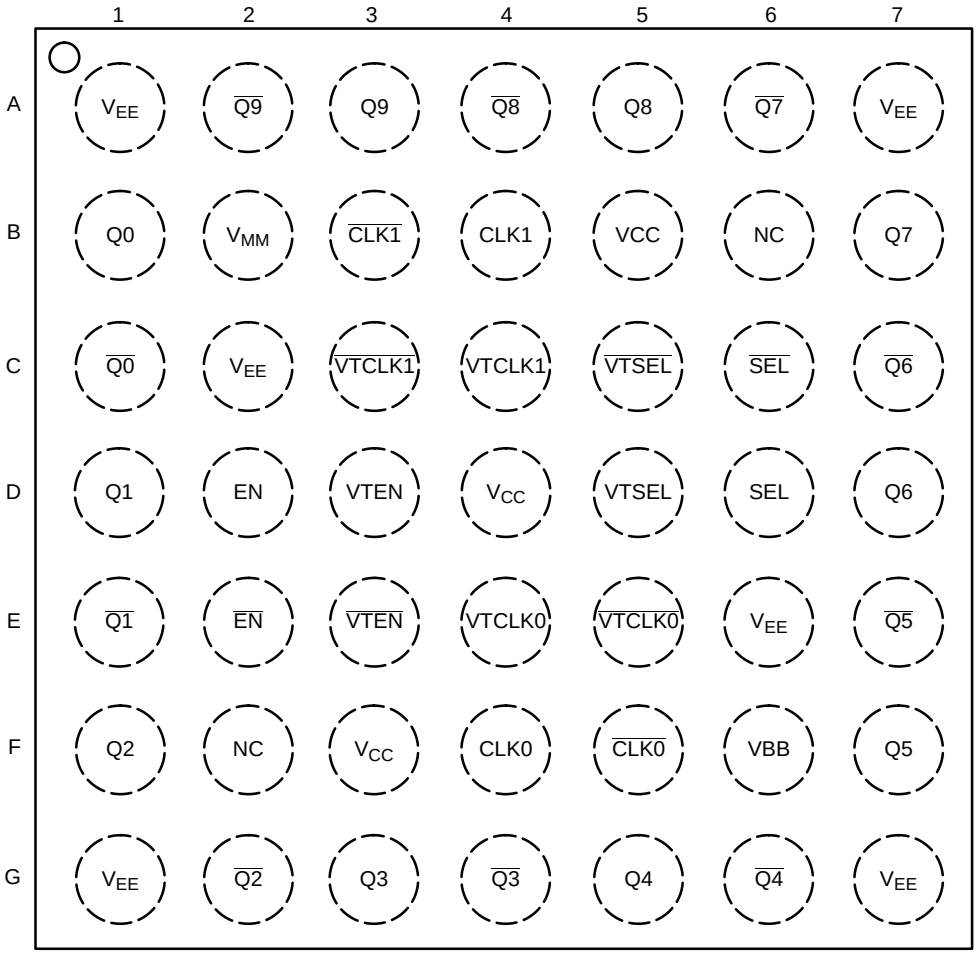


Figure 1. Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
SEL*, $\overline{\text{SEL}}$**	Active Clock Select Input
EN*, $\overline{\text{EN}}$**	Output Enable
VTEN, $\overline{\text{VTEN}}$, VTSEL, $\overline{\text{VTSEL}}$, VTCLK0, $\overline{\text{VTCLK0}}$, VTCLK1, $\overline{\text{VTCLK1}}$	50 Ω Internal Input Termination Resistors
CLK0*, $\overline{\text{CLK0}}$**, CLK1*, $\overline{\text{CLK1}}$**	ECL/TTL/CMOS/CML/LVDS Compatible (CLK) Inputs
Q0:9, $\overline{\text{Q0:9}}$	RSECL Data Outputs
V_{BB}	(ECL) Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply
V_{MM}	(CMOS) Reference Voltage Output, (V_{CC}–V_{EE})/2
NC	No Connect

* Pin will default low when left open.
** Pin will default to V_{CC}/2 when left open.

FUNCTION TABLE

SEL	EN	Active Input
L	L	Disabled Outputs
L	H	CLK0, $\overline{CLK0}$
H	L	Disabled Outputs
H	H	CLK1, $\overline{CLK1}$

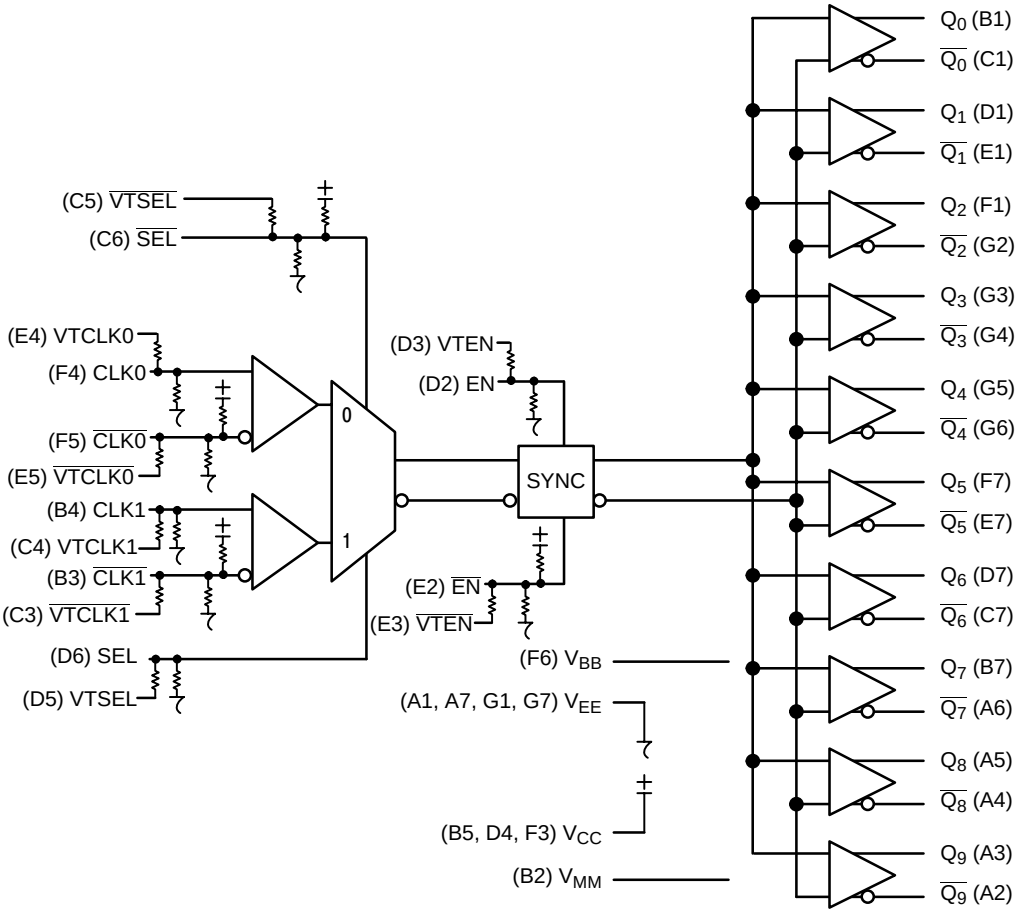


Figure 2. Logic Diagram

INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK0, VTCLK1, VTEN, VTSEL and $\overline{VTCLK0}$, $\overline{VTCLK1}$, $\overline{VTEN}$, $\overline{VTSEL}$ to V_{CC}
LVDS	Connect VTCLK0, VTCLK1, VTEN, VTSEL and $\overline{VTCLK0}$, $\overline{VTCLK1}$, $\overline{VTEN}$, $\overline{VTSEL}$ Together
AC–COUPLED	Bias VTCLK0, VTCLK1, VTEN, VTSEL and $\overline{VTCLK0}$, $\overline{VTCLK1}$, $\overline{VTEN}$, $\overline{VTSEL}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	See Text on Page 1. Unused Differential Input Switching Voltage Reference Range is from V_{EE} + 1125 mV to V_{CC} – 75 mV

ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor (CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$, SEL, $\overline{SEL}$, EN, $\overline{EN}$)	75 kΩ
Internal Input Pullup Resistor ($\overline{CLK0}$, $\overline{CLK1}$, $\overline{SEL}$, $\overline{EN}$)	36.5 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	>2 kV >100 V TBD
Moisture Sensitivity (Note 1)	Level 3
Flammability Rating	UL 94 V–0 @ 0.125 in
Oxygen Index	28 to 34
Transistor Count	457
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		–3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	3.6 –3.6	V V
V_{INPP} (IN–IN)	Differential Input Voltage (|CLK – $\overline{CLK}$|)	$V_{CC} – V_{EE} \geq$ 2.8 V $V_{CC} – V_{EE} <$ 2.8 V		2.8 $\|V_{CC} – V_{EE}\|$	V V
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{BB}	V_{BB} Sink/Source			1	mA
I_{MM}	V_{MM} Sink/Source			1	mA
TA	Operating Temperature Range			–40 to +70	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 3) (Note 3)	0 LFPM 500 LFPM	49 FCBGA 49 FCBGA	67 57	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	2S2P (Note 3)	49 FCBGA	2 to 4	°C/W
T_{sol}	Wave Solder	< 15 sec.		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard 51–6, multilayer board – 2S2P (2 signal, 2 power).

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 4)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current					90					mA
V_{OH}	Output HIGH Voltage (Note 5)					1600					mV
V_{OUTpp}	Output P–P Voltage					400					mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 7 and 8)	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 7 and 9)	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	mV
V_{BB}	PECL Output Voltage Reference	1080	1140	1200	1080	1140	1200	1080	1140	1200	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		2.5	1.2		2.5	1.2		2.5	V
V_{MM}	CMOS Output Voltage Reference (V_{CC} – V_{EE})/2	1100	1250	1400	1100	1250	1400	1100	1250	1400	mV
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 10)

Symbol	Characteristic	–40°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current					90					mA
V_{OH}	Output HIGH Voltage (Note 5)					2400					mV
V_{OUTpp}	Output P–P Voltage					400					mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 7 and 8)	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 7 and 9)	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	mV
V_{BB}	PECL Output Voltage Reference	1880	1940	2000	1880	1940	2000	1880	1940	2000	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 6)	1.2		3.3	1.2		3.3	1.2		3.3	V
V_{MM}	CMOS Output Voltage Reference (V_{CC} – V_{EE})/2	1500	1650	1800	1500	1650	1800	1500	1650	1800	mV
R_T	Internal Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above tables after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

4. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to –0.965 V.
5. All outputs loaded with 50 Ω to V_{CC} – 1.5 volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).
6. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
7. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}. $V_{THR(MIN)} = V_{IHCMR} + 75$ mV. $V_{THR(MAX)} = V_{IHCMR} – 75$ mV.
8. V_{IH} cannot exceed V_{CC}.
9. V_{IL} always $\geq V_{EE}$.
10. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925 V to –0.165 V.

*Typicals used for testing purposes.

DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V (Note 11)

		–40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current					90					mA
V_{OH}	Output HIGH Voltage (Note 12)					–900					mV
V_{OUTpp}	Output P–P Voltage					400					mV
V_{IH}	Input HIGH Voltage (Single–Ended) (Notes 14 and 15)	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	V_{THR} + 75	V_{CC} – 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single–Ended) (Notes 14 and 16)	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	V_{IH} – 2500	V_{CC} – 1400*	V_{THR} – 75	mV
V_{BB}	NECL Output Voltage Reference	–1420	–1360	–1300	–1420	–1360	–1300	–1420	–1360	–1300	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V_{EE}+1.2		0.0	V
V_{MM}	CMOS Output Voltage Reference (Note 17)	V_{MMT} – 150	V_{MMT}	V_{MMT} + 150	V_{MMT} – 150	V_{MMT}	V_{MMT} + 150	V_{MMT} – 150	V_{MMT}	V_{MMT} + 150	mV
I_{IH}	Input HIGH Current (@ V_{IH})		30	100		30	100		30	100	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}.
12. All outputs loaded with 50 Ω to V_{CC} – 1.5 volts. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
14. V_{THR} is the voltage applied to the complementary input, typically V_{BB} or V_{MM}. $V_{THR(MIN)} = V_{IHCMR} + 75$ mV. $V_{THR(MAX)} = V_{IHCMR} – 75$ mV.
15. V_{IH} cannot exceed V_{CC}.
16. V_{IL} always $\geq V_{EE}$.
17. V_{MM} Typical = $|V_{CC} – V_{EE}| / 2 + V_{EE} = V_{MMT}$.

*Typicals used for testing purposes.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		–40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 3) (Note 18)					> 6					GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential					260					ps
t_{SKEW}	Duty Cycle Skew (Note 19) Within–Device Skew (Note 20) Device–to–Device Skew (Note 21)					< 10 < 15 < 85					ps
t_S	Setup Time to CLK (EN to Selected CLK0:1)					TBD					ps
t_H	Hold Time (EN to Selected CLK0:1)					TBD					ps
t_{JITTER}	Cycle–to–Cycle Jitter (RMS) (See Figure 3) (Note 18)					< 2					ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential) (Note 22)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, $\overline{Q}$					40					ps

18. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to V_{CC} – 1.5 V.
19. $t_{SKEW} = |t_{PLH} – t_{PHL}|$ for a nominal 50% differential clock input waveform (Figure 4).
20. Within–Device skew is measured between outputs under identical transitions and conditions on any one device.
21. Device–to–Device skew for identical transitions at identical V_{CC} levels.
22. V_{INPP} (MAX) cannot exceed $V_{CC} – V_{EE}$ (applicable only when $V_{CC} – V_{EE} < 2600$ mV).

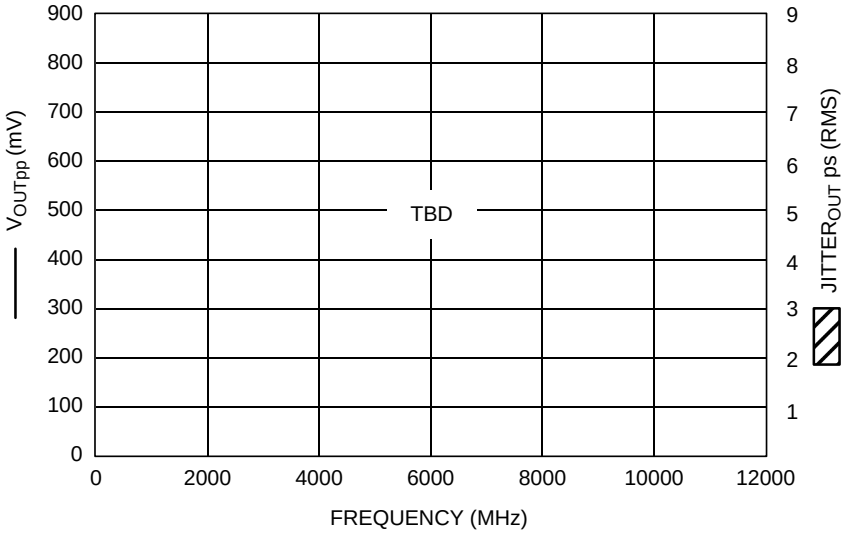


Figure 3. V_{OUT}/Jitter vs. Frequency

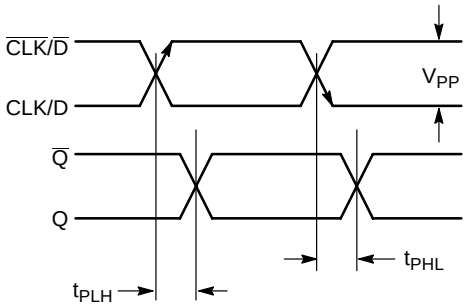


Figure 4. AC Reference Measurement

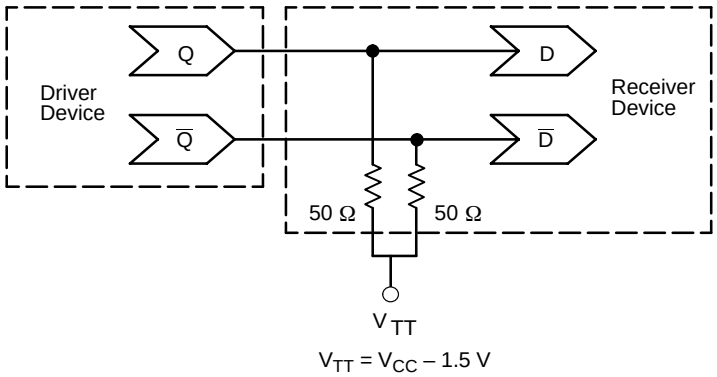
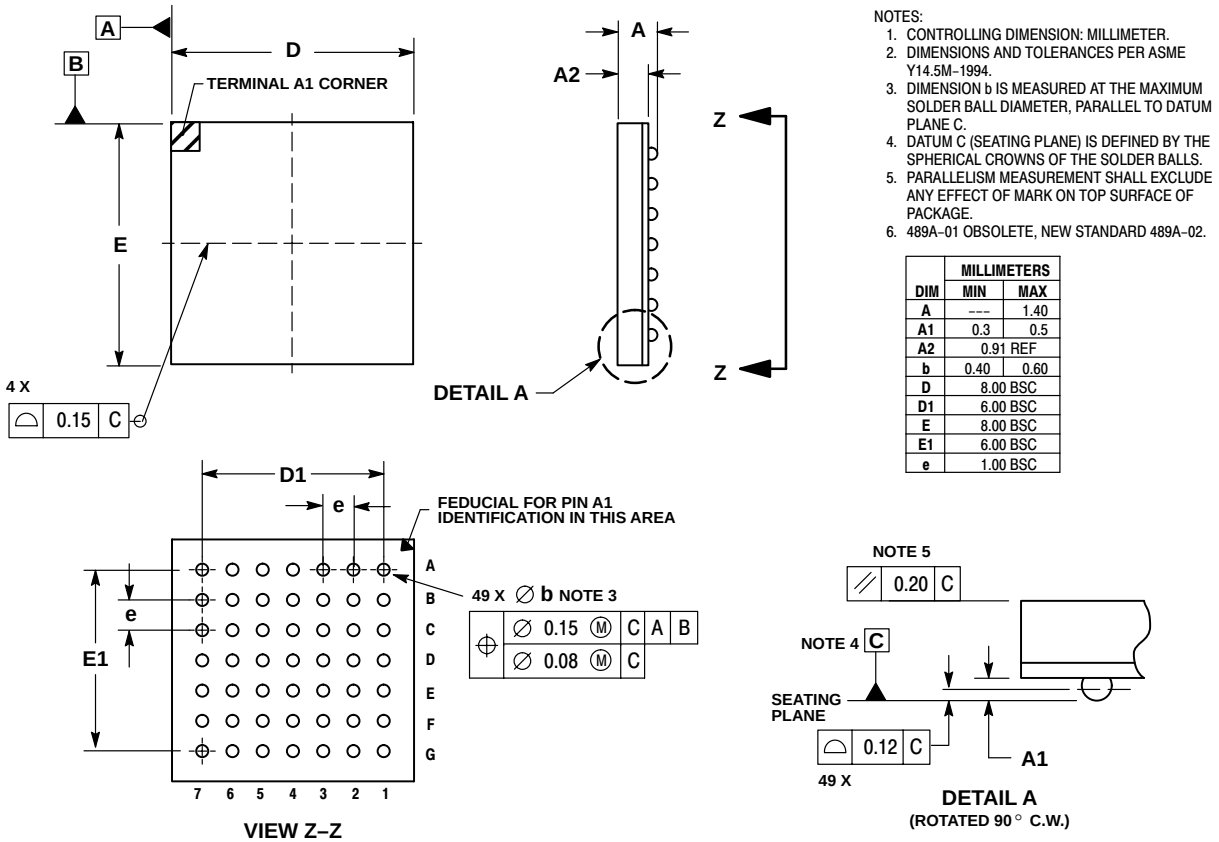


Figure 5. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 – Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA–49
BA SUFFIX
PLASTIC 8x8 mm (1.0 mm pitch) BGA FLIP CHIP PACKAGE
CASE 489A
ISSUE A



NOTES:
1. CONTROLLING DIMENSION: MILLIMETER.
2. DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
4. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. 489A–01 OBSOLETE, NEW STANDARD 489A–02.

	MILLIMETERS	
DIM	MIN	MAX
A	---	1.40
A1	0.3	0.5
A2	0.91 REF	
b	0.40	0.60
D	8.00 BSC	
D1	6.00 BSC	
E	8.00 BSC	
E1	6.00 BSC	
e	1.00 BSC	

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