

# NTHD5905T1

## Power MOSFET Dual P-Channel ChipFET™

3.0 Amps, 8 Volts

### Features

- Low  $R_{DS(on)}$  for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package

### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 secs	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	-8.0		V
Gate-Source Voltage	$V_{GS}$	$\pm 8.0$		V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	$\pm 4.1$ $\pm 2.9$	$\pm 3.0$ $\pm 2.2$	A
Pulsed Drain Current	$I_{DM}$	$\pm 10$		A
Continuous Source Current (Diode Conduction) (Note 1)	$I_S$	-1.8	-0.9	A
Maximum Power Dissipation (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.1 1.1	1.1 0.6	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		$^\circ\text{C}$

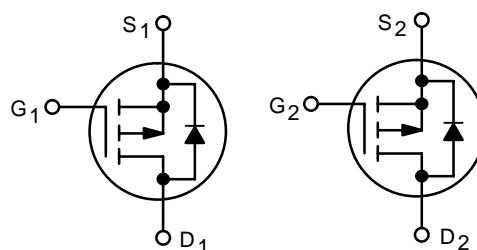
1. Surface Mounted on 1" x 1" FR4 Board.



ON Semiconductor®

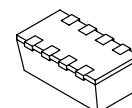
<http://onsemi.com>

**DUAL P-CHANNEL**  
**3.0 AMPS, 8 VOLTS**  
 **$R_{DS(on)} = 90 \text{ m}\Omega$**



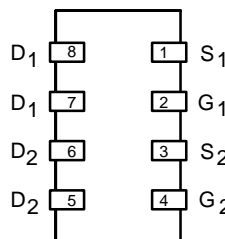
P-Channel MOSFET

P-Channel MOSFET

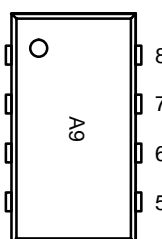


ChipFET  
CASE 1206A  
STYLE 2

### PIN CONNECTIONS



### MARKING DIAGRAM



A9 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
NTHD5905T1	ChipFET	3000/Tape & Reel

# NTHD5905T1

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2) $t \leq 5$ sec Steady State	$R_{thJA}$	50 90	60 110	$^{\circ}\text{C/W}$
Maximum Junction-to-Foot (Drain) Steady State	$R_{thJF}$	30	40	$^{\circ}\text{C/W}$

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### Static

Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.45	–	–	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8.0 \text{ V}$	–	–	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -6.4 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	-1.0	$\mu\text{A}$
		$V_{DS} = -6.4 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^{\circ}\text{C}$	–	–	-5.0	
On-State Drain Current (Note 3)	$I_{D(on)}$	$V_{DS} \leq -5.0 \text{ V}, V_{GS} = -4.5 \text{ V}$	-10	–	–	A
Drain-Source On-State Resistance (Note 3)	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -3.0 \text{ A}$	–	0.075	0.090	$\Omega$
		$V_{GS} = -2.5 \text{ V}, I_D = -2.5 \text{ A}$	–	0.110	0.130	
		$V_{GS} = -1.8 \text{ V}, I_D = -1.0 \text{ A}$	–	0.150	0.180	
Forward Transconductance (Note 3)	$g_{fs}$	$V_{DS} = -5.0 \text{ V}, I_D = -3.0 \text{ A}$	–	7.0	–	S
Diode Forward Voltage (Note 3)	$V_{SD}$	$I_S = -0.9 \text{ A}, V_{GS} = 0 \text{ V}$	–	-0.8	-1.2	V

### Dynamic (Note 4)

Total Gate Charge	$Q_g$	$V_{DS} = -4.0 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.0 \text{ A}$	–	5.5	9.0	nC
Gate-Source Charge	$Q_{gs}$		–	0.5	–	
Gate-Drain Charge	$Q_{gd}$		–	1.5	–	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -4.0 \text{ V}, R_L = 4 \Omega$ $I_D \cong -1.0 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$	–	10	15	ns
Rise Time	$t_r$		–	45	70	
Turn-Off Delay Time	$t_{d(off)}$		–	30	45	
Fall Time	$t_f$		–	10	15	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = -0.9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	–	30	60	

2. Surface Mounted on 1" x 1" FR4 Board.

3. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL CHARACTERISTICS

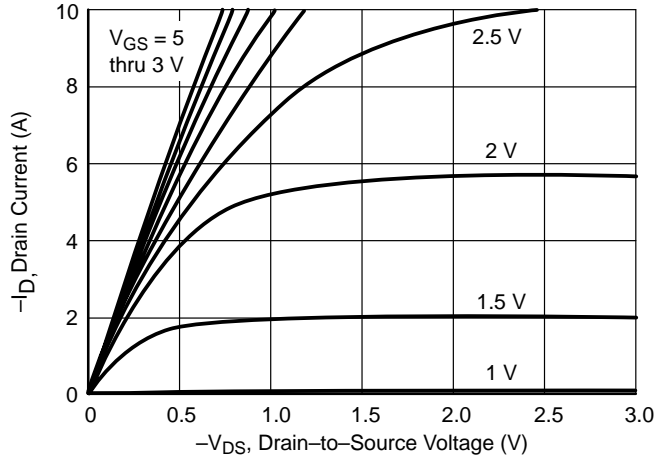


Figure 1. Output Characteristics

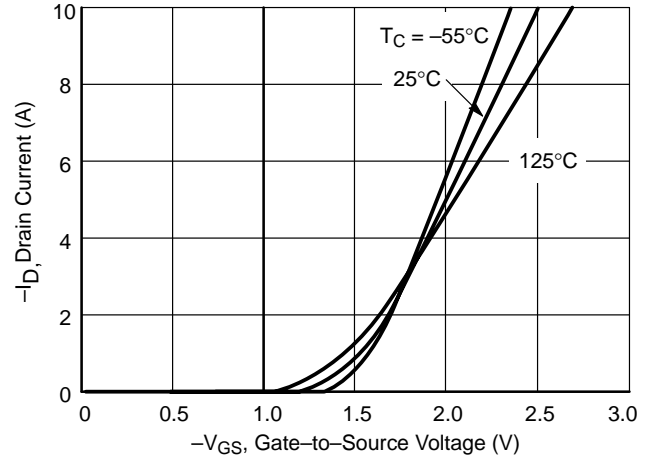


Figure 2. Transfer Characteristics

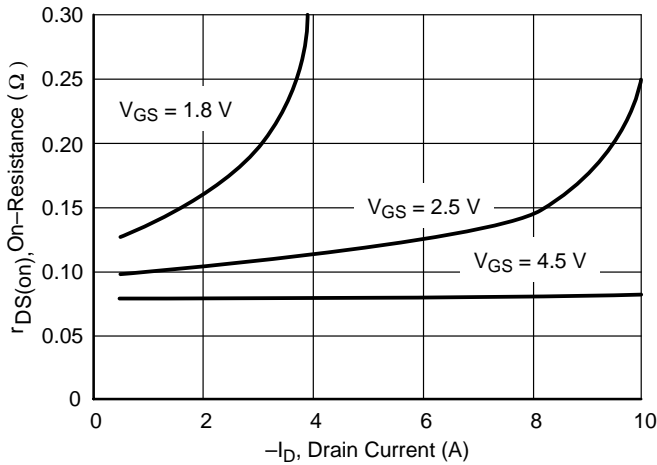


Figure 3. On-Resistance vs. Drain Current

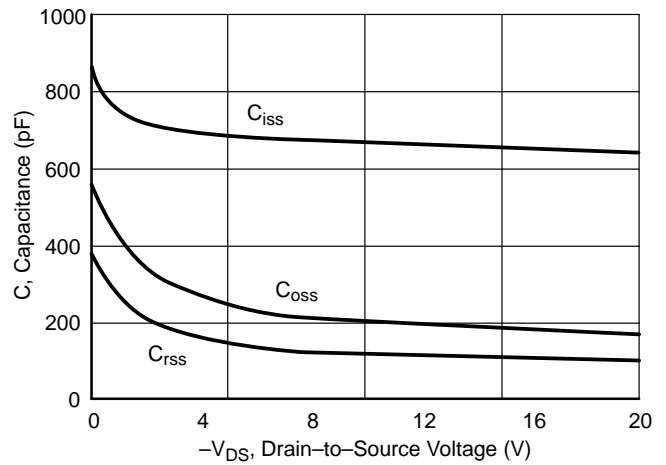


Figure 4. Capacitance

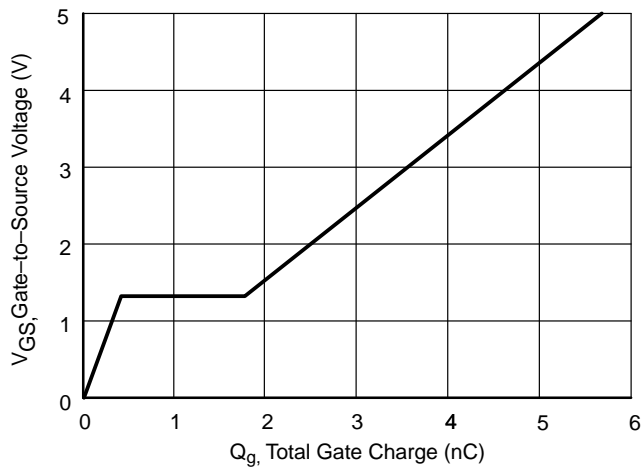


Figure 5. Gate Charge

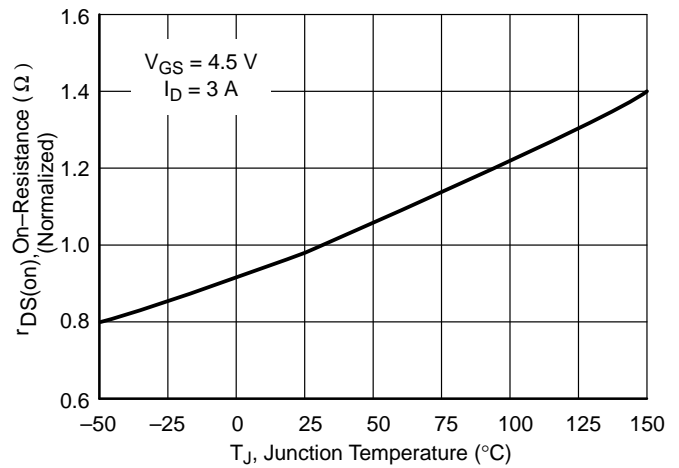


Figure 6. On-Resistance vs. Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

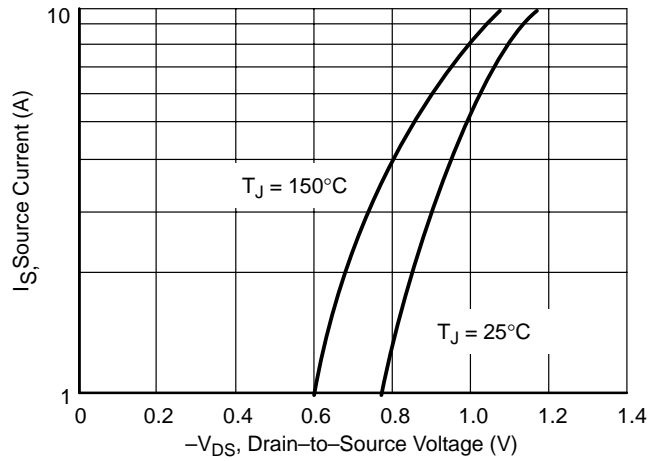


Figure 7. Source Diode Forward Voltage

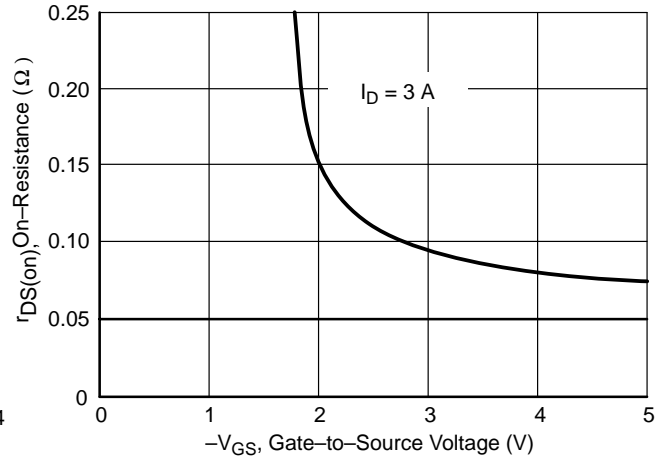


Figure 8. On-Resistance vs. Gate-to-Source Voltage

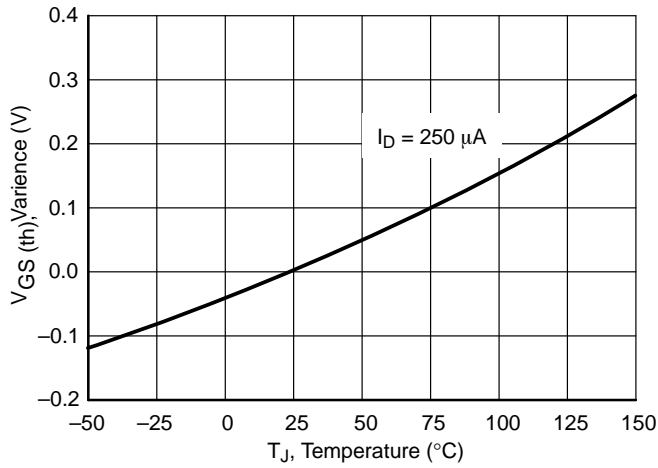


Figure 9. Threshold Voltage

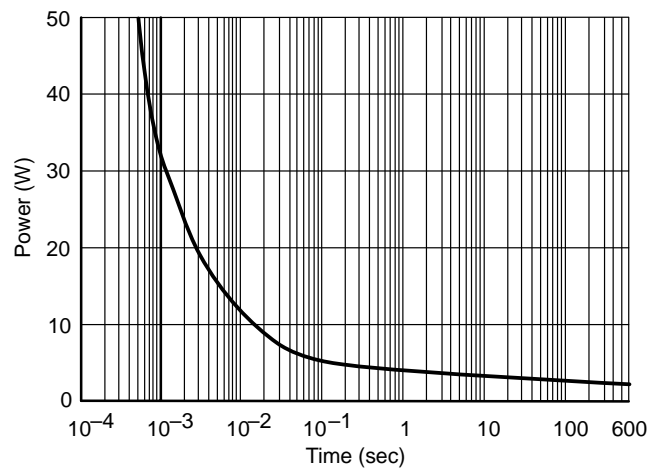


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

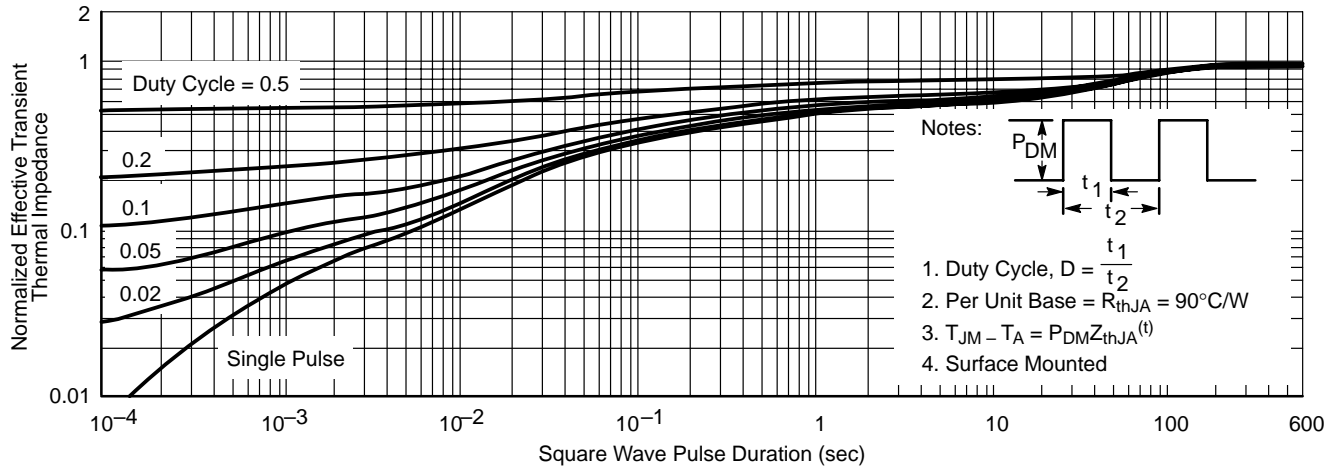


Figure 11. Normalized Thermal Transient Impedance, Junction-to-Ambient

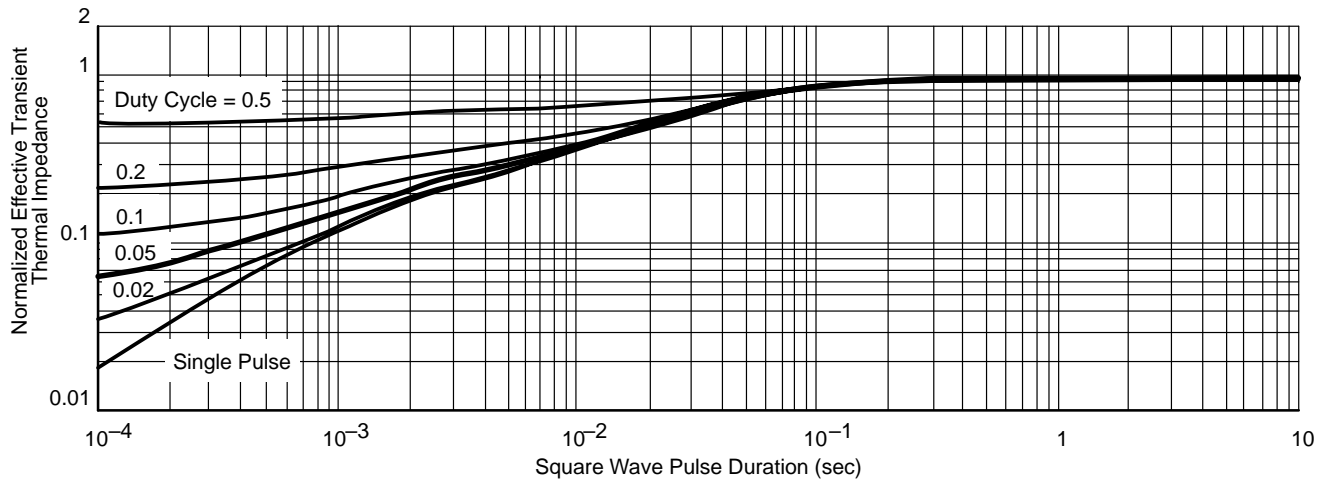


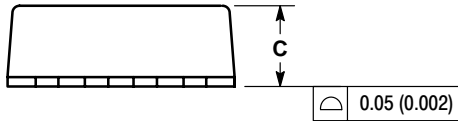
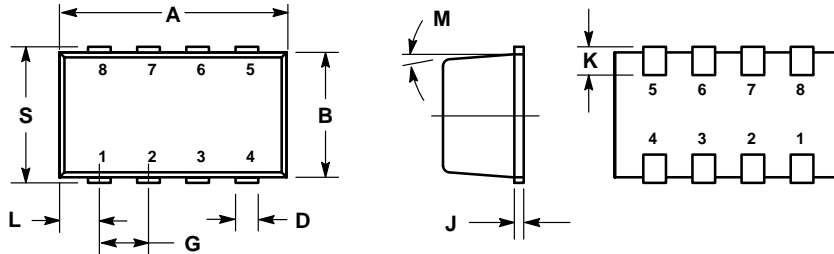
Figure 12. Normalized Thermal Transient Impedance, Junction-to-Foot

## **Notes**

# NTHD5905T1

## PACKAGE DIMENSIONS

**ChipFET**  
CASE 1206A-03  
ISSUE D




STYLE 2:  
PIN 1. SOURCE 1  
2. GATE 1  
3. SOURCE 2  
4. GATE 2  
5. DRAIN 2  
6. DRAIN 2  
7. DRAIN 1  
8. DRAIN 1

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.
7. 1206A-01 AND 1206A-02 OBSOLETE. NEW STANDARD IS 1206A-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.95	3.10	0.116	0.122
B	1.55	1.70	0.061	0.067
C	1.00	1.10	0.039	0.043
D	0.25	0.35	0.010	0.014
G	0.65 BSC		0.025 BSC	
J	0.10	0.20	0.004	0.008
K	0.28	0.42	0.011	0.017
L	0.55 BSC		0.022 BSC	
M	5 ° NOM		5 ° NOM	
S	1.80	2.00	0.072	0.080

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