

# NTMC1300R2

## Power MOSFET 3 Amps, 30 Volts

### Complementary SO-8 Dual

#### Features

- Ultra Low  $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature SO-8 Surface Mount Package

#### Applications

- DC-DC Converters
- Power Management in Portable and Battery Powered Products, i.e.: Computers, Printers, Cellular and Cordless Phones
- Low Voltage Motor Controls in Mass Storage Products, i.e.: Disk Drives, Tape Drives

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage - Continuous	$V_{GS}$	$\pm 20$	V
Drain Current - Continuous (Note 1) N-Channel P-Channel	$I_D$	2.2 1.8	Adc
Drain Current - Continuous (Note 2) N-Channel P-Channel	$I_D$	2.8 2.3	Adc
Drain Current - Continuous (Note 3) N-Channel P-Channel	$I_D$	3.6 3.0	Adc
Drain Current - Pulsed N-Channel P-Channel	$I_{DM}$	8.5 7.0	Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 3)	$P_D$	2.0	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 20\text{ Vdc}$ , $V_{GS} = 10\text{ Vdc}$ , $I_L = 2.45\text{ Apk}$ , $L = 25\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	75	mJ
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2) Junction-to-Ambient (Note 3)	$R_{\theta JA}$	178.5 106 62.5	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes for 10 Seconds	$T_L$	260	$^\circ\text{C}$

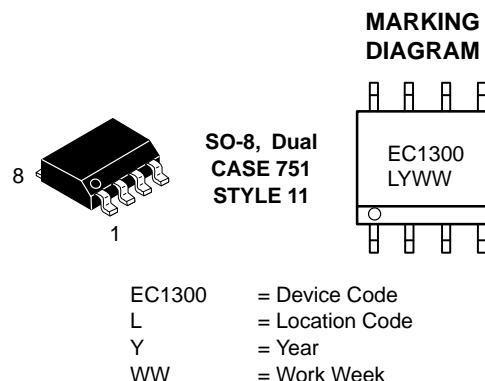
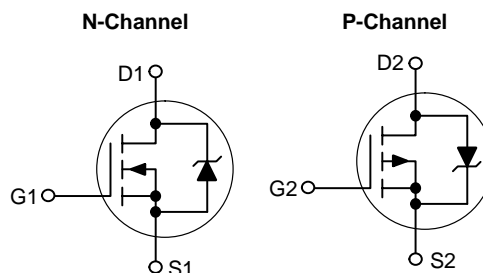
1. When surface mounted to an FR-4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>), Steady State.
2. When surface mounted to an FR-4 board using 1" pad size, (Cu Area 0.412 in<sup>2</sup>), Steady State.
3. When surface mounted to an FR-4 board using 1" pad size, (Cu Area 0.412 in<sup>2</sup>),  $T \leq 10$  Seconds.



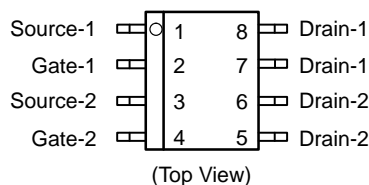
ON Semiconductor®

<http://onsemi.com>

**3 AMPERES, 30 VOLTS**  
**73 m $\Omega$  @  $V_{GS} = 10\text{ V}$  (Typ)**  
**(N-Channel)**  
**100 m $\Omega$  @  $V_{GS} = 10\text{ V}$  (Typ)**  
**(P-Channel)**



#### PIN ASSIGNMENT



#### ORDERING INFORMATION

Device	Package	Shipping
NTMC1300R2	SO-8	2500/Tape & Reel

# NTMC1300R2

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Polarity	Min	Typ	Max	Unit
----------------	--------	----------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μA)	V <sub>(BR)DSS</sub>	-	30	-	-	Vdc
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = 30 Vdc, T <sub>J</sub> = 25°C)	I <sub>DSS</sub>	(N) (P)	- -	- -	1.0 1.0	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-	100	nAdc

### ON CHARACTERISTICS (Notes 4 & 6)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc)	V <sub>GS(th)</sub>	(N) (P)	1.0 1.0	1.8 1.6	2.2 2.2	Vdc
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = 10 Vdc, I <sub>D</sub> = 3.0 Adc)	R <sub>DS(on)</sub>	(N) (P)	- -	0.073 0.100	0.090 0.140	Ω
Static Drain-to-Source On-State Resistance (V <sub>GS</sub> = 4.5 Vdc, I <sub>D</sub> = 1.5 Adc)	R <sub>DS(on)</sub>	(N) (P)	- -	0.093 0.150	0.130 0.200	Ω
Forward Transconductance (V <sub>DS</sub> = 3.0 Vdc, I <sub>D</sub> = 1.5 Adc)	g <sub>FS</sub>	(N) (P)	- -	4.0 4.0	- -	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	(N) (P)	- -	190 325	300 550	pF
Output Capacitance		C <sub>oss</sub>	(N) (P)	- -	75 110	150 175	
Reverse Transfer Capacitance		C <sub>rss</sub>	(N) (P)	- -	30 40	60 75	

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V <sub>DD</sub> = 24 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 10 Vdc, R <sub>G</sub> = 6.0 Ω)	t <sub>d(on)</sub>	(N) (P)	- -	10 9.0	20 20	ns
Rise Time		t <sub>r</sub>	(N) (P)	- -	7.0 11	15 20	
Turn-Off Delay Time		t <sub>d(off)</sub>	(N) (P)	- -	20 25	35 40	
Fall Time		t <sub>f</sub>	(N) (P)	- -	5.0 13	15 25	
Gate Charge	(V <sub>DS</sub> = 16 Vdc, I <sub>D</sub> = 2.0 Adc, V <sub>GS</sub> = 4.5 Vdc)	Q <sub>T</sub>	(N) (P)	- -	3.0 10	5.0 15	nC
		Q <sub>gs</sub>	(N) (P)	- -	1.0 1.5	- -	
		Q <sub>gd</sub>	(N) (P)	- -	1.5 4.0	- -	

### BODY-DRAIN DIODE RATINGS (Note 6)

Diode Forward On-Voltage	(I <sub>S</sub> = 1.7 Adc, V <sub>GS</sub> = 0 Vdc)	V <sub>SD</sub>	(N) (P)	- -	0.85 0.81	1.1 1.1	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 2.0 Adc, V <sub>GS</sub> = 0 Vdc, dI <sub>S</sub> /dt = 100 A/μs)	t <sub>rr</sub>	(N) (P)	- -	11 20	- -	ns
		t <sub>a</sub>	(N) (P)	- -	8.0 16	- -	
		t <sub>b</sub>	(N) (P)	- -	3.0 4.0	- -	
Reverse Recovery Stored Charge		Q <sub>rr</sub>	(N) (P)	- -	0.005 0.020	- -	μC

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.
6. Negative signs for P-Channel device omitted for clarity.

TYPICAL ELECTRICAL CHARACTERISTICS

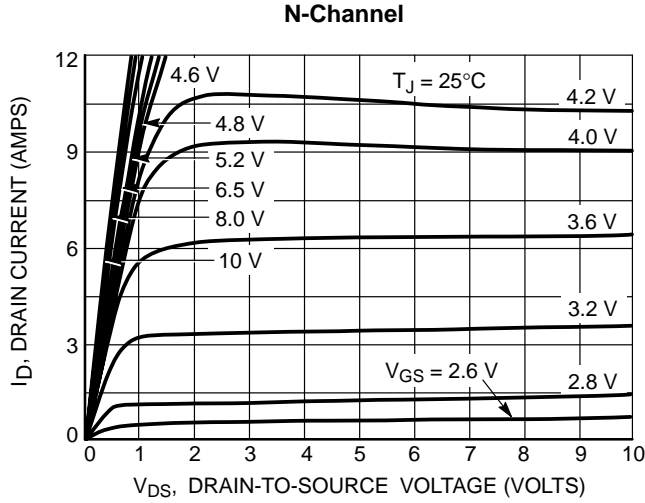


Figure 1. On-Region Characteristics

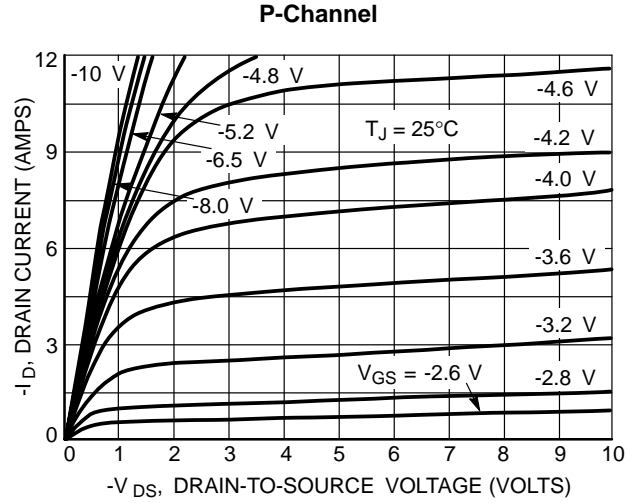


Figure 2. On-Region Characteristics

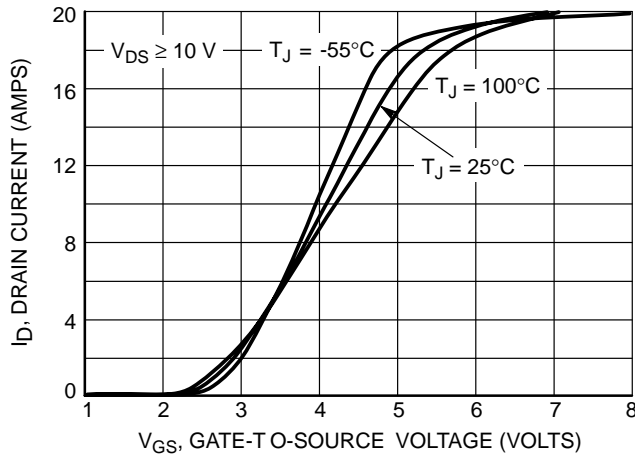


Figure 3. Transfer Characteristics

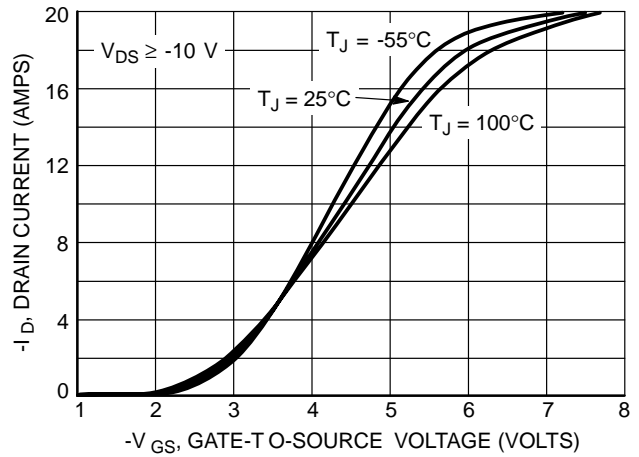


Figure 4. Transfer Characteristics

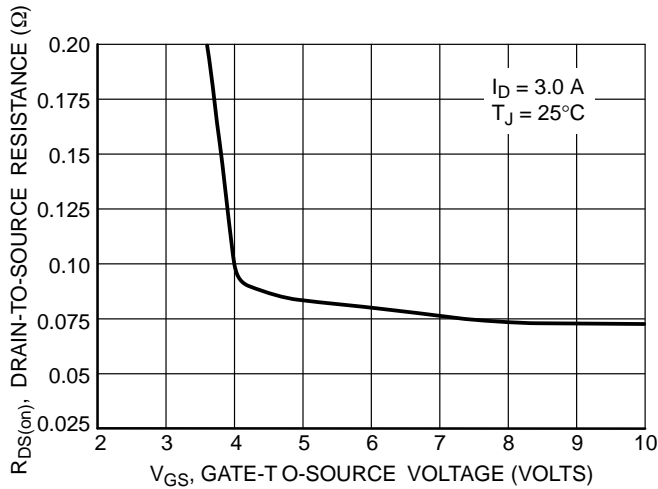


Figure 5. On-Resistance versus Gate-To-Source Voltage

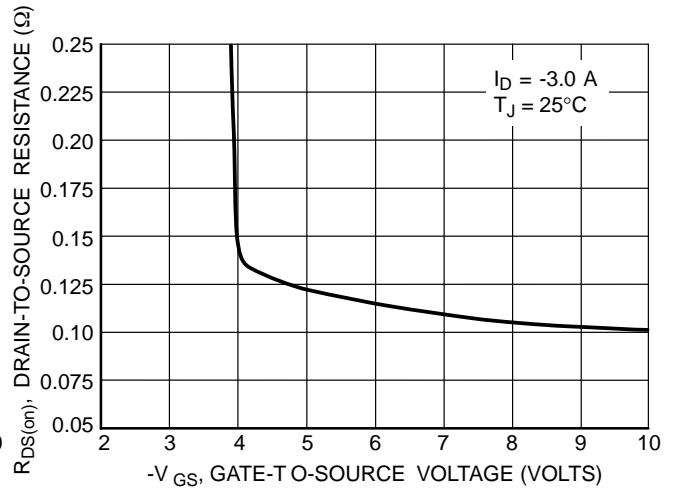


Figure 6. On-Resistance versus Gate-To-Source Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

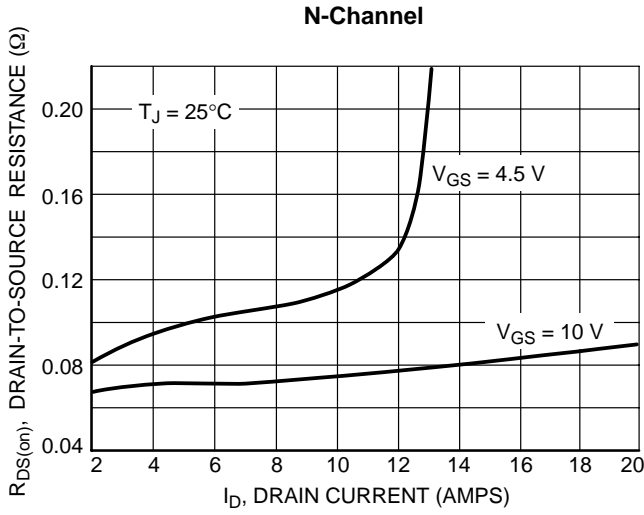


Figure 7. On-Resistance versus Drain Current and Gate Voltage

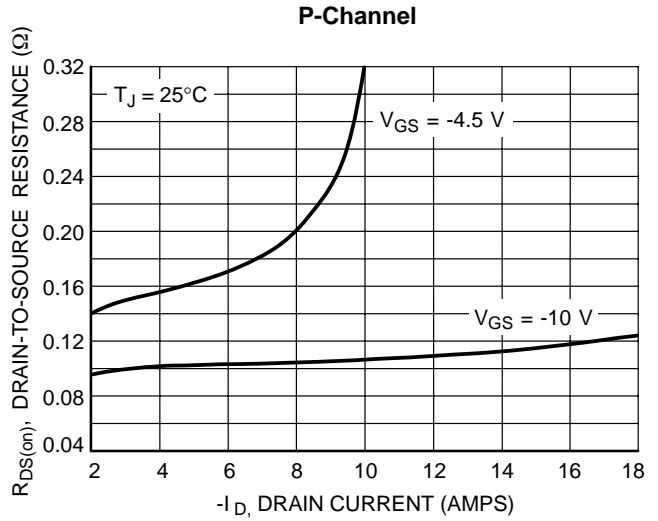


Figure 8. On-Resistance versus Drain Current and Gate Voltage

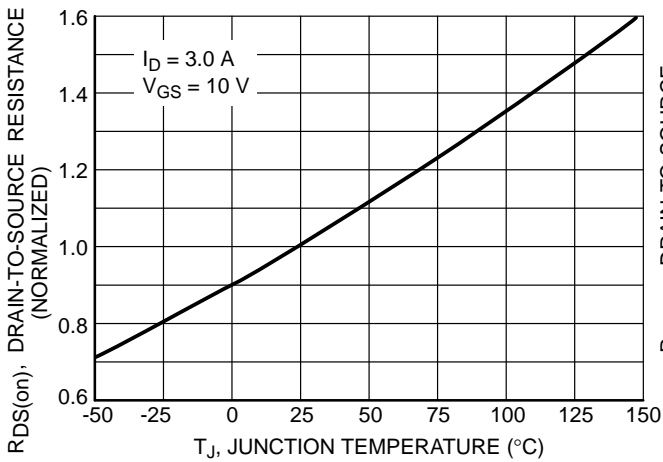


Figure 9. On-Resistance Variation with Temperature

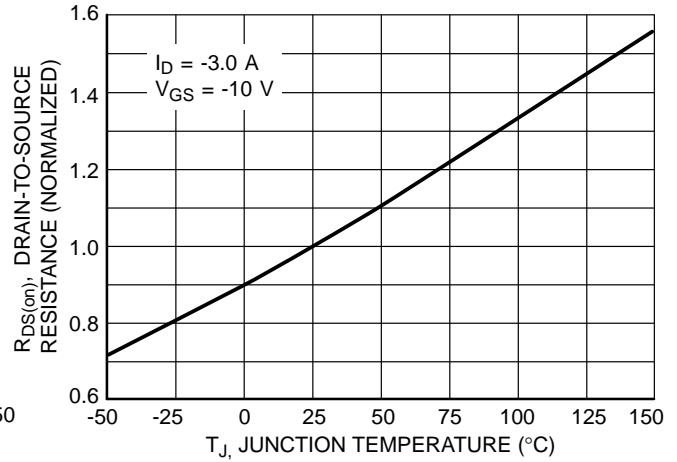


Figure 10. On-Resistance Variation with Temperature

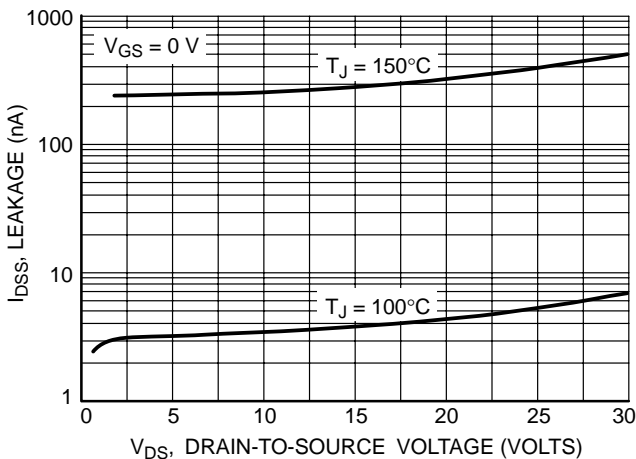


Figure 11. Drain-To-Source Leakage Current versus Voltage

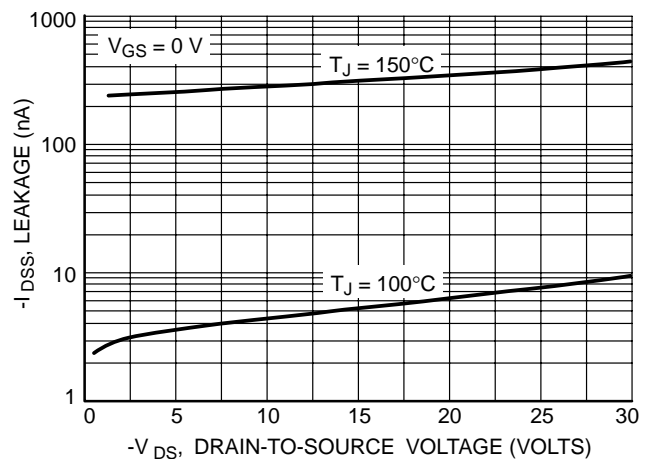
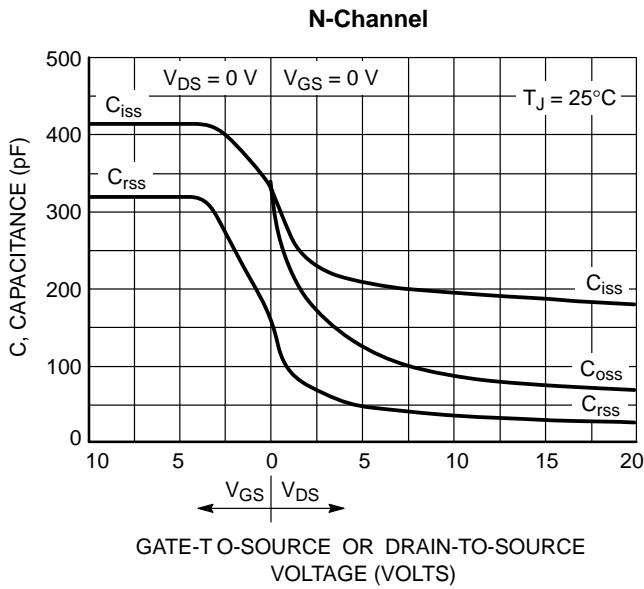
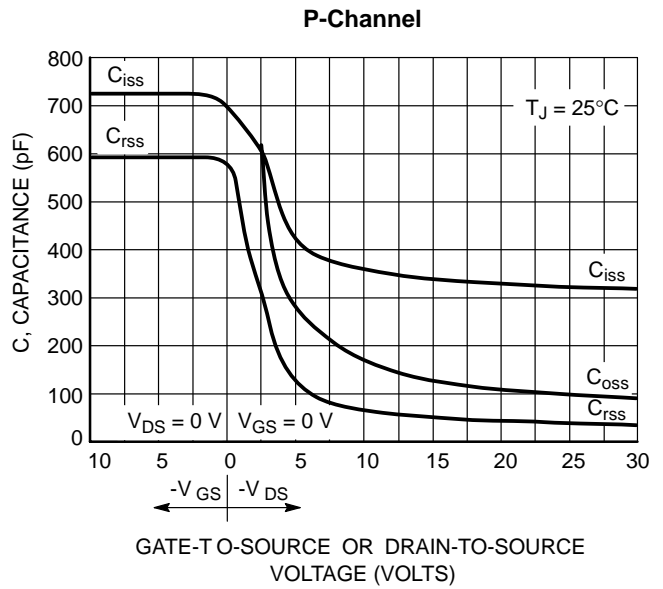


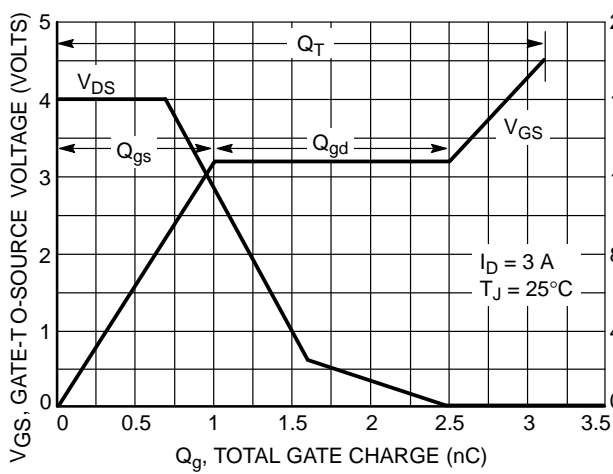
Figure 12. Drain-To-Source Leakage Current versus Voltage



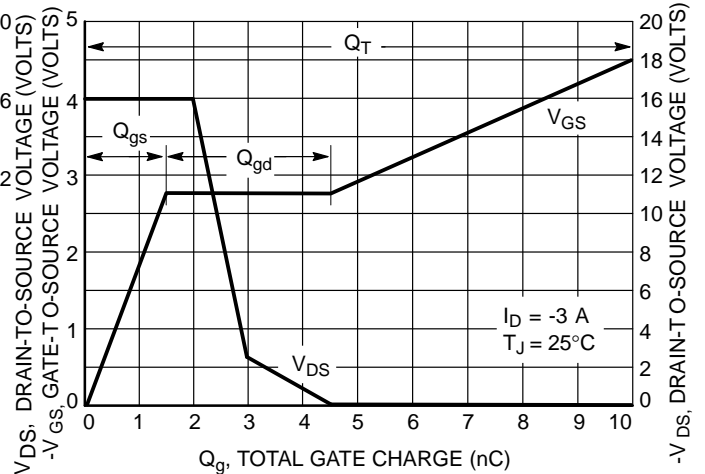
**Figure 13. Capacitance Variation**



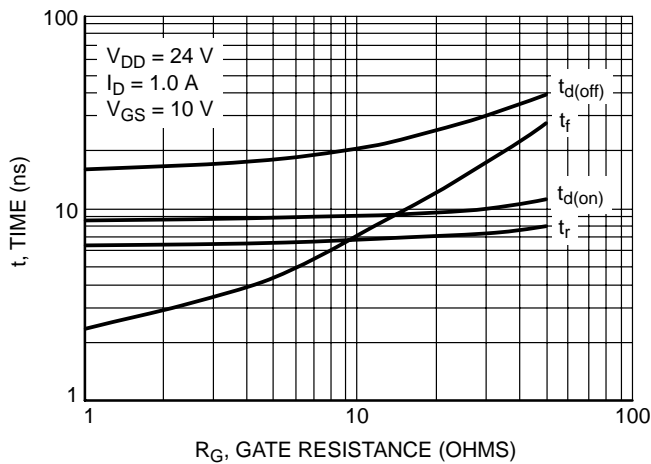
**Figure 14. Capacitance Variation**



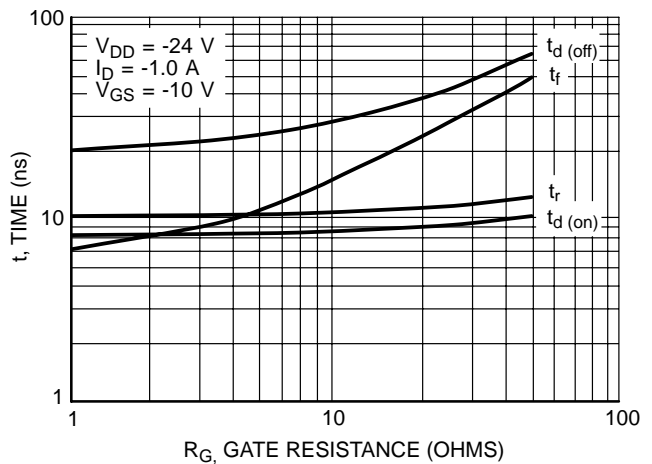
**Figure 15. Gate-To-Source and  
Drain-To-Source Voltage versus Total Charge**



**Figure 16. Gate-To-Source and  
Drain-To-Source Voltage versus Total Charge**



**Figure 17. Resistive Switching Time  
Variation versus Gate Resistance**



**Figure 18. Resistive Switching Time  
Variation versus Gate Resistance**

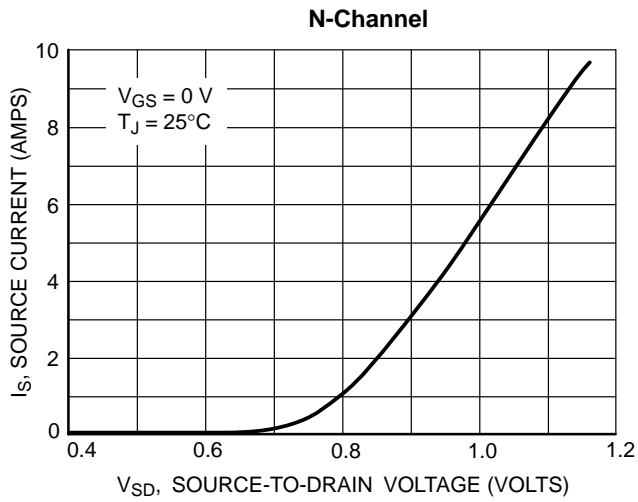


Figure 19. Diode Forward Voltage versus Current

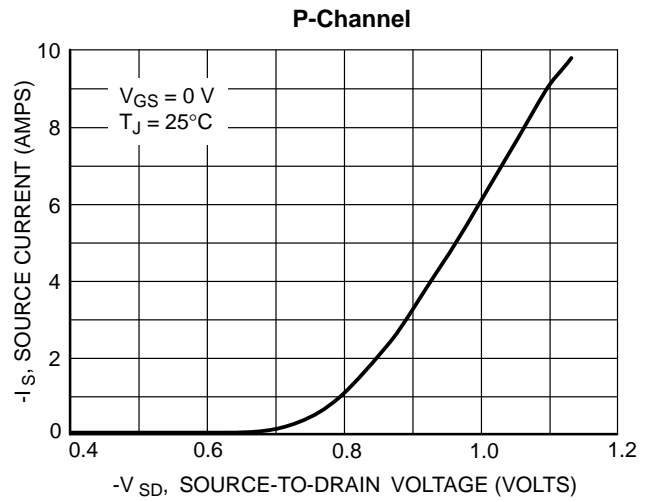


Figure 20. Diode Forward Voltage versus Current

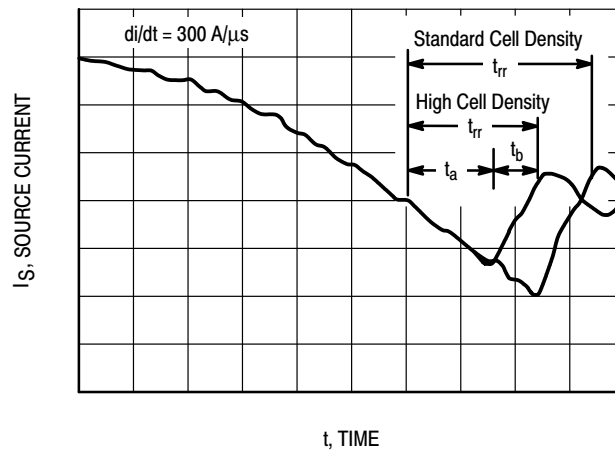


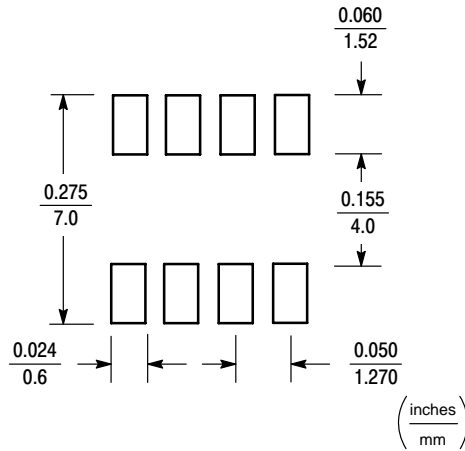
Figure 21. Reverse Recovery Time ( $t_{rr}$ )

## INFORMATION FOR USING THE SO-8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self-align when subjected to a solder reflow process.



### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.

- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 22 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows

temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177-189 °C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

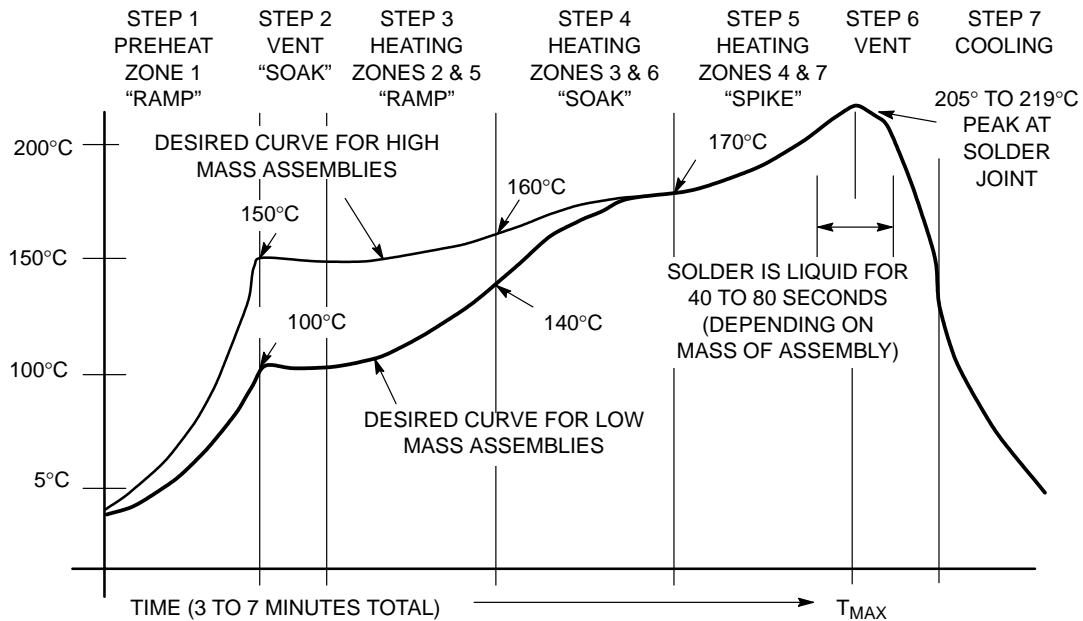


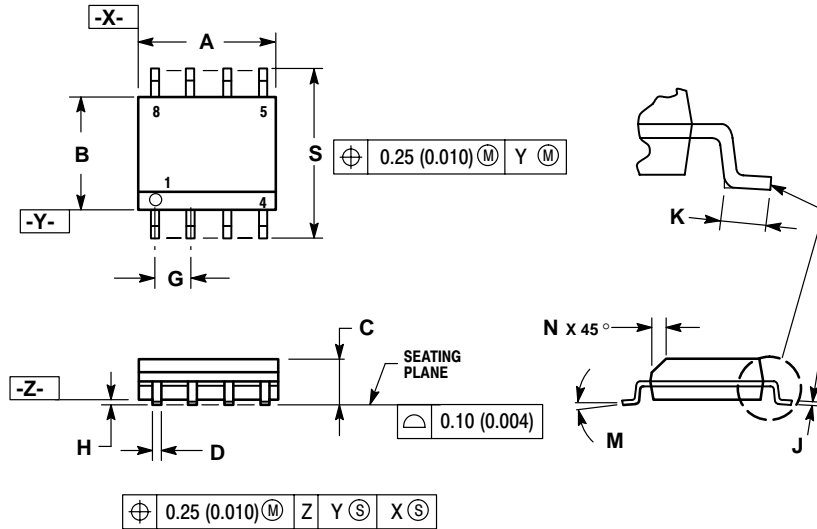
Figure 22. Typical Solder Heating Profile



# NTMC1300R2

## PACKAGE DIMENSIONS

SO-8  
CASE 751-07  
ISSUE AA




### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0.0	8.0	0.0	8.0
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### STYLE 11:

- PIN 1:
1. SOURCE 1
  2. GATE 1
  3. SOURCE 2
  4. GATE 2
  5. DRAIN 2
  6. DRAIN 2
  7. DRAIN 1
  8. DRAIN 1

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051

**Phone:** 81-3-5773-3850

**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local  
Sales Representative.