

MOS FIELD EFFECT TRANSISTOR

NP82N055CLE, NP82N055DLE, NP82N055ELE

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

RDS(on)1 = 8.4 m Ω MAX. (VGS = 10 V, ID = 41 A)

RDS(on)2 = 11 m Ω MAX. (VGS = 5 V, ID = 41 A)

- Low Ciss : Ciss = 4750 pF (TYP.)
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP82N055CLE	TO-220AB
NP82N055DLE	TO-262
NP82N055ELE	TO-263

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage	Voss	55	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC) Note1	ID(DC)	±82	Α
Drain Current (Pulse) Note2	D(pulse)	±328	Α
Total Power Dissipation (T _A = 25°C)	P⊤	1.8	W
Total Power Dissipation (Tch = 25°C)	P⊤	110	W
Single Avalanche Current	las	T.B.D.	Α
Single Avalanche Energy Note3	Eas	T.B.D.	mJ
Channel Temperature	Tch	175	°C
Storage Temperature	T_{stg}	-55 to +175	°C

Notes 1. Package Limit = \pm 75 A

- **2.** PW \leq 10 μ s, Duty cycle \leq 1 %
- 3. Starting Tch = 25°C, RG = 25 Ω , VGS = 20 V \rightarrow 0 V

THERMAL RESISTANCE

Channel to Case	Rth(ch-c)	1.36	°C/W
Channel to Ambient	Rth(ch-a)	83.3	°C/W

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.



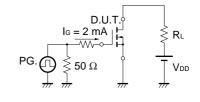
ELECTRICAL CHARACTERISTICS (TA = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 41 A		6.7	8.4	mΩ
	RDS(on)2	Vgs = 5 V, ID = 41 A		7.9	11	mΩ
	RDS(on)3	Vgs = 4.5 V, ID = 41 A		8.2	12	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	$V_{DS} = 10 \text{ V}, \text{ ID} = 250 \mu\text{A}$	1.5	2.0	2.5	V
Forward Transfer Admittance	y fs	V _{DS} = 10 V, I _D = 41 A	25	50		S
Drain Leakage Current	IDSS	Vps = 55 V, Vgs = 0			10	μΑ
Gate to Source Leakage Current	Igss	V _{GS} = ±20 V, V _{DS} = 0			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 25 V, V _{GS} = 0, f = 1 MHz		4750	7130	pF
Output Capacitance	Coss			840	1260	pF
Reverse Transfer Capacitance	Crss			340	610	pF
Turn-on Delay Time	td(on)	$I_D = 41 \text{ A}, V_{GS(on)} = 10 \text{ V}, V_{DD} = 28 \text{ V},$		100	220	ns
Rise Time	t r	$R_G = 10 \Omega$		550	1380	ns
Turn-off Delay Time	td(off)			200	400	ns
Fall Time	t f			330	830	ns
Total Gate Charge 1	Q _{G1}	ID = 82 A, VDD = 44 V, VGS = 10 V		72	110	nC
Total Gate Charge 2	Q _{G2}	ID = 82 A, VDD = 44 V, VGS = 5 V		51	77	nC
Gate to Source Charge	Qgs			11		nC
Gate to Drain Charge	Q _{GD}			20		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 82 A, VGS = 0		1.0		V
Reverse Recovery Time	trr	IF = 82 A, VGS = 0, di/dt = $100A/\mu$ S		48		ns
Reverse Recovery Charge	Qrr			100		nC

TEST CIRCUIT 1 SWITCHING TIME

$PG. \bigcap_{RG} RG = 10 \ \Omega$ $V_{GS} \bigvee_{Wave \ Form} V_{DD}$ $V_{GS} \bigvee_{Wave \ Form} V_{GS(on)} 90 \%$ $V_{GS} \bigvee_{Wave \ Form} V_{DD} \bigvee_{Wave \ Form} V_{DD} \bigvee_{UD} V_{GS(on)} V_{GS$

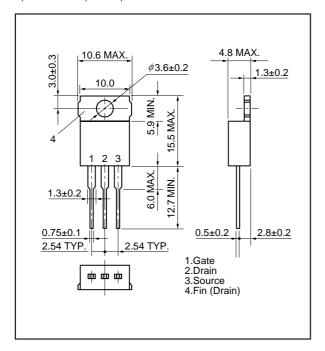
TEST CIRCUIT 2 GATE CHARGE



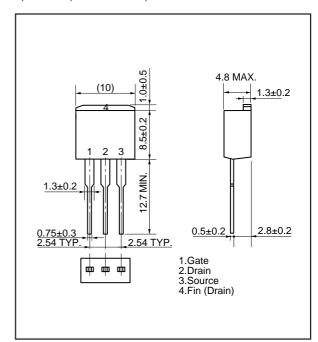


PACKAGE DRAWINGS (Unit: mm)

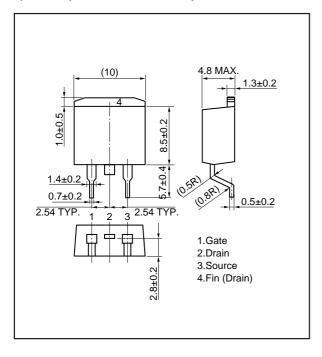
1) TO-220AB (MP-25)



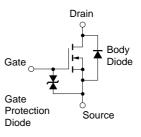
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (JEDEC TYPE: MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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