

MOS FIELD EFFECT TRANSISTOR

NP48N055CLE, NP48N055DLE, NP48N055ELE

SWITCHING

N-CHANNEL POWER MOS FET

INDUSTRIAL USE

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
- ★ $R_{DS(on)1} = 17 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 24 \text{ A)}$
- ★ $R_{DS(on)2} = 21 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5 \text{ V, } I_D = 24 \text{ A)}$
- ★ • Low C_{iss} : $C_{iss} = 1970 \text{ pF TYP.}$
- Built-in gate protection diode

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP48N055CLE	TO-220AB(MP-25)
NP48N055DLE	TO-262(MP-25 Fin Cut)
NP48N055ELE	TO-263(MP-25ZJ)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage	V_{DSS}	55	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 48	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 192	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_T	1.8	W
★ Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_T	85	W
★ Single Avalanche Current ^{Note2}	I_{AS}	46 / 27 / 10	A
★ Single Avalanche Energy ^{Note2}	E_{AS}	2.1 / 73 / 100	mJ
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +175	$^\circ\text{C}$

Notes 1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1 \%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

THERMAL RESISTANCE

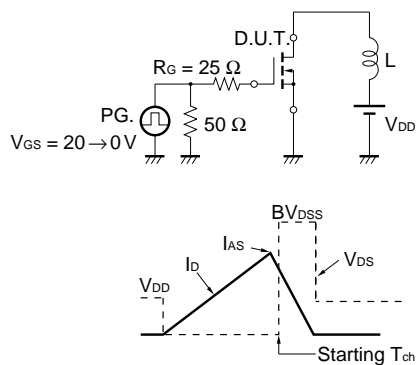
★ Channel to Case	$R_{th(ch-C)}$	1.76	$^\circ\text{C/W}$
★ Channel to Ambient	$R_{th(ch-A)}$	83.3	$^\circ\text{C/W}$

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

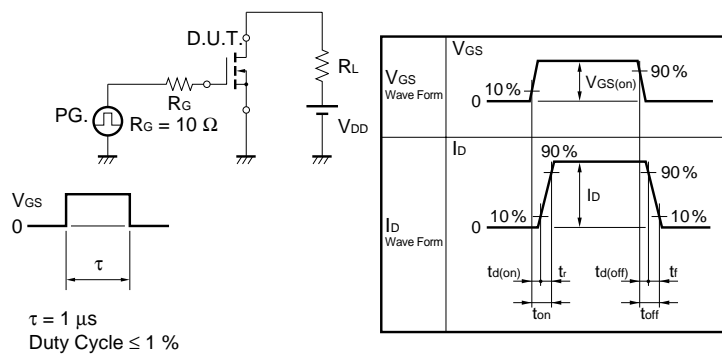
★ ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 24 A		13	17	mΩ
	R _{DS(on)2}	V _{GS} = 5 V, I _D = 24 A		16	21	mΩ
	R _{DS(on)3}	V _{GS} = 4.5 V, I _D = 24 A		18	24	mΩ
Gate to Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 24 A	13	25		S
Drain Leakage Current	I _{DSS}	V _{DS} = 55 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		1970	3000	pF
Output Capacitance	C _{oss}			250	380	pF
Reverse Transfer Capacitance	C _{rss}			130	240	pF
Turn-on Delay Time	t _{d(on)}	I _D = 24 A, V _{GS(on)} = 10 V, V _{DD} = 28 V, R _G = 10 Ω		44	100	ns
Rise Time	t _r			490	1230	ns
Turn-off Delay Time	t _{d(off)}			100	210	ns
Fall Time	t _f			160	410	ns
Total Gate Charge 1	Q _{G1}	I _D = 48 A, V _{DD} = 44 V, V _{GS} = 10 V		40	60	nC
Total Gate Charge 2	Q _{G2}	I _D = 48 A, V _{DD} = 44 V, V _{GS} = 5 V		21	32	nC
Gate to Source Charge	Q _{GS}			7		nC
Gate to Drain Charge	Q _{GD}			10		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 48 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 48 A, V _{GS} = 0 V, di/dt = 100 A/μs		40		ns
Reverse Recovery Charge	Q _{rr}			55		nC

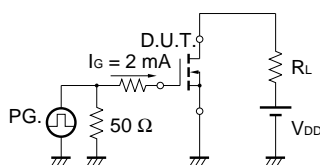
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

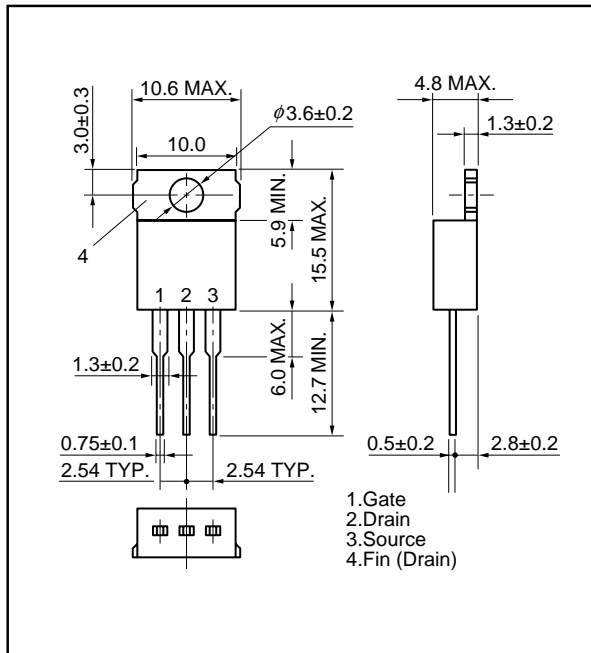


TEST CIRCUIT 3 GATE CHARGE

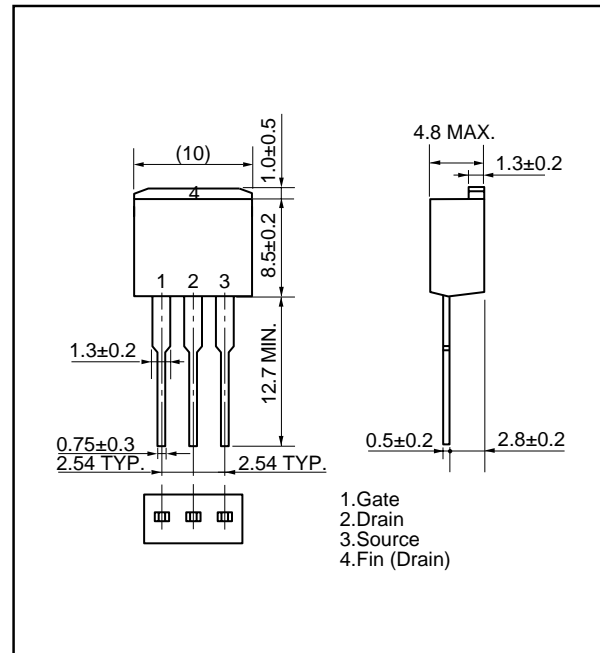


PACKAGE DRAWINGS (Unit: mm)

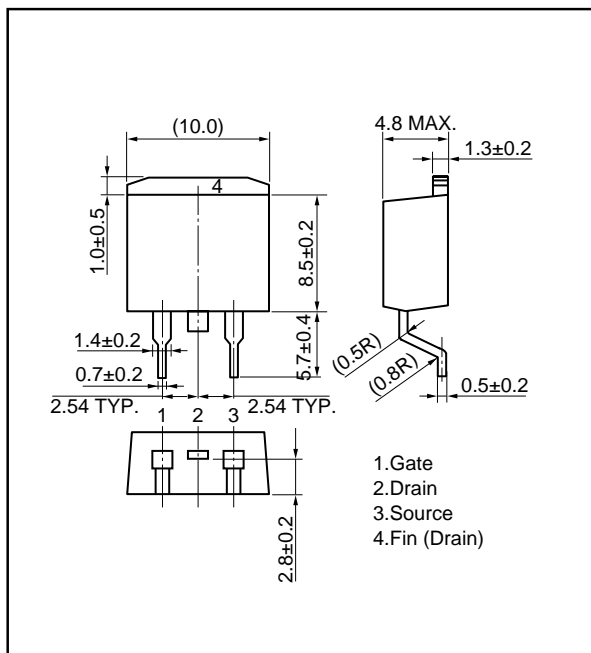
1) TO-220AB (MP-25)



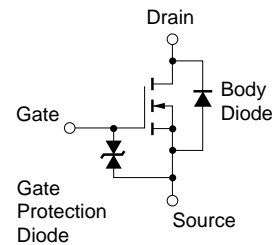
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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